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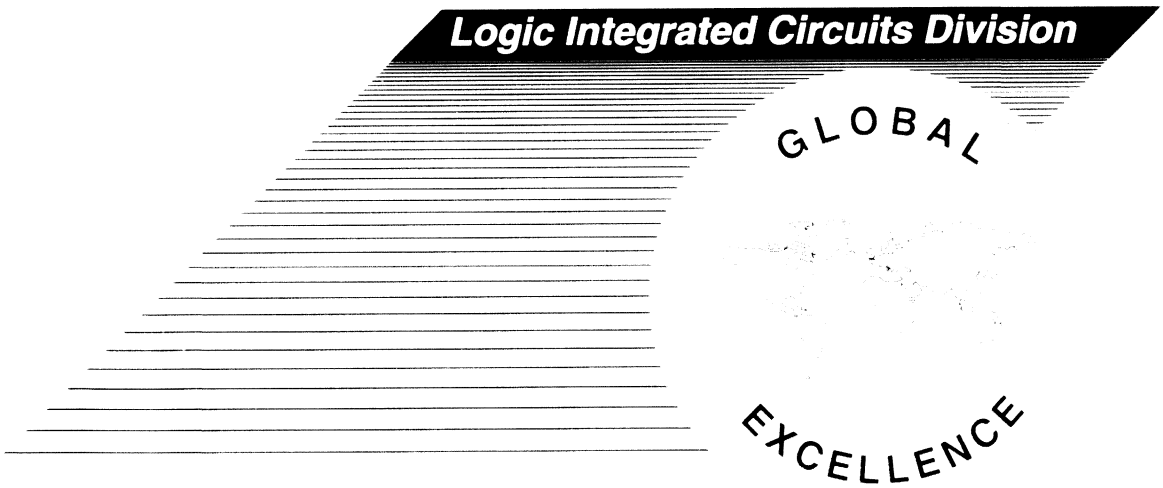
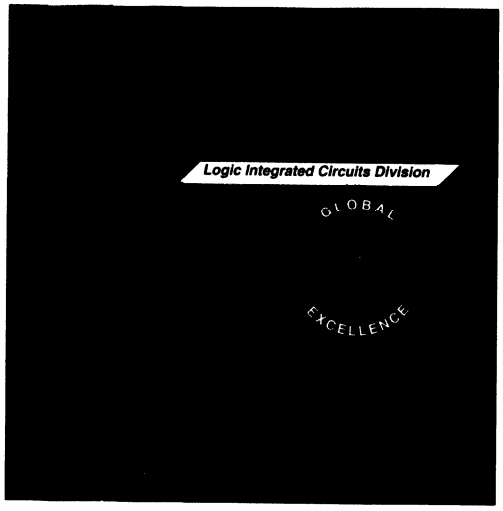
MECL Data





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MECL INTEGRATED CIRCUITS

This book presents technical data for a broad line of MECL integrated circuits. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, selector guides are included to simplify the task of choosing the best combination of circuits for optimum system architecture.

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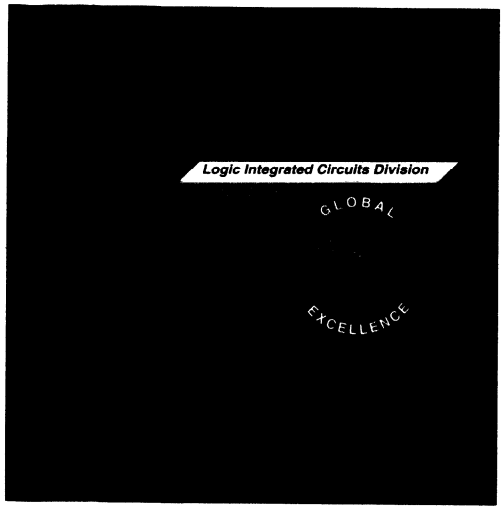

General Information

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GENERAL INFORMATION
SECTION 1 — HIGH-SPEED LOGIC

High speed logic is used whenever improved system performance would increase a product's market value. For a given system design, high-speed logic is the most direct way to improve system performance and emitter-coupled logic (ECL) is today's fastest form of digital logic. Emitter-coupled logic offers both the logic speed and logic features to meet the market demands for higher performance systems.

1

MECL PRODUCTS

Motorola introduced the original monolithic emitter-coupled logic family with MECL I (1962) and followed this with MECL II (1966). These two families are now obsolete and have given way to the MECL III (MC1600 series), MECL 10K, PLL (MC12000 series) and the new MECL 10H families.

Chronologically the third family introduced, MECL III (1968) is a higher power, higher speed logic. Typical 1 ns edge speeds and propagation delays along with greater than 500 MHz flip-flop toggle rates, make MECL III useful for high-speed test and communications equipment. Also, this family is used in the high-speed sections and critical timing delays of larger systems. For more general purpose applications, however, trends in large high-speed systems showed the need for an easy-to-use logic family with propagation delays on the order of 2 ns. To match this requirement, the MECL 10,000 Series was introduced in 1971.

An important feature of MECL 10K is its compatibility with MECL III to facilitate using both families in the same system. A second important feature is its significant power economy — MECL 10K gates use less than one-half the power of MECL III.

Motorola introduced the MECL 10H product family in 1981. This latest MECL family features 100% improvements in propagation delay and clock speeds while maintaining power supply currents equal to MECL 10K. MECL 10H is voltage compensated allowing guaranteed dc and switching parameters over a ±5% power supply range. Noise margins have been improved by 75% over the MECL 10K series.

Compatibility with MECL 10K and MECL III is a key element in allowing users to enhance existing systems by increasing the speed in critical timing areas. Also, many MECL 10H devices are pin out/functional duplications of the MECL 10K series devices. The emphasis of this new family will be placed on more powerful logic functions having more complexity and greater performance. With 1.0 ns propagation delays and 25 mW per gate, MECL 10H features the best speed-power product of any ECL logic family available today.

MECL FAMILY COMPARISONS

Feature	MECL 10H	MECL 10K		MECL III
		10,100 Series	10,200 Series	
1. Gate Propagation Delay	1.0 ns	2.0 ns	1.5 ns	1.0 ns
2. Output Edge Speed*	1.0 ns	3.5 ns	2.5 ns	1.0 ns
3. Flip-Flop Toggle Speed	250 MHz min	125 MHz min	200 MHz min	300–500 MHz min
4. Gate Power	25 mW	25 mW	25 mW	60 mW
5. Speed Power Product	25 pJ	50 pJ	37 pJ	60 pJ

*Output edge speed: MECL 10K/10H measured 20% to 80%, MECL III measured 10% to 90% of E out.

FIGURE 1a — GENERAL CHARACTERISTICS

Ambient Temperature Range	MECL 10H	MECL 10K	MECL III	PLL
0° to 75°C	MC10H100 Series			MC12000 Series
−30°C to +85°C		MC10100 Series MC10200 Series	MC1600 Series	MC12000 Series

FIGURE 1b — OPERATING TEMPERATURE RANGE

MECL IN PERSPECTIVE

In evaluating any logic line, speed and power requirements are the obvious primary considerations. Figure 1 provides the basic parameters of the MECL 10H, MECL 10K, and MECL III families. But these provide only the start of any comparative analysis, as there are a number of other important features that make MECL highly desirable for system implementation. Among these:

Complementary Outputs cause a function and its complement to appear simultaneously at the device outputs, without the use of external inverters. It reduces package count by eliminating the need for associated invert functions and, at the same time, cuts system power requirements and reduces timing differential problems arising from the time delays introduced by inverters.

High Input Impedance and Low Output Impedance permit large fan out and versatile drive characteristics.

Insignificant Power Supply Noise Generation, due to differential amplifier design which eliminates current spikes even during signal transition period.

Nearly Constant Power Supply Current Drain simplifies power-supply design and reduces costs.

Low Cross-Talk due to low-current switching in signal path and small (typically 850 mV) voltage swing, and to relatively long rise and fall times.

Wide Variety of Functions, including complex functions facilitated by low power dissipation (particularly in MECL 10H and MECL 10K series). A basic MECL 10K gate consumes less than 8 mW in on-chip power in some complex functions.

Wide Performance Flexibility due to differential amplifier design which permits MECL circuits to be used as linear as well as digital circuits.

Transmission Line Drive Capability is afforded by the open emitter outputs of MECL devices. No "Line Drivers" are listed in MECL families, because *every* device is a line driver.

Wire-ORing reduces the number of logic devices required in a design by producing additional OR gate functions with only an interconnection.

Twisted Pair Drive Capability permits MECL circuits to drive twisted-pair transmission lines as long as 1000 feet.

Wire-Wrap Capability is possible with the MECL 10K family because of the slow rise and fall time characteristic of the circuits.

Open Emitter-Follower Outputs are used for MECL outputs to simplify signal line drive. The outputs match any line impedance and the absence of internal pulldown resistors saves power.

Input Pulldown Resistors of approximately 50 kΩ permit unused inputs to remain unconnected for easier circuit board layout.

MECL APPLICATIONS

Motorola's MECL product lines are designed for a wide range of systems needs. Within the computer market, MECL 10K is used in systems ranging from special purpose peripheral controllers to large mainframe computers. Big growth areas in this market include disk and communication channel controllers for larger systems and high performance minicomputers.

The industrial market primarily uses MECL for high performance test systems such as IC or PC board testers. However, the high bandwidths of MECL 10H, MECL 10K, MECL III, and MC12,000 are required for many frequency synthesizer systems using high speed phase lock loop networks. MECL will continue to grow in the industrial market through complex medical electronic products and high performance process control systems.

MECL 10K and MECL III have been accepted within the Federal market for numerous signal processors and navigation systems. Full military temperature range MECL 10K is offered in the MC10500 and MC10600 Series, and in the PLL family as the MC12500 Series.

BASIC CONSIDERATIONS FOR HIGH-SPEED LOGIC DESIGN

High-speed operation involves only four considerations that differ significantly from operation at low and medium speeds:

1. Time delays through interconnect wiring, which may have been ignored in medium-speed systems, become highly important at state-of-the-art speeds.
2. The possibility of distorted waveforms due to reflections on signal lines increases with edge speed.
3. The possibility of "crosstalk" between adjacent signal leads is proportionately increased in high-speed systems.
4. Electrical noise generation and pick-up are more detrimental at higher speeds.

In general, these four characteristics are speed- and frequency-dependent, and are virtually independent of the type of logic employed. The merit of a particular logic family is measured by how well it compensates for these deleterious effects in system applications.

The interconnect-wiring time delays can be reduced only by reducing the length of the interconnecting lines. At logic speeds of two nanoseconds, an equivalent "gate delay" is introduced by every foot of interconnecting wiring. Obviously, for functions interconnected within a single monolithic chip, the time delays of signals travelling from one function to another are insignificant. But for a great many externally interconnected parts, this can soon add up to an appreciable delay time. Hence, the greater the number of functions per chip, the higher the system speed. *MECL circuits, particularly those of the MECL 10K and MECL 10H Series are designed with a propensity toward complex functions to enhance overall system speed.*

Waveform distortion due to line reflections also becomes troublesome principally at state-of-the-art speeds. At slow and medium speeds, reflections on interconnecting lines are not usually a serious problem. At higher speeds, however, line lengths can approach the wavelength of the signal and improperly terminated lines can result in reflections that will cause false triggering (see Figure 2). The solution, as in RF technology, is to employ "transmission-line" practices and properly terminate each signal line with its characteristic impedance at the end of its run. *The low-impedance, emitter-follower outputs of MECL circuits facilitate transmission-line practices without upsetting the voltage levels of the system.*

The increased affinity for crosstalk in high-speed circuits is the result of very steep leading and trailing edges (fast rise and fall times) of the high-speed signal. These steep wavefronts are rich in harmonics that couple readily to adjacent circuits. *In the design of MECL 10K and*

MECL 10H, the rise and fall times have been deliberately slowed. This reduces the affinity for crosstalk without compromising other important performance parameters.

From the above, it is evident that the MECL logic line is not simply capable of operating at high speed, but has been specifically designed to reduce the problems that are normally associated with high-speed operation.

CIRCUIT DESCRIPTION

The typical MECL 10K circuit, Figure 3, consists of a differential-amplifier input circuit, a temperature and voltage compensated bias network, and emitter-follower outputs to restore dc levels and provide buffering for transmission line driving. High fan-out operation is possible because of the high input impedance of the differ-

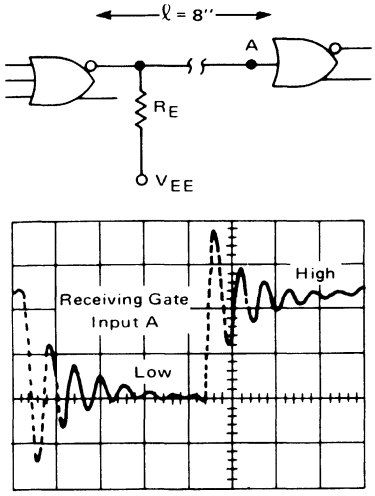


FIGURE 2a — UNTERMINATED TRANSMISSION LINE (No Ground Plane Used)

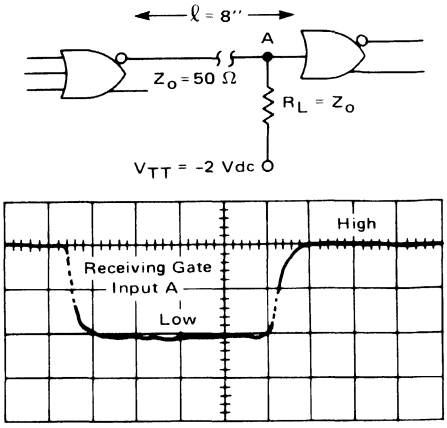


FIGURE 2b — PROPERLY TERMINATED TRANSMISSION LINE (Ground Plane Added)

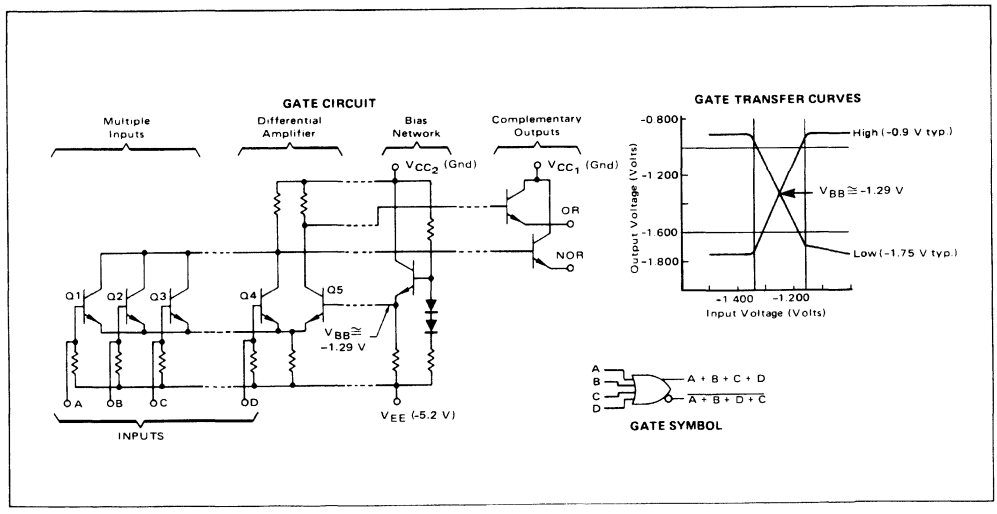


FIGURE 3 — MECL 10K GATE STRUCTURE AND SWITCHING BEHAVIOR

ential amplifier input and the low output impedance of the emitter follower outputs. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function. The design of the MECL 10H gate is unchanged, with two exceptions. The bias network has been replaced with a voltage regulator, and the differential amplifier source resistor has been replaced with a constant current source. (See section 2 for additional MECL 10H information.)

Power-Supply Connections — Any of the power supply levels, V_{TT}, V_{CC}, or V_{EE} may be used as ground; however, the use of the V_{CC} node as ground results in best noise immunity. In such a case: $V_{CC} = 0$, $V_{TT} = -2.0$ V, $V_{EE} = -5.2$ V.

System Logic Specifications — The output logic swing of 0.85 V, as shown by the typical transfer characteristics curve, varies from a LOW state of $V_{OL} = -1.75$ V to a HIGH state of $V_{OH} = -0.9$ V with respect to ground.

Positive logic is used when reference is made to logical "0's" or "1's." Then

"0" = −1.75 V = LOW
"1" = −0.9 V = HIGH
typical

Circuit Operation — Beginning with all logic inputs LOW (nominal −1.75 V), assume that Q1 through Q4 are cut off because their P-N base-emitter junctions are not conducting, and the forward-biased Q5 is conducting. Under these conditions, with the base of Q5 held at −1.29 V by the V_{BB} network, its emitter will be one diode drop (0.8 V) more negative than its base, or −2.09 V. (The 0.8 V differential is a characteristic of this P-N junction.) The base-to-emitter differential across Q1 — Q4 is then the difference between the common emitter voltage (−2.09 V) and the LOW logic level (−1.75 V) or 0.34 V. This is less than the threshold voltage of Q1 through Q4 so that these transistors will remain cut off.

When any one (or all) of the logic inputs are shifted upward from the −1.75 V LOW state to the −0.9 V HIGH state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on. When this happens, the voltage at the common-emitter point rises from −2.09 V to −1.7 (one diode drop below the −0.9 V base voltage of the input transistor), and since the base voltage of the fixed-bias transistor (Q5) is held at −1.29 V, the base-emitter voltage Q5 cannot sustain conduction. Hence, this transistor is cut off.

This action is reversible, so that when the input signal(s) return to the LOW state, Q1 – Q4 are again turned off and Q5 again becomes forward biased. The collector voltages resulting from the switching action of Q1 – Q4 and Q5 are transferred through the output emitter-follower to the output terminal. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

DEFINITIONS OF LETTER SYMBOLS AND ABBREVIATIONS

Current:

I_{CC}	Total power supply current drawn from the positive supply by a MECL unit under test.
I_{CBO}	Leakage current from input transistor on MECL devices without pulldown resistors when test voltage is applied.
I_{CCH}	Current drain from V_{CC} power supply with all inputs at logic HIGH level.
I_{CCL}	Current drain from V_{CC} power supply with all inputs at logic LOW level.
I_E	Total power supply current drawn from a MECL test unit by the negative power supply.
I_F	Forward diode current drawn from an input of a saturated logic-to-MECL translator when that input is at ground potential.
I_{in}	Current into the input of the test unit when a maximum logic HIGH ($V_{IH\ max}$) is applied at that input.
I_{INH}	HIGH level input current into a node with a specified HIGH level ($V_{IH\ max}$) logic voltage applied to that node. (Same as I_{in} for positive logic.)
I_{INL}	LOW level input current, into a node with a specified LOW level ($V_{IL\ min}$) logic voltage applied to that node.
I_L	Load current that is drawn from a MECL circuit output when measuring the output HIGH level voltage.
I_{OH}	HIGH level output current: the current flowing into the output, at a specified HIGH level output voltage.
I_{OL}	LOW level output current: the current flowing into the output, at a specified LOW level output voltage.
I_{OS}	Output short circuit current.
I_{out}	Output current (from a device or circuit, under such conditions mentioned in context).
I_R	Reverse current drawn from a transistor input of a test unit when V_{EE} is applied at that input.
I_{SC}	Short-circuit current drawn from a translator saturating output when that output is at ground potential.

Voltage:

V_{BB}	Reference bias supply voltage.
V_{BE}	Base-to-emitter voltage drop of a transistor at specified collector and base currents.
V_{CB}	Collector-to-base voltage drop of a transistor at specified collector and base currents.
V_{CC}	General term for the most positive power supply voltage to a MECL device (usually ground, except for translator and interface circuits).
V_{CC1}	Most positive power supply voltage (output devices). (Usually ground for MECL devices.)

Voltage (cont.):

V_{CC2} Most positive power supply voltage (current switches and bias driver). (Usually ground for MECL devices.)

V_{EE} Most negative power supply voltage for a circuit (usually −5.2 V for MECL devices).

V_F Input voltage for measuring I_F on TTL interface circuits.

V_{IH} Input logic HIGH voltage level (nominal value).

$V_{IH\ max}$ Maximum HIGH level input voltage: The most positive (least negative) value of high-level input voltage, for which operation of the logic element within specification limits is guaranteed.

V_{IHA} Input logic HIGH threshold voltage level.

$V_{IHA\ min}$ Minimum input logic HIGH level (threshold) voltage for which performance is specified.

$V_{IH\ min}$ Minimum HIGH level input voltage: The least positive (most negative) value of HIGH level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Input logic LOW voltage level (nominal value).

$V_{IL\ max}$ Maximum LOW level input voltage: The most positive (least negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{ILA} Input logic LOW threshold voltage level.

$V_{ILA\ max}$ Maximum input logic LOW level (threshold) voltage for which performance is specified.

$V_{IL\ min}$ Minimum LOW level input voltage: The least positive (most negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{in} Input voltage (to a circuit or device).

V_{max} Maximum (most positive) supply voltage, permitted under a specified set of conditions.

V_{OH} Output logic HIGH voltage level: The voltage level at an output terminal for a specified output current, with the specified conditions applied to establish a HIGH level at the output.

V_{OHA} Output logic HIGH threshold voltage level.

$V_{OHA\ min}$ Minimum output HIGH threshold voltage level for which performance is specified.

$V_{OH\ max}$ Maximum output HIGH or high-level voltage for given inputs.

$V_{OH\ min}$ Minimum output HIGH or high-level voltage for given inputs.

V_{OL} Output logic LOW voltage level: The voltage level at the output terminal for a specified output current, with the specified conditions applied to establish a LOW level at the output.

V_{OLA} Output logic LOW threshold voltage level.

$V_{OLA\ max}$ Maximum output LOW threshold voltage level for which performance is specified.

$V_{OL\ max}$ Maximum output LOW level voltage for given inputs.

$V_{OL\ min}$ Minimum output LOW level voltage for given inputs.

V_{TT} Line load-resistor terminating voltage for outputs from a MECL device.

V_{OLS1} Output logic LOW level on MECL 10,000 line receiver devices with all inputs at V_{EE} voltage level.

V_{OLS2} Output logic LOW level on MECL 10,000 line receiver devices with all inputs open.

Time Parameters:

t+ Waveform rise time (LOW to HIGH), 10% to 90%, or 20% to 80%, as specified.

t− Waveform fall time (HIGH to LOW), 90% to 10%, or 80% to 20%, as specified.

t_r Same as t+

t_f Same as t−

t+− Propagation Delay, see Figure 9.

t−+ Propagation Delay, see Figure 9.

t_{pd} Propagation delay, input to output from the 50% point of the input waveform at pin x (falling edge noted by — or rising edge noted by +) to the 50% point of the output waveform at pin y (falling edge noted by − or rising edge noted by +). (Cf Figure 9.)

t_{x+} Output waveform rise time as measured from 10% to 90% or 20% to 80% points on waveform (whichever is specified) at pin x with input conditions as specified.

t_{x-} Output waveform fall time as measured from 90% to 10% or 80% to 20% points on waveform (whichever is specified) at pin x, with input conditions as specified.

f_{Tog} Toggle frequency of a flip-flop or counter device.

f_{shift} Shift rate for a shift register.

Read Mode (Memories)

t_{ACS} Chip Select Access Time

t_{RCS} Chip Select Recovery Time

t_{AA} Address Access Time

Write Mode (Memories)

t_W Write Pulse Width

t_{WSD} Data Setup Time Prior to Write

t_{WHD} Data Hold Time After Write

t_{WSA} Address setup time prior to write

t_{WHA} Address hold time after write

t_{WSCS} Chip select setup time prior to write

t_{WHCS} Chip select hold time after write

t_{WS} Write disable time

t_{WR} Write recovery time

Temperature:

T_{stg}	Maximum temperature at which device may be stored without damage or performance degradation.
T_J	Junction (or die) temperature of an integrated circuit device.
T_A	Ambient (environment) temperature existing in the immediate vicinity of an integrated circuit device package.
θ_{JA}	Thermal resistance of an IC package, junction to ambient.
θ_{JC}	Thermal resistance of an IC package, junction to case.
lfpm	Linear feet per minute.
θ_{CA}	Thermal resistance of an IC package, case to ambient.

Miscellaneous:

e_g	Signal generator inputs to a test circuit.
TP_{in}	Test point at input of unit under test.
TP_{out}	Test point at output of unit under test.
D.U.T.	Device under test.
C_{in}	Input capacitance.
C_{out}	Output capacitance.
Z_{out}	Output impedance.
P_D	The total dc power applied to a device, not including any power delivered from the device to a load.
R_L	Load Resistance.
R_T	Terminating (load) resistor.
R_p	An input pull-down resistor (i.e., connected to the most negative voltage).
P.U.T.	Pin under test.

1

MECL POSITIVE AND NEGATIVE LOGIC

INTRODUCTION

The increasing popularity and use of emitter coupled logic has created a dilemma for some logic designers. Saturated logic families such as TTL have traditionally been designed with the NAND function as the basic logic function, however, the basic ECL logic function is the NOR function (positive logic). Therefore, the designer may either design ECL systems with positive logic using the NOR, or design with negative logic using the NAND. Which is the more convenient? On the one hand the designer is familiar with positive logic levels and definitions, and on the other hand, he is familiar with implementing systems using NAND functions. Perhaps a presentation of the basic definitions and characteristics of positive and negative logic will clarify the situation and eliminate misunderstanding.

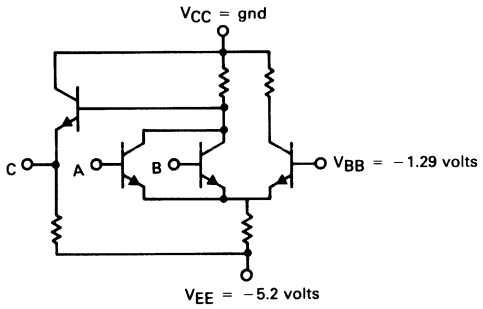


TABLE 1

INPUTS		OUTPUT
A	B	C
LO	LO	HI
LO	HI	LO
HI	LO	LO
HI	HI	LO

HI = −0.9 volts
LO = −1.7 volts

TABLE 2

NEGATIVE LOGIC

INPUTS		OUTPUT
A	B	C
1	1	0
1	0	1
0	1	1
0	0	1

C = A + B

TABLE 3

POSITIVE LOGIC

INPUTS		OUTPUT
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

C = A + B

FIGURE 1 — Basic MECL Gate Circuit and Logic Function In Positive and Negative Nomenclature.

LOGIC EQUIVALENCES

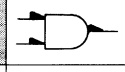
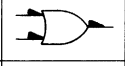
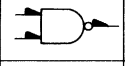
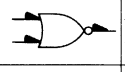
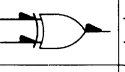
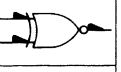
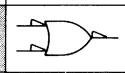
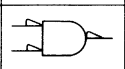
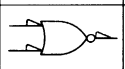
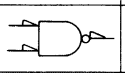
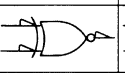
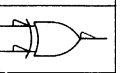
Binary logic must have two states to represent the binary 1 and 0. With ECL the typical states are a high level of −0.9 volts and a low level of −1.7 volts. Two choices are possible then to represent the binary 1 and 0. Positive logic defines the 1 or "true" state as the most positive voltage level, whereas negative logic defines the most negative voltage level as the 1 or "true" state. Because of the difference in definition of states, the basic ECL gate is a NOR function in positive logic and is a NAND function in negative logic.

Figure 1 more clearly shows the above comparison of functions. Table I lists the output voltage level as a function of input voltage levels of the MECL gate circuit shown. Table 2 translates the voltage levels into the appropriate negative logic levels which show the function to be $C = \overline{A \cdot B}$; that is, the circuit performs the NAND function. Table 3 translates the equivalent positive logic function into $C = \overline{A + B}$, the NOR function.

Similar comparisons could be made for other positive logic functions. As an example, the positive OR function translates to the negative AND function. Figure 2 shows a comparison of several common logic functions.

Any function available in a logic family may be expressed in terms of positive or negative logic, bearing in mind the definition of logic levels. The choice of logic definition, as previously stated, is dependent on the designer. Motorola provides both positive and negative logic symbols on data sheets for the popular MECL 10,000 logic series.

FIGURE 2 — Comparative Positive and Negative Logic Functions.

POSITIVE LOGIC							
INPUTS							
A	B	AND	OR	NAND	NOR	EXOR	COIN*
LO	LO	LO	LO	HI	HI	LO	HI
LO	HI	LO	HI	HI	LO	HI	LO
HI	LO	LO	HI	HI	LO	HI	LO
HI	HI	HI	HI	LO	LO	LO	HI
A	B	OR	AND	NOR	NAND	COIN*	EXOR
INPUTS							
NEGATIVE LOGIC							

*Coincidence

SUMMARY

Conversion from one logic form to another or the use of a particular logic form need not be a complicated process. If the designer uses the logic form with which he is familiar and bears in mind the previously mentioned definition of levels, problems arising from definition of logic functions should be minimized.

REFERENCE

Y. Chu, Digital Computer Design Fundamentals New York, McGraw-Hill, 1962

SECTION II — TECHNICAL DATA

GENERAL CHARACTERISTICS AND SPECIFICATIONS

(See pages 1-5 through 1-7 for definitions of symbols and abbreviations.)

In subsequent sections of this Data Book, the important MECL parameters are identified and characterized, and complete data provided for each of the functions. To make this data as useful as possible, and to avoid a great deal of repetition, the data that is common to all functional blocks in a line is not repeated on each individual sheet. Rather, these common characteristics, as well as the application information that applies to each family, are discussed in this section.

In general, the common characteristics of major importance are:

Maximum Ratings, including both dc and ac characteristics and temperature limits;

Transfer Characteristics, which define logic levels and switching thresholds;

DC Parameters, such as output levels, threshold levels, and forcing functions.

AC Parameters, such as propagation delays, rise and fall times and other time dependent characteristics.

In addition, this section will discuss general layout and design guides that will help the designer in building and testing systems with MECL circuits.

LETTER SYMBOLS AND ABBREVIATIONS

Throughout this section, and in the subsequent data sheets, letter symbols and abbreviations will be used in discussing electrical characteristics and specifications. The symbols used in this book, and their definitions, are listed on the preceding pages.

MAXIMUM RATINGS

The limit parameters beyond which the life of the devices may be impaired are given in Figure 4a. In addition, Table 4b provides certain limits which, if exceeded, will not damage the devices, but could degrade the performance below that of the guaranteed specifications.

FIGURE 4a — LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

Characteristic	Symbol	Unit	MECL 10H	MECL 10K	MECL III
Power Supply	V_{EE}	Vdc	−8.0 to 0	−8.0 to 0	−8.0 to 0
Input Voltage (V_{CC} = 0)	V_{in}	Vdc	0 to V_{EE}	0 to V_{EE}	0 to V_{EE}
Output Source Current Continuous	I_{out}	mAdc	50	50	40
Output Source Current Surge	I_{out}	mAdc	100	100	—
Storage Temperature	T_{stg}	°C	−65 to +150	−65 to +150	−65 to +150
Junction Temperature Ceramic Package①	T_J	°C	165	165	165②
Junction Temperature Plastic Package③	T_J	°C	140	140	140

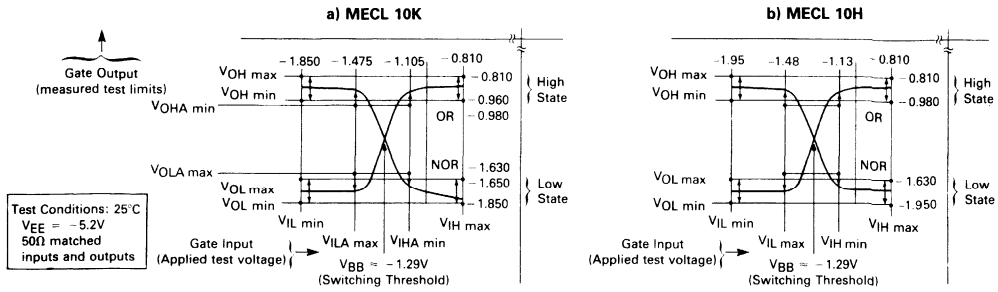
NOTES: 1. Maximum T_J may be exceeded (≤ 250°C) for short periods of time (≤ 240 hours) without significant reduction in device life.
2. Except MC1670 which has a maximum junction temperature = 145°C.
3. For long term (≥ 10 yrs.) max T_J of 110°C required. Max T_J may be exceeded (≤ 175°C) for short periods of time (≤ 240 hours) without significant reduction in device life.

FIGURE 4b — LIMITS BEYOND WHICH PERFORMANCE MAY BE DEGRADED

Characteristics	Symbol	Unit	MECL 10H	MECL 10K	MECL III
Operating Temperature Range Commercial①	T_A	°C	0 to +75	−30 to +85	−30 to +85
Supply Voltage (V_{CC} = 0)	V_{EE}	Vdc	−4.94 to −5.46	−4.68 to −5.72②⑤	−4.68 to −5.72②
Output Drive Commercial	—	Ω	50 Ω to −2.0 Vdc	50 Ω to −2.0 Vdc	50 Ω to −2.0 Vdc④

NOTES: 1. With airflow ≥ 500 lfpm.
2. Functionality only. Data sheet limits are specified for −5.2 V ± 0.010 V.
3. Except MC1648 which has an internal output pulldown resistor.
4. Functional and Data sheet limits.
5. MC10137 has a guaranteed supply voltage of −5.2 V to −5.72 V @ −30°C.

FIGURE 5 — MECL TRANSFER CURVES and SPECIFICATION TEST POINTS



1

MECL TRANSFER CURVES

For MECL logic gates, the dual (complementary) outputs must be represented by two transfer curves: one to describe the OR switching action and one to describe the NOR switching action. Typical transfer curves and associated data for the MECL 10K/10H family are shown in Figures 5a and 5b respectively.

It is not necessary to measure transfer curves at all points of the curves. To guarantee correct operation it is sufficient merely to measure two sets of min/max logic level parameters.

The first set is obtained for 10K by applying test voltages, $V_{IL\ min}$ and $V_{IH\ max}$ (sequentially) to the gate inputs, and measuring the OR and NOR output levels to make sure they are between $V_{OL\ max}$ and $V_{OL\ min}$, and $V_{OH\ max}$ and $V_{OH\ min}$ specifications.

The second set of logic level parameters relates to the switching thresholds. This set of data is distinguished by an "A" in symbol subscripts. A test voltage, $V_{ILA\ max}$, is applied to the gate and the NOR and OR outputs are measured to see that they are above the $V_{OHA\ min}$ and below the $V_{OLA\ max}$ levels, respectively. Similar checks are made using the test input voltage $V_{IHA\ min}$.

The result of these specifications insures that:

a) The switching threshold ($\approx V_{BB}$) falls within the darkest rectangle; i.e. switching does not begin outside this rectangle;

b) Quiescent logic levels fall in the lightest shaded ranges;

c) Guaranteed noise immunity is met.

As shown in Figure 6, MECL 10K outputs rise with increasing ambient temperature. All circuits in each family have the same worst-case output level specifications regardless of power dissipation or junction temperature differences to reduce loss of noise margin due to thermal differences.

All of these specifications assume −5.2 V power supply operation. Operation at other power-supply voltages is possible, but will result in further transfer curve changes. Figure 7 gives rate of change of output voltages as a function of power supply.

FIGURE 6 — TYPICAL TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE (MECL 10K)

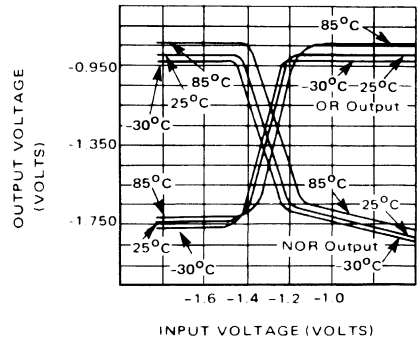


FIGURE 7 — TYPICAL LEVEL CHANGE RATES

Voltage	MECL 10H	MECL 10K	MECL III
$\Delta V_{OH}/\Delta V_{EE}$	0.008	0.016	0.033
$\Delta V_{OL}/\Delta V_{EE}$	0.020	0.250	0.270
$\Delta V_{BB}/\Delta V_{EE}$	0.010	0.148	0.140

NOISE MARGIN

"Noise margin" is a measure of logic circuit's resistance to undesired switching. MECL noise margin is defined in terms of the specification points surrounding the switching threshold. The critical parameters of interest here are those designated with the "A" subscript ($V_{OHA\ min}$, $V_{OLA\ max}$, $V_{IHA\ min}$, $V_{ILA\ max}$) in the transfer characteristic curves. MECL 10H is specified and tested with $V_{OHA\ min}$ equal $V_{OH\ min}$, $V_{OLA\ max}$ equal $V_{OL\ max}$, $V_{IHA\ min}$ equal $V_{IH\ min}$ and $V_{ILA\ max}$ equal $V_{IL\ max}$. Guaranteed noise margin (NM) is defined as follows:

$NM_{HIGH\ LEVEL} = V_{OHA\ min} - V_{IHA\ min}$

$NM_{LOW\ LEVEL} = V_{ILA\ max} - V_{OLA\ max}$

To see how noise margin is computed, assume a MECL gate drives a similar MECL gate, Figure 8.

At a gate input (point B) equal to $V_{ILA\ max}$, MECL gate #2 can begin to enter the shaded transition region.

This is a "worst case" condition, since the $V_{OLA\ max}$ specification point guarantees that no device can enter the transition region before an input equal to $V_{ILA\ max}$ is reached. Clearly then, $V_{ILA\ max}$ is one critical point for noise margin computation, since it is the edge of the transition region.

To find the other critical voltage, consider the output from MECL gate #1 (point A). What is the most positive value possible for this voltage (considering worst case specifications)? From Figure 8 it can be observed that the $V_{OLA\ max}$ specification insures that the LOW state OR output from gate #1 can be no greater than $V_{OLA\ max}$.

Note that $V_{OLA\ max}$ is more negative than $V_{ILA\ max}$. Thus, with $V_{OLA\ max}$ at the input to gate #2, the transition region is not yet reached. (The input voltage to gate #2 is still to the left of $V_{ILA\ max}$ on the transfer curve.)

In order to ever run the chance of switching gate #2, we would need an additional voltage, to move the input from $V_{OLA\ max}$ to $V_{ILA\ max}$. This constitutes the "safety factor" known as noise margin. It can be calculated as the magnitude of the difference between the two specification voltages, or for the MECL 10K levels shown:

$NM_{LOW} = V_{ILA\ max} - V_{OLA\ max}$
$= -1.475\ V - (-1.630\ V)$
$= 155\ mV.$

Similarly, for the HIGH state:

$NM_{HIGH} = V_{OHA\ min} - V_{IHA\ min}$
$= -0.980\ V - (-1.105\ V)$
$= 125\ mV$

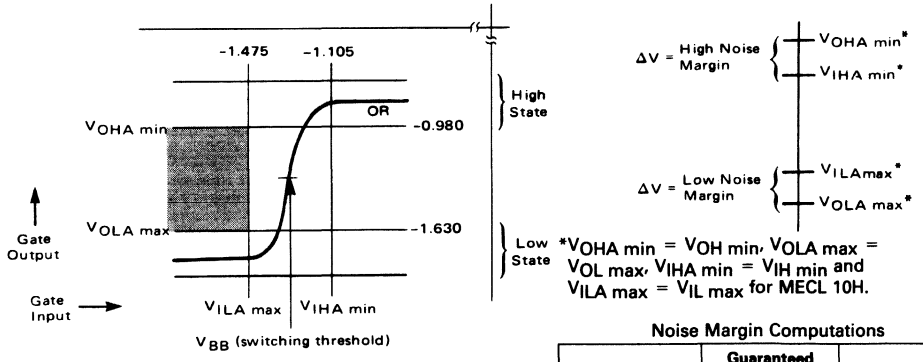
Analogous results are obtained when considering the "NOR" transfer data.

Note that these noise margins are absolute worst case conditions. The lessor of the two noise margins is that for the HIGH state, 125 mV. This then, constitutes the guaranteed margin against signal undershoot, and power or thermal disturbances.

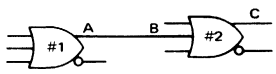
As shown in the table, typical noise margins are usually better than guaranteed — by about 75 mV. For MECL 10H the "noise margin" is 150 mV for NM low and NM high. (See Section 3 for details.)

Noise margin is a dc specification that can be calculated, since it is defined by specification points tabulated on MECL data sheets. However, by itself, this specification does not give a complete picture regarding the noise immunity of a system built with a particular set of circuits. Overall system noise immunity involves not only noise-margin specifications, but also other circuit-related factors that determine how difficult it is to apply a noise signal of sufficient magnitude and duration to cause the circuit to propagate a false logic state. In general, then, noise immunity involves line impedances, circuit output impedances, and propagation delay in addition to noise-margin specifications. This subject to discussed in greater detail in the MECL System Design Handbook, HB205.

FIGURE 8 — MECL Noise Margin Data



Specification Points for Determining Noise Margin



Noise Margin Computations

Family	Guaranteed Worst-Case dc Noise Margin (V)	Typical dc Noise Margin (V)
MECL 10H	0.150	0.270
MECL 10K	0.125	0.210
MECL III	0.115	0.200

AC OR SWITCHING PARAMETERS

Time-dependent specifications are those that define the effects of the circuit on a specified input signal, as it travels through the circuit. They include the time delay involved in changing the output level from one logic state to another. In addition, they include the time required for the output of a circuit to respond to the input signal, designated as propagation delay, MECL waveform and propagation delay terminologies are depicted in Figure 9. Specific rise, fall, and propagation delay times are given on the data sheet for each specific functional block, but like the transfer characteristics, ac parameters are temperature and voltage dependent. Typical variations for MECL 10K are given in the curves of Figure 10.

FIGURE 9 — TYPICAL LOGIC WAVEFORMS

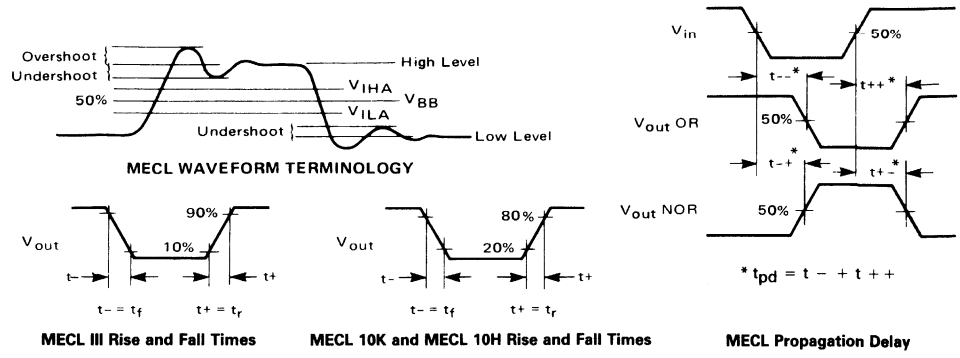


FIGURE 10a — TYPICAL PROPAGATION DELAY t- - versus V_{EE} AND TEMPERATURE (MECL 10K)

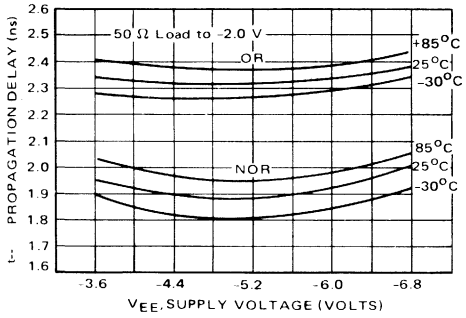


FIGURE 10b — TYPICAL PROPAGATION DELAY t+ + versus V_{EE} AND TEMPERATURE (MECL 10K)

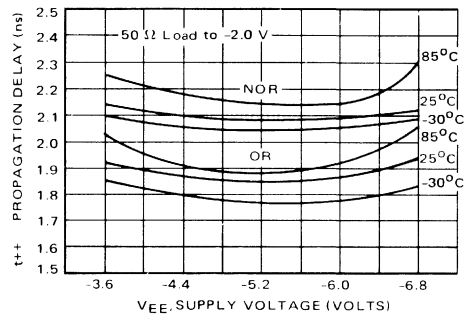


FIGURE 10c — TYPICAL FALL TIME (90% to 10%) versus TEMPERATURE AND SUPPLY VOLTAGE (MECL 10K)

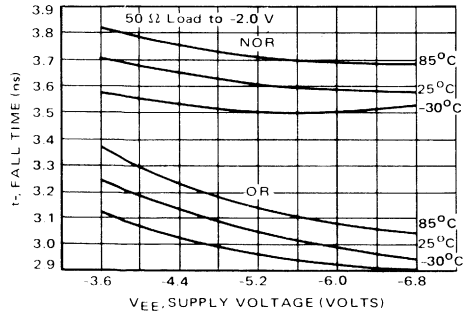
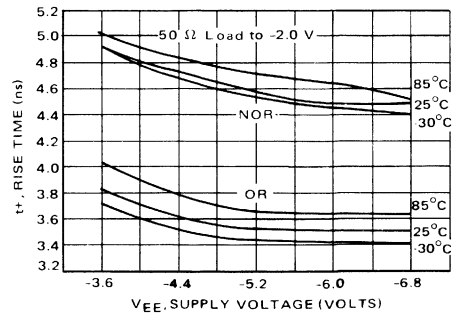


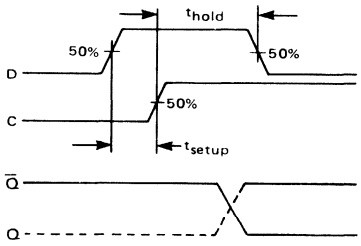
FIGURE 10d — TYPICAL RISE TIME (10% to 90%) versus TEMPERATURE AND SUPPLY VOLTAGE (MECL 10K)



SETUP AND HOLD TIMES

Setup and hold times are two ac parameters which can easily be confused unless clearly defined. For MECL logic devices, t_{setup} is the minimum time (50% – 50%) before the positive transition of the clock pulse (C) that information must be present at the Data input (D) to insure proper operation of the device. The t_{hold} is defined similarly as the minimum time after the positive transition of the clock pulse (C) that the information must remain unchanged at the Data input (D) to insure proper operation. Setup and hold waveforms for logic devices are shown in Figure 11.

FIGURE 11 — SETUP AND HOLD WAVEFORMS FOR MECL LOGIC DEVICES



TESTING MECL 10H, MECL 10K AND MECL III

To obtain results correlating with Motorola circuit specifications certain test techniques must be used. A schematic of a typical gate test circuit is shown in Figure 12.

This test circuit is the standard ac test configuration for most MECL devices. (Exceptions are shown with the device specification.)

A solid ground plane is used in the test setup, and capacitors bypass V_{CC1}, V_{CC2}, and V_{EE} pins to ground. All power leads and signal leads are kept as short as possible.

The sampling scope interface runs directly to the 50-ohm inputs of Channel A and B via 50-ohm coaxial cable. Equal-length coaxial cables must be used between the test set and the A and B scope inputs. A 50-ohm coax cable such as RG58/U or RG188A/U, is recommended.

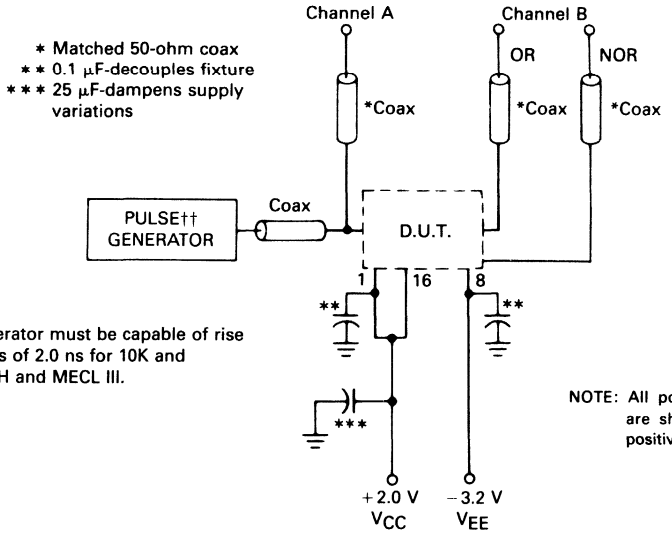
Interconnect fittings should be 50-ohm GR, BNC, Sealectro Conhex, or equivalent. Wire length should be $< \frac{1}{4}$ inch from TP_{in} to input pin and TP_{out} to output pin.

The pulse generator must be capable of 2.0 ns rise and fall times for MECL 10K and 1.5 ns for MECL 10H and MECL III. In addition, the generator voltage must have an offset to give MECL signal swings of $\approx \pm 400$ mV about a threshold of $\approx +0.7$ V when $V_{CC} = +2.0$ V and $V_{EE} = -3.2$ V for ac testing of logic devices.

The power supplies are shifted +2.0 V, so that the device under test has only one resistor value to load into the precision 50-ohm input impedance of the sampling oscilloscope. Use of this technique yields a close correlation between Motorola and customer testing. Unused outputs are loaded with a 50-ohm resistor (100-ohm for MC105XX devices) to ground. The positive supply (V_{CC}) should be decoupled from the test board by RF type 25 μF capacitors to ground. The V_{CC} pins are bypassed to ground with 0.1 μF, as is the V_{EE} pin.

Additional information on testing MECL 10K and understanding data sheets is found in Application Note AN701 and the MECL System Design Handbook, HB205.

FIGURE 12 — MECL LOGIC SWITCHING TIME TEST SETUP



SECTION III — OPERATIONAL DATA

POWER SUPPLY CONSIDERATIONS

MECL circuits are characterized with the V_{CC} point at ground potential and the V_{EE} point at −5.2 V. While this MECL convention is not necessarily mandatory, it does result in maximum noise immunity. This is so because any noise induced on the V_{EE} line is applied to the circuit as a common-mode signal which is rejected by the differential action of the MECL input circuit. Noise induced into the V_{CC} line is not cancelled out in this fashion. Hence, a good system ground at the V_{CC} bus is required for best noise immunity. Also, MECL 10H circuits may be operated with V_{EE} at −4.5 V with a negligible loss of noise immunity.

Power supply regulation which will achieve 10% regulation or better at the device level is recommended. The −5.2 V power supply potential will result in best circuit speed. Other values for V_{EE} may be used. A more negative voltage will increase noise margins at a cost of increased power dissipation. A less negative voltage will have just the opposite effect. (Noise margins and performance specifications of MECL 10H are unaffected by variations in V_{EE} because of the internal voltage regulation.)

On logic cards, a ground plane or ground bus system should be used. A bus system should be wide enough to prevent significant voltage drops between supply and device and to produce a low source inductance.

Although little power supply noise is generated by MECL logic, power supply bypass capacitors are recommended to handle switching currents caused by stray capacitance and asymmetric circuit loading. A parallel combination of a 1.0 μF and a 100 pF capacitor at the power entrance to the board, and a 0.01 μF low-inductance capacitor between ground and the −5.2 V line every four to six packages, are recommended.

Most MECL 10H, MECL 10K and MECL III circuits have two V_{CC} leads. V_{CC1} supplies current to the output transistors and V_{CC2} is connected to the circuit logic transistors. The separate V_{CC} pins reduce cross-coupling between individual circuits within a package when the outputs are driving heavy loads. Circuits with large drive capability, similar to the MC10110, have two V_{CC1} pins. All V_{CC} pins should be connected to the ground plane or ground bus as close to the package as possible.

For further discussion of MECL power supply considerations to be made in system designing, see MECL System Design Handbook, HB205.

POWER DISSIPATION

The power dissipation of MECL functional blocks is specified on their respective data sheets. This specification does not include power dissipated in the output devices due to output termination. The omission of internal output pulldown resistors permits the use of external terminations designed to yield best system performance. To obtain total operating power dissipation of a particular functional block in a system, the dissipation of the output transistor, under load, must be added to the circuit power dissipation.

The table in Figure 13 lists the power dissipation in the output transistors plus that in the external terminating resistors, for the more commonly used termination values and circuit configurations. To obtain true package power dissipation, one output-transistor power-dissipation value must be added to the specified package power dissipation for each external termination resistor used in conjunction with that package. To obtain system power dissipation, the stated dissipation in the external terminating resistors must be added as well. Unused outputs draw no power and may be ignored.

FIGURE 13 — AVERAGE POWER DISSIPATION IN OUTPUT CIRCUIT WITH EXTERNAL TERMINATING RESISTORS

Terminating Resistor Value	Output Transistor Power Dissipation (mW)	Terminating Resistor Power Dissipation (mW)
150 ohms to −2.0 Vdc	5.0	4.3
100 ohms to −2.0 Vdc	7.5	6.5
75 ohms to −2.0 Vdc	10	8.7
50 ohms to −2.0 Vdc	15	13
2.0 k ohms to V_{EE}	2.5	7.7
1.0 k ohm to V_{EE}	4.9	15.4
680 ohms to V_{EE}	7.2	22.6
510 ohms to V_{EE}	9.7	30.2
270 ohms to V_{EE}	18.3	57.2
82 ohms to V_{CC} and 130 ohms to V_{EE}	15	140

LOADING CHARACTERISTICS

The differential input to MECL circuits offers several advantages. Its common-mode-rejection feature offers immunity against power-supply noise injection, and its relatively high input impedance makes it possible for any circuit to drive a relatively large number of inputs without deterioration of the guaranteed noise margin. Hence, dc fanout with MECL circuits does not normally present a design problem.

Graphs showing typical output voltage levels as a function of load current for MECL 10H, MECL 10K and MECL III shown in Figure 14. These graphs can be used to determine the actual output voltages for loads exceeding normal operation.

While dc loading causes a change in output voltage levels, thereby tending to affect noise margins, ac loading increases the capacitances associated with the circuit and, therefore, affects circuit speed, primarily rise and fall times.

MECL circuits typically have a 7 ohm output impedance and a relatively unaffected by capacitive loading on a positive-going output signal. However, the negative-going edge is dependent on the output pulldown or termination resistor. Loading close to a MECL output pin will cause an additional propagation delay of 0.1 ns per fanout load with a 50 ohm resistor to −2.0 Vdc or 270 ohms to −5.2 Vdc. A 100 ohm resistor to −2.0 Vdc or

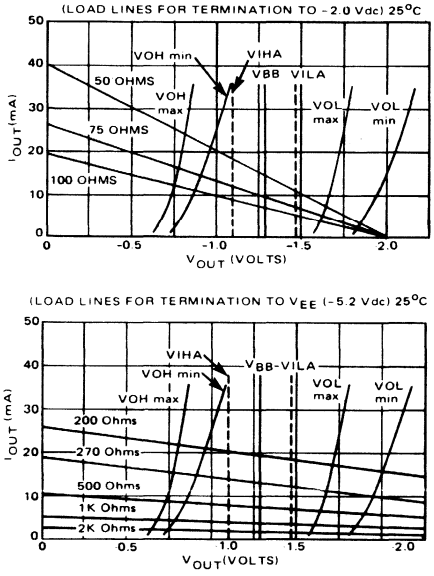
510 ohms to −5.2 Vdc results in an additional 0.2 ns propagation delay per fanout load.

Terminated transmission line signal interconnections are used for best system performance. The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel-terminated transmission line. However, the delay and characteristic impedance of the transmission line itself are affected by the distributed capacitance. Signal propagation down the line will be increased by a factor, $\sqrt{1+C_d/C_o}$. Here C_o is the normal intrinsic line capacitance, and C_d is the distributed capacitance due to loading and stubs off the line.

Maximum allowable stub lengths for loading off of a MECL 10K transmission line vary with the line impedance. For example, with Z_o = 50 ohms, maximum stub length would be 4.5 inches (1.8 in. for MECL III). But when Z_o = 100 ohms, the maximum allowable stub length is decreased to 2.8 inches (1.0 in. for MECL III).

The input loading capacitance of a MECL 10H and MECL 10K gate is about 2.9 pF and 3.3 pF for MECL III. To allow for the IC connector or solder connection and a short stub length, 5 to 7 pF is commonly used in loading calculations.

FIGURE 14 — OUTPUT VOLTAGE LEVELS versus DC LOADING



UNUSED MECL INPUTS

The input impedance of a differential amplifier, as used in the typical MECL input circuit, is very high when the applied signal level is low. Under low-signal conditions, therefore, any leakage to the input capacitance of the gate could cause a gradual buildup of voltage on the input lead, thereby adversely affecting the switching characteristics at low repetition rates.

All single-ended input MECL logic circuits contain input pulldown resistors between the input transistor bases and V_{EE}. As a result, unused inputs may be left unconnected (the resistor provides a sink for I_{CBO} leakage currents, and inputs are held sufficiently negative that circuits will not trigger due to noise coupled into such inputs). Input pulldown resistor values are typically 50 kΩ and are not to be used as pulldown resistors for preceding open-emitter outputs.

Some MECL devices do not have input pulldowns. Examples are the differential line receivers. If a single differential receiver within a package is unused, one input of that receiver must be tied to the V_{BB} pin provided, and the other input goes to V_{EE} or is left open.

MECL circuits do not operate properly when inputs are connected to V_{CC} for a HIGH logic level. Proper design practice is to set a HIGH level as about −0.9 volts below V_{CC} with a resistor divider, a diode drop, or an unused gate output.

SECTION IV — SYSTEM DESIGN CONSIDERATIONS

THERMAL MANAGEMENT

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit — from the junction region to the ambient environment. The basic formula (a) for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\bar{\theta}_{JC} + \bar{\theta}_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D(\bar{\theta}_{JA}) \quad (2)$$

where

T_J = maximum junction temperature
T_A = maximum ambient temperature
P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III).

$\bar{\theta}_{JC}$ = average thermal resistance, junction to case
$\bar{\theta}_{CA}$ = average thermal resistance, case to ambient
$\bar{\theta}_{JA}$ = average thermal resistance, junction to ambient

This Motorola recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL-M-38510 (JAN) MECL 10K devices.

Only two terms on the right side of equation (1) can be varied by the user — the ambient temperature, and the device case-to-ambient thermal resistance, $\bar{\theta}_{CA}$. (To some extent the device power dissipation can be also controlled, but under recommended use the V_{EE} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\bar{\theta}_{CA}$ thermal resistance term. $\bar{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

FIGURE 15 — THERMAL RESISTANCE VALUES FOR STANDARD MECL I/C PACKAGES

Thermal Resistance in Still Air										
Package Description							θ_{JA} (°C/Watt)		θ_{JC} (°C/Watt)	
No. Leads	Body Style	Body Material	Body WxL	Die Bond	Die Area (Sq. Mils)	Flag Area (Sq. Mils)	Avg.	Max.	Avg.	Max.
8	DIL	EPOXY	1/4"x3/8"	EPOXY	2496	8100	102	133	50	80
8	DIL	ALUMINA	1/4"x3/8"	SILVER/GLASS	2496	N/A	140	182	35	56
14	FLAT	ALUMINA	1/4"x1/4"	SILVER/GLASS	4096	N/A	165	215	28	45
14	DIL	EPOXY	1/4"x3/4"	EPOXY	4096	6400	84	109	38	61
14	DIL	ALUMINA	1/4"x3/4"	SILVER/GLASS	4096	N/A	100	130	25	40
16	FLAT	ALUMINA	1/4"x3/8"	SILVER/GLASS	4096	N/A	140	182	24	38
16	DIL	EPOXY	1/4"x3/4"	EPOXY	4096	12100	70	91	34	54
16	DIL	ALUMINA	1/4"x3/4"	SILVER/GLASS	4096	N/A	100	130	25	40
20	PLCC	EPOXY	0.35"x0.35"	EPOXY	4096	14,400	74	82	N/A (6)	N/A (6)
24	FLAT	ALUMINA	3/8"x5/8"	SILVER/GLASS	8192	N/A	64	83	11	18
24	DIL (4)	EPOXY	1/2"x1-1/4"	EPOXY	8192	22500	67	87	31	50
24	DIL (5)	ALUMINA	1/2"x1-1/4"	SILVER/GLASS	8192	N/A	50	65	10	16
28	PLCC	EPOXY	0.45"x0.45"	EPOXY	7134	28,900	65	68	N/A (6)	N/A (6)

NOTES:
1. All plastic packages use copper lead frames — ceramic packages use alloy 42 frames.
2. Body style DIL is "Dual-In-Line."
3. Standard Mounting Methods:
   a. Dual-In-Line In Socket or P/C board with no contact between bottom of package and socket or P/C board.
   b. Flat Pack — Bottom of package in direct contact with non-metallized area of P/C board.
   c. PLCC packages solder attached to traces on 2.24" x 2.24" x 0.062" FR4 type glass epoxy board with 1 oz./S.F. copper (solder coated) mounted to tester with 3 leads of 24 gauge copper wire.
4. Case Outline 649
5. Case Outline 623
6. $\theta_{JC} = \theta_{JA} - \left(\frac{T_C - T_A}{P_D}\right)$

   T_C = Case Temperature (determined by thermocouple)

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature-controlled heatsink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D (\bar{\theta}_{JC}) \quad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average thermal resistance values for standard MECL IC packages are given in Figure 15. In Figure 16, this basic data is converted into graphs showing the maximum power dissipation allowable at various ambient temperatures (still air) for circuits mounted in the different packages, taking into account the maximum permissible operating junction temperature for long term life (≥ 100,000 hours for ceramic packages).

AIR FLOW

The effect of air flow over the packages on $\bar{\theta}_{JA}$ (due to a decrease in $\bar{\theta}_{CA}$) is illustrated in the graphs of Figure 17. This air flow reduces the thermal resistance of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

As an example of the use of the information above, the maximum junction temperature for a 16 lead ceramic dual-in-line packaged MECL 10K quad OR/NOR gate (MC10101L) loaded with four 50 ohm loads can be calculated. Maximum total power dissipation (including 4 output loads) for this quad gate is 195 mW. Assume for this thermal study that air flow is 500 linear feet per minute. From Figure 17, $\bar{\theta}_{JA}$ is 50°C/W. With T_A (air flow temperature at the device) equal to 25°C, the following maximum junction temperature results:

$$T_J = P_D (\bar{\theta}_{JA}) + T_A$$
$$T_J = (0.195\ W)\ (50°C/W) + 25°C = 34.8°C$$

Under the above operating conditions, the MECL 10K quad gate has its junction elevated above ambient temperature by only 9.8°C.

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over the devices, or differences in ambient temperature between two devices.

FIGURE 16A — AMBIENT TEMPERATURE DERATING CURVES (CERAMIC DUAL-IN-LINE PACKAGE)

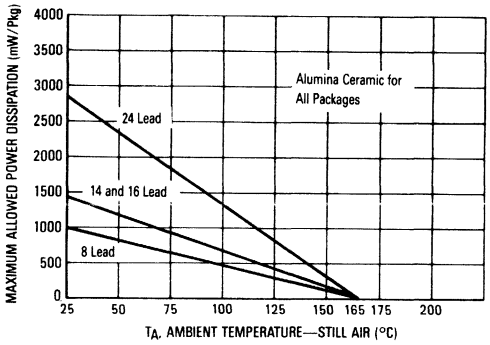


FIGURE 16B — AMBIENT TEMPERATURE DERATING CURVES (CERAMIC FLAT PACKAGE)

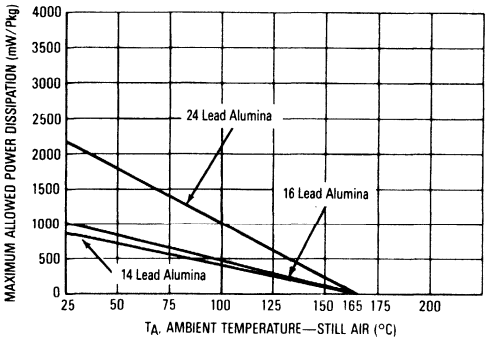


FIGURE 17A — AIRFLOW versus THERMAL RESISTANCE (CERAMIC DUAL-IN-LINE PACKAGE)

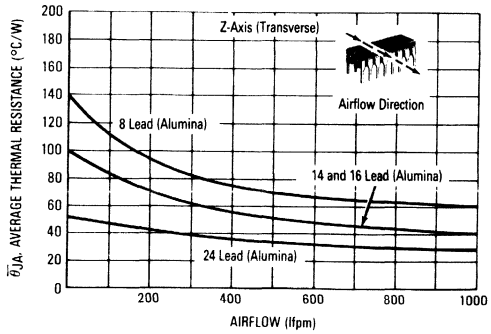


FIGURE 17B — AIRFLOW versus THERMAL RESISTANCE (CERAMIC FLAT PACKAGE)

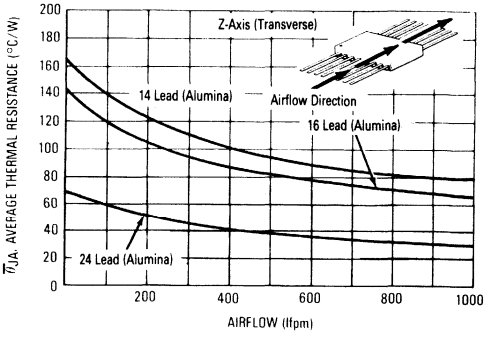


FIGURE 16C — AMBIENT TEMPERATURE DERATING CURVES (PLASTIC DUAL-IN-LINE PACKAGE)

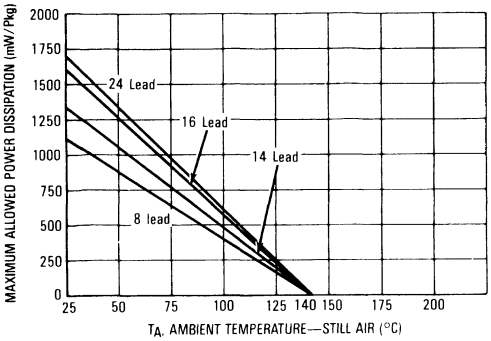


FIGURE 16D — AMBIENT TEMPERATURE DERATING CURVES (PLCC PACKAGE)

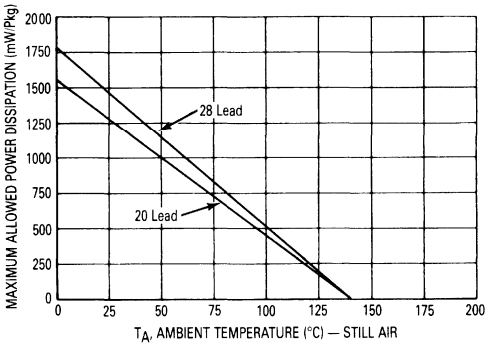


FIGURE 17C — AIRFLOW versus THERMAL RESISTANCE (PLASTIC DUAL-IN-LINE PACKAGE)

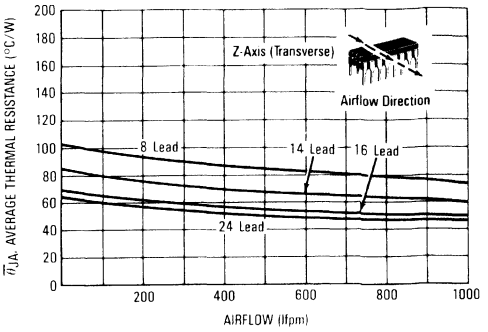


FIGURE 17D — AIRFLOW versus THERMAL RESISTANCE (PLCC PACKAGE)

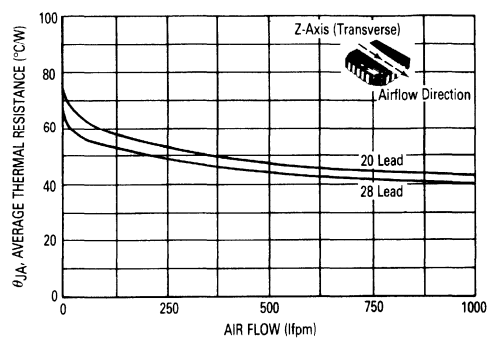


FIGURE 18 — THERMAL GRADIENT OF JUNCTION TEMPERATURE (16-Pin MECL Dual-In-Line Package)

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062" PC board with Z axis spacing of 0.5". Air flow is 500 lfpm along the Z axis.

The majority of MECL 10H, MECL 10K, and MECL III users employ some form of air-flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations. Figure 18 provides gradient data at power levels of 200 mW, 250 mW, 300 mW, and 400 mW with an air flow rate of 500 lfpm. These figures show the proportionate increase in the junction temperature of each dual-in-line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

OPTIMIZING THE LONG TERM RELIABILITY OF PLASTIC PACKAGES

Todays plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However when the ultimate in system reliability is required, thermal management must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperatures are consistent with system reliability goals.

Predicting Bond Failure Time:

Based on the results of almost ten (10) years of +125°C operating life testing, a special arrhenius equation has been developed to show the relationship between junction temperature and reliability.

$$(1)\ T = (6.376 \times 10^{-9})e\left[\frac{11554.267}{273.15 + T_J}\right]$$

Where: T = Time in hours to 0.1% bond failure (1 failure per 1,000 bonds).
T_J = Device junction temperature, °C.

And:

$$(2)\ T_J = T_A + P_D\theta J_A = T_A + \Delta T_J$$

Where: T_J = Device junction temperature, °C.
T_A = Ambient temperature, °C.
P_D = Device power dissipation in watts.
θJ_A = Device thermal resistance, junction to air, °C/Watt.
ΔT_J = Increase in junction temperature due to on-chip power dissipation.

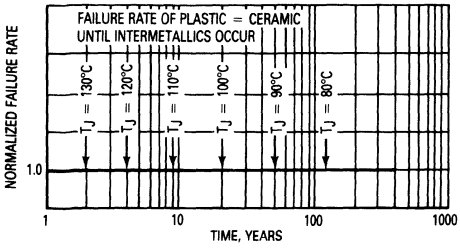
Table 1 shows the relationship between junction temperature, and continuous operating time to 0.1% bond failure, (1 failure per 1,000 bonds).

TABLE 4 — DEVICE JUNCTION TEMPERATURE versus TIME TO 0.1% BOND FAILURES.

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Table 4 is graphically illustrated in Figure 19 which shows that the reliability for plastic and ceramic devices are the same until elevated junction temperatures induces intermetallic failures in plastic devices. Early and mid-life failure rates of plastic devices are not effected by this intermetallic mechanism.

FIGURE 19. FAILURE RATE versus TIME JUNCTION TEMPERATURE



MECL Junction Temperatures:

Power levels have been calculated for a number of MECL 10K and MECL 10H devices in 20 pin plastic leaded chip carriers and translated to the resulting increase of junction temperature (ΔT_J) for still air and moving air at 500 LFPM using equation 2 and are shown in Table 5.

TABLE 5 — INCREASE IN JUNCTION TEMPERATURE DUE TO I/C POWER DISSIPATION. 20 PIN PLASTIC LEADED CHIP CARRIER

MECL 10K Device Type	ΔT_J,°C Still Air	ΔT_J,°C 500 LFPM Air	MECL 10H Device Type	ΔT_J,°C Still Air	ΔT_J,°C 500 LFPM Air
MC10100	16.2	10.5	MC10H016	48.0	30.0
MC10101	21.8	14.1	MC10H100	16.6	10.8
MC10102	17.6	11.4	MC10H101	22.1	14.5
MC10103	17.6	11.4	MC10H102	18.0	11.8
MC10104	20.8	13.4	MC10H103	18.0	11.8
MC10105	17.2	11.2	MC10H104	21.0	13.5
MC10106	13.0	8.4	MC10H105	17.8	11.7
MC10107	19.8	12.8	MC10H106	13.2	8.7
MC10109	11.7	7.7	MC10H107	20.0	12.9
MC10110	24.7	16.1	MC10H109	11.9	7.8
MC10111	24.7	16.1	MC10H113	22.8	14.8
MC10113	22.2	14.3	MC10H115	16.7	10.9
MC10114	22.6	14.6	MC10H116	17.8	11.7
MC10115	16.7	10.9	MC10H117	16.7	11.0
MC10116	17.2	11.1	MC10H118	13.8	9.0
MC10117	16.2	10.5	MC10H119	12.5	8.2
MC10118	13.4	8.7	MC10H121	13.9	9.1
MC10119	12.1	7.8	MC10H123	23.1	15.0
MC10121	13.5	8.5	MC10H124	44.2	28.4
MC10123	37.6	24.0	MC10H125	—	—
MC10124	42.9	27.3	MC10H130	19.7	12.7
MC10125	—	—	MC10H131	28.2	18.2
MC10130	19.6	12.6	MC10H135	33.2	21.4
MC10131	26.9	17.1	MC10H136	61.7	38.5
MC10133	34.4	21.9	MC10H141	44.3	28.0
MC10134	27.0	17.2	MC10H145	59.4	36.9
MC10135	31.9	20.3	MC10H158	25.3	16.4
MC10136	52.3	32.6	MC10H159	27.3	177
MC10138	37.0	23.2	MC10H160	32.1	20.5
MC10141	42.7	26.7	MC10H161	41.5	26.7
MC10153	34.4	21.9	MC10H162	41.5	26.7
MC10158	23.9	15.2	MC10H164	31.9	20.6
MC10159	25.8	16.4	MC10H165	56.3	35.8
MC10160	32.0	20.4	MC10H166	44.4	28.3
MC10161	40.7	26.0	MC10H171	41.9	26.9
MC10162	40.7	26.0	MC10H172	41.9	26.9
MC10164	31.3	20.1	MC10H173	32.6	21.1
MC10165	53.7	33.6	MC10H174	32.5	21.0
MC10166	43.5	27.6	MC10H175	45.9	29.6
MC10168	34.4	21.9	MC10H176	50.9	32.3
MC10170	29.9	18.9	MC10H179	35.0	22.6
MC10171	41.1	26.2	MC10H180	42.4	27.2
MC10172	41.1	26.2	MC10H181[4]	64.4	38.6
MC10173	30.5	19.3	MC10H186	50.2	31.8
MC10174	31.9	20.5	MC10H188	25.8	16.7
MC10175	43.7	27.6	MC10H189	25.8	16.7
MC10176	49.6	31.3	MC10H209	18.9	12.5
MC10178	38.1	23.9	MC10H210	25.0	16.4
MC10186	49.6	31.1	MC10H211	25.0	16.4
MC10188	25.4	16.4	MC10H330[4]	65.8	36.1
MC10189	24.6	15.9	MC10H332	52.2	33.5
MC10190	25.5	16.2	MC10H334	77.8	49.3
MC10192	67.0	43.0	MC10H350	—	—
MC10195	46.7	29.9	MC10H423	31.3	20.3
MC10197	27.7	17.7	MC10H424	37.7	24.3
MC10198	21.2	13.4			
MC10210	24.5	16.0			
MC10211	24.6	16.0			
MC10212	24.3	15.8			
MC10216	24.1	15.6			
MC10231	30.6	19.5			

NOTES:
(1) All ECL outputs are loaded with a 50 Ω resistor and assumed operating at 50% duty cycle.
(2) ΔT_J for ECL to TTL translators are excluded since the supply current to the TTL section is dependent on frequency, duty cycle and loading.
(3) Thermal Resistance (θ_{JA}) measured with PLCC packages solder attached to traces on 2.24" x 2.24" x 0.062" FR4 type glass epoxy board with 1 oz./sq. ft. copper (solder-coated) mounted to tester with 3 leads of 24 gauge copper wire.
(4) 28 lead PLCC.

Case Example:

After the desired system failure rate has been established for failure mechanisms other than intermetallics, each plastic device in the system should be evaluated for maximum junction temperature using Table 5. Knowing the maximum junction temperature refer to Table 4 or Equation 1 to determine the continuous operating time required to 0.1% bond failures due to intermetallic formation. At this time, system reliability departs from the desired value as indicated in Figure 19.

To illustrate, assume that system ambient air temperature is 55°C (an accepted industry standard for evaluating system failure rates). Reference is made to Table 5 to determine the maximum junction temperature for each device for still air and transverse air flow of 500 LFPM.

Adding the 55°C ambient to the highest ΔT_J listed, 77.8°C (for the MC10H334 with no air flow), gives a maximum junction temperature of 132.8°C. Reference to Table 4 indicates a departure from the desired failure rate after about 2 years of constant exposure to this junction temperature. If 500 LFPM of air flow is utilized, maximum junction temperature for this device is reduced to 104.3°C for which Table 4 indicates an increased failure rate in about 15 years.

Air flow is one method of thermal management which should be considered for system longevity. Other commonly used methods include heat sinks for higher powered devices, refrigerated air flow and lower density board stuffing.

The material presented here emphasizes the need to consider thermal management as an integral part of system design and also the tools to determine if the management methods being considered are adequate to produce the desired system reliability.

THERMAL EFFECTS ON NOISE MARGIN

The data sheet dc specifications for standard MECL 10K and MECL III devices are given for an operating temperature range from −30°C to +85°C (0° to +75°C for MECL 10H and memories). These values are based on having an airflow of 500 lfpm over socket or P/C board mounted packages with no special heatsinking (i.e., dual-in-line package mounted on lead seating plane with no contact between bottom of package and socket or P/C board and flat package mounted with bottom in direct contact with non-metallized area of P/C board).

The designer may want to use MECL devices under conditions other than those given above. The majority of the low-power device types may be used without air and with higher θ_{JA}. However, the designer must bear in mind that junction temperatures will be higher for higher θ_{JA}, even though the ambient temperature is the same. Higher junction temperatures will cause logic levels to shift.

As an example, a 300 mW 16 lead dual-in-line ceramic device operated at θ_{JA} = 100°C/W (in still air) shows a HIGH logic level shift of about 21 mV above the HIGH logic level when operated with 500 lfpm air flow and a θ_{JA} = 50°C/W. (Level shift = ΔT_J x 1.4 mV/°C).

If logic levels of individual devices shift by different amounts (depending on P_D and θ_{JA}), noise margins are somewhat reduced. Therefore, the system designer must lay out his system bearing in mind that the mounting procedures to be used should minimize thermal effects on noise margin.

The following sections on package mounting and heatsinking are intended to provide the designer with sufficient information to insure good noise margins and high reliability in MECL system use.

MOUNTING AND HEATSINK SUGGESTIONS

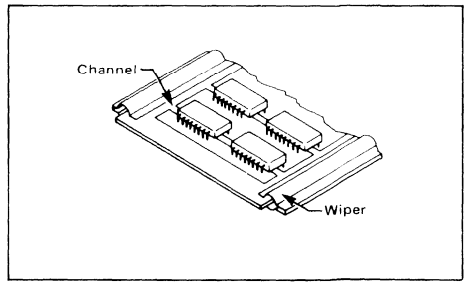
With large high-speed logic systems, the use of multilayer printed circuit boards is recommended to provide both a better ground plane and a good thermal path for heat dissipation. Also, a multilayer board allows the use of microstrip line techniques to provide transmission line interconnections.

Two-sided printed circuit boards may be used where board dimensions and package count are small. If possible, the V_{CC} ground plane should face the bottom of the package to form the thermal conduction plane. If signal lines must be placed on both sides of the board, the V_{EE} plane may be used as the thermal plane, and at the same time may be used as a pseudo ground plane. The pseudo ground plane becomes the ac ground reference under the signal lines placed on the same side as the V_{CC} ground plane (now on the opposite side of the board from the packages), thus maintaining a microstrip signal line environment.

Two-ounce copper P/C board is recommended for thermal conduction and mechanical strength. Also, mounting holes for low power devices may be countersunk to allow the package bottom to contact the heat plane. This technique used along with thermal paste will provide good thermal conduction.

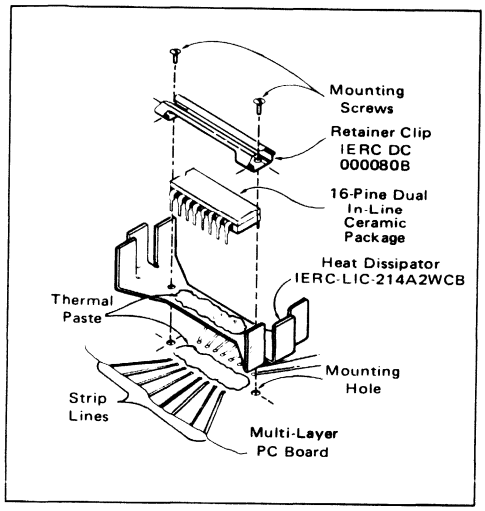
Printed channeling is a useful technique for conduction of heat away from the packages when the devices are soldered into a printed circuit board. As illustrated in Figure 20, this heat dissipation method could also serve as V_{EE} voltage distribution or as a ground bus. The channels should terminate into channel strips at each side or the rear of a plug-in type printed circuit board. The heat can then be removed from the circuit board, or board slide rack, by means of wipers that come into thermal contact with the edge channels.

FIGURE 20 — CHANNEL/WIPER HEATSINKING ON DOUBLE LAYER BOARD



For operating some of the higher power device types* in 16 lead dual-in-line packages in still air, requiring θ_{JA} <100°C/W, a suitable heatsink is the IERC LIC-214A2WCB shown in Figure 21. This sink reduces the still air θ_{JA} to around 55°C/W. By mounting this heatsink directly on a copper ground plane (using silicone paste) and passing 500 lfpm air over the packages, θ_{JA} is reduced to approximately 35°C/W, permitting use at higher ambient temperatures than +85°C (+75°C for MECL 10H memories) or in lowering T_J for improved reliability.

FIGURE 21 — MECL HIGH-POWER DUAL-IN-LINE PACKAGE MOUNTING METHOD



It should be noted that the use of a heatsink on the top surface of the dual-in-line package is not very effective in lowering the θ_{JA}. This is due to the location of the die near the bottom surface of the package. Also, very little (< 10%) of the internal heat is withdrawn through the package leads due to the isolation from the ceramic by the solder glass seals and the limited heat conduction from the die through 1.0 to 1.5 mil aluminum bonding wires.

INTERFACING MECL TO SLOWER LOGIC TYPES

MECL circuits are interfaceable with most other logic forms. For MECL/TTL/DTL interfaces, when MECL is operated at the recommended −5.2 volts and TTL/DTL at +5.0 V supply, currently available translator circuits, such as the MC10124 and MC10125, may be used.

For systems where a dual supply (−5.2 V and +5 V) is not practical, the MC10H350 includes four single supply MECL to TTL translators, or a discrete component translator can be designed. For details, see MECL System Design Handbook (HB205). Such circuits can easily be made fast enough for any available TTL.

MECL also interfaces readily with MOS. With CMOS operating at +5 V, any of the MECL to TTL translators works very well.

Specific circuitry for use in interfacing MECL families to other logic types is given in detail in the MECL System Design Handbook.

Complex MECL 10K devices are presently available for interfacing MECL with MOS logic, MOS memories, TTL three-state circuits, and IBM bus logic levels. See Application Note AN-720 for additional interfacing information.

CIRCUIT INTERCONNECTIONS

Though not necessarily essential, the use of multilayer printed circuit boards offers a number of advantages in the development of high-speed logic cards. Not only do multilayer boards achieve a much higher package density, interconnecting leads are kept shorter, thus minimizing propagation delay between packages. This is particularly beneficial with MECL III which has relatively fast (1 ns) rise and fall times. Moreover, the unbroken ground planes made possible with multilayer boards permit much more precise control of transmission line impedances when these are used for interconnecting purposes. Thus multilayer boards are recommended for MECL III layouts and are justified when operating MECL 10H and MECL 10K at top circuit speed, when high-density packaging is a requirement, or when transmission line interconnects are used.

Point-to-point back-plane wiring without matched line terminations may be employed for MECL interconnections if line runs are kept short. At MECL 10K speeds, this applies to line runs up to 6 inches, for MECL 10H and MECL III up to 1 inch (Maximum open wire lengths for less than 100 mV undershoot). But, because of the open-emitter outputs of MECL 10H, MECL 10K and MECL III circuits, pull-down resistors are always required. Several ways of connecting such pull-down resistors are shown in Figure 22.

Resistor values for the connection in Figure 22a may range from 270 ohms to kΩ depending on power and load requirements. (See MECL System Design Handbook.) Power may be saved by connecting pull-down resistors in the range of 50 ohms to 150 ohms, to −2.0 Vdc, as shown in Figure 22b. Use of a series damping resistor, Figure 22c, will extend permissible lengths of unmatched-impedance interconnections, with some loss of edge speed.

With proper choice of the series damping resistor, line lengths can be extended to any length,** while limiting overshoot and undershoot to a predetermined amount. Damping resistors usually range in value from 10 ohms to 100 ohms, depending on the line length, fanout, and line impedance, the open emitter-follower outputs of MECL 10H, MECL III and MECL 10K give the system designer all possible line driving options.

One major advantage of MECL over saturated logic is its capability for driving matched-impedance transmission lines. Use of transmission lines retains signal integrity over long distances. The MECL 10H and MECL 10K emitter-follower output transistors will drive a 50-ohm transmission line terminated to −2.0 Vdc. This is the equivalent current load of 22 mA in the HIGH logic state and 6 mA in the LOW state.

* 10128, 10129, 10136, 10H136, 10137, 10177, 10182, and 10804, Max P_D > 800 mW.

** Limited only by line attenuation and band-width characteristics.

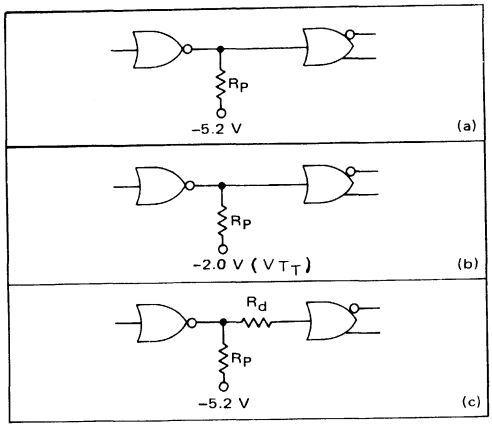
Parallel termination of transmission lines can be done in two ways. One, as shown in Figure 23a, uses a single resistor whose value is equal to the impedance (Z_o) of the line. A terminating voltage (V_{TT}) of −2.0 Vdc must be supplied to the terminating resistor.

Another method of parallel termination uses a pair of resistors, R1 and R2. Figure 23b illustrates this method. The following two equations are used to calculate the values of R1 and R2:

$$R1 = 1.6\ Z_o$$
$$R2 = 2.6\ Z_o$$

Another popular approach is the series-terminated transmission line (see Figure 23). This differs from parallel termination in that only one-half the logic swing is propagated through the lines. The logic swing doubles at the end of the transmission line due to reflection on an open line, again establishing a full logic swing.

FIGURE 22 — PULL-DOWN RESISTOR TECHNIQUES



To maintain clean wave fronts, the input impedance of the driven gate must be much greater than the characteristic impedance of the transmission line. This condition is satisfied by MECL circuits which have high impedance inputs. Using the appropriate terminating resistor (R_S) at point A (Figure 24), the reflections in the transmission line will be terminated.

FIGURE 23a — PARALLEL TERMINATED LINE

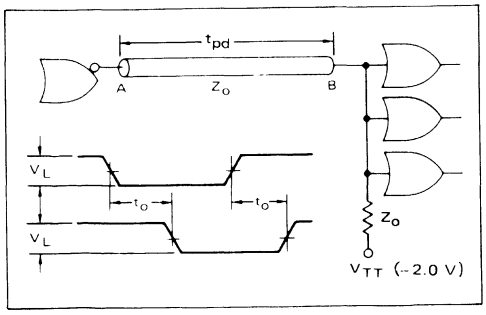


FIGURE 23b — PARALLEL TERMINATION — THEVENIN EQUIVALENT

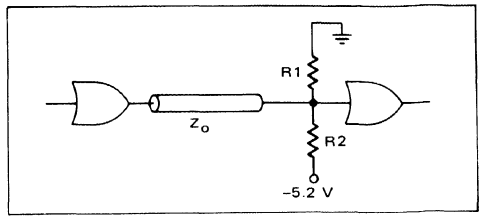
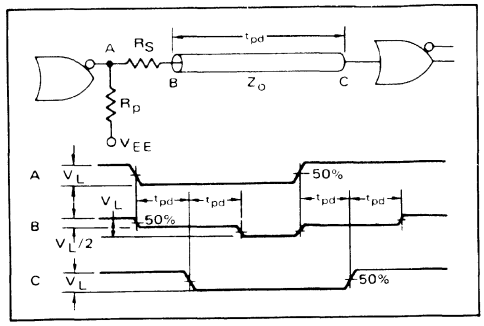


FIGURE 24 — SERIES TERMINATED LINE



The advantages of series termination include ease of driving multiple series-terminated lines, low power consumption, and low cross talk between adjacent lines. The disadvantage of this system is that loads may not be distributed along the transmission line due to the one-half logic swing present at intermediate points.

For board-to-board interconnections, coaxial cable may be used for signal conductors. The termination techniques just discussed also apply when using coax. Coaxial cable has the advantages of good noise immunity and low attenuation at high frequencies.

Twisted pair lines are one of the most popular methods of interconnecting cards or panels. The complementary outputs of any MECL function may be connected to one end of the twisted pair line, and any MECL differential line receiver to the other as shown in the example, Figure 25. R_T is used to terminate the twisted pair line. The 1 to 1.5 V common-mode noise rejection of the line receiver ignores common-mode cross talk, permitting multiple twisted pair lines to be tied into cables. MECL signals may be sent very long distances (> 1000 feet) on twisted pair, although line attenuation will limit bandwidth, degrading edge speeds when long line runs are made.

If timing is critical, parallel signals paths (shown in Figure 26) should be used when fanout to several cards is required. This will eliminate distortion caused by long stub lengths off a signal path.

Wire-wrapped connections can be used with MECL 10K. For MECL III and MECL 10H, the fast edge speeds (1 ns) create a mismatch at the wire-wrap connections which can cause reflections, thus reducing noise immunity. The mismatch occurs also with MECL 10K, but the distance between the wire-wrap connections and the end of the line is generally short enough so the reflections cause no problem.

Series damping resistors may be used with wire-wrapped lines to extend permissible backplane wiring lengths. Twisted pair lines may be used for even longer distances across large wire-wrapped cards. The twisted pair gives a more defined characteristic impedance (than a single wire), and can be connected either single-ended, or differentially using a line receiver.

The recommended wire-wrapped circuit cards have a ground plane on one side and a voltage plane on the other side to insure a good ground and a stable voltage source for the circuits. In addition, the ground plane near the wire-wrapped lines lowers the impedance of those lines and facilitates terminating the line. Finally, the ground plane serves to minimize cross talk between parallel paths in the signal lines. Point-to-point wire routing is recommended because cross talk will be minimized and line lengths will be shortest. Commercial wire-wrap boards designed for MECL 10K are available from several vendors.

FIGURE 25 — TWISTED PAIR LINE DRIVER/RECEIVER

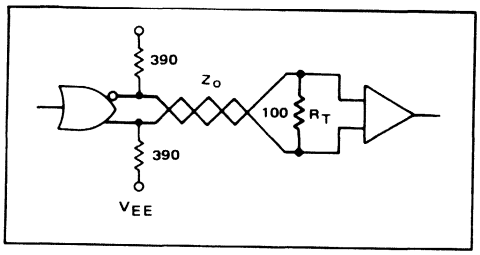
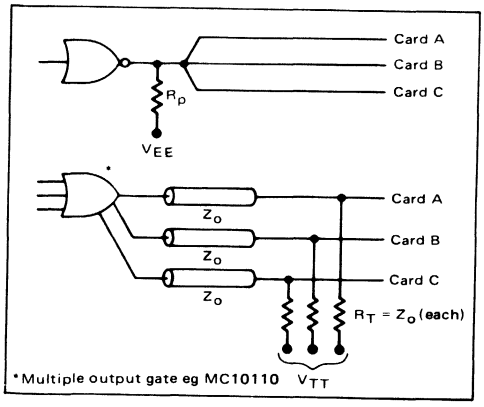


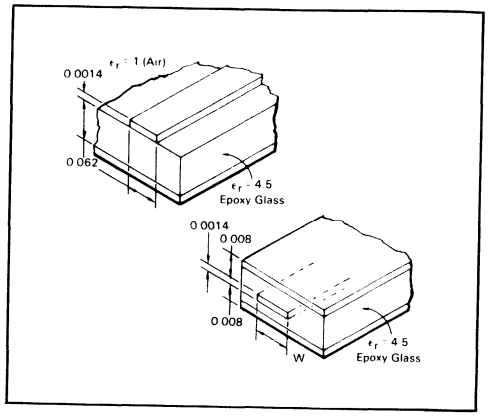
FIGURE 26 — PARALLEL FANOUT TECHNIQUES



Microstrip and Stripline

Microstrip and stripline techniques are used with printed circuit boards to form transmission lines. Microstrip consists of a constant-width conductor on one side of a circuit board, with a ground plane on the other side (shown in Figure 27). The characteristic impedance is determined by the width and thickness of the conductor, the thickness of the circuit board, and the dielectric constant of the circuit board material.

FIGURE 27 — PC INTERCONNECTION LINES FOR USE WITH MECL



Stripline is used with multilayer circuit boards as shown in Figure 27. Stripline consists of a constant-width conductor between two ground planes.

Refer to MECL System Design Handbook for a full discussion of the properties and use of these.

CLOCK DISTRIBUTION

Clock distribution can be a system problem. At MECL 10K speeds, either coaxial cable or twisted pair line (using the MC10101 and MC10115) can be used to distribute clock signals throughout a system. Clock line lengths should be controlled and matched when timing could be critical. Once the clocking signals arrive on card, a tree distribution should be used for large-fanouts at high frequency. An example of the application of the technique is shown in Figure 28.

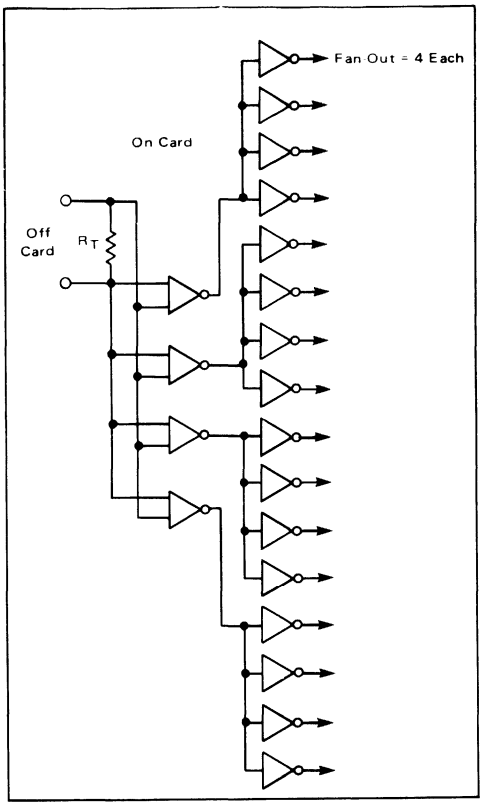
Because of the very high clock rates encountered in MECL III systems, rules for clocking are more rigorous than in slower systems.

The following guidelines should be followed for best results:

A. On-card Synchronous Clock Distribution via Transmission Line

1. Use the NOR output in developing clock chains or trees. Do not mix OR and NOR outputs in the chain.
2. Use balanced fanouts on the clock drivers.
3. Overshoot can be reduced by using two parallel drive lines in place of one drive line with twice the lumped load.

FIGURE 28 — 64 FANOUT CLOCK DISTRIBUTION
(PROPER TERMINATION REQUIRED)



4. To minimize clock skewing problems on synchronous sections of the system, line delays should be matched to within 1 ns.

5. Parallel drive gates should be used when clocking repetition rates are high, or when high capacitance loads occur. The bandwidth of a MECL III gate may be extended by paralleling both halves of a dual gate. Approximately 40 or 50 MHz bandwidth can be gained by paralleling two or three clock driver gates.

6. Fanout limits should be applied to clock distribution drivers. Four to six loads should be the maximum load per driver for best high speed performance. Avoid large lumped loads at the end of lines greater than 3 inches. A lumped load, if used, should be four or fewer loads.

7. For wire-OR (emitter dotting), two-way lines (busses) are recommended. To produce such lines, both ends of a transmission line are terminated with 100-ohms impedance. This method should be used when wire-OR connections exceed 1 inch apart on a drive line.

B. Off-Card Clock Distribution

1. The OR/NOR outputs of an MC1660 may be used to drive into twisted pair lines or into flat, fixed-impedance ribbon cable. At the far end of the twisted pair on MC1692 differential line receiver is used. The line should be terminated as shown in Figure 25. This method not only provides high speed, board-to-board clock distribution, but also provides system noise margin advantages. Since the line receiver operates independently of the V_{BB} reference voltage (differential inputs) the noise margin from board to board is also independent of temperature differentials.

LOGIC SHORTCUTS

MECL circuitry offers several logic design conveniences. Among these are:

1. **Wire-OR** (can be produced by wiring MECL output emitters together outside packages).

2. **Complementary Logic Outputs** (both OR and NOR are brought out to package pins in most cases).

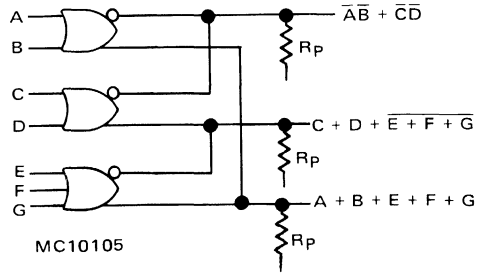
An example of the use of these two features to reduce gate and package count is shown in Figure 29.

The connection shown saves several gate circuits over performing the same functions with non-ECL type logic. Also, the logic functions in Figure 29 are all accomplished with one gate propagation delay time for best system speed. Wire-ORing permits direct connections of MECL circuits to busses. (MECL System Design Handbook and Application Note AN-726).

Propagation delay is increased approximately 50 ps per wire-OR connection. In general, wire-OR should be limited to 6 MECL outputs to maintain a proper LOW logic level. The MC10123 is an exception to this rule because it has a special V_{OL} level that allows very high fanout on a bus or wire-OR line. The use of a single output pull-down resistor is recommended per wire-OR, to economize on power dissipation. However, two pull-down resistors per wired-OR can improve fall times and be used for double termination of busses.

Wire-OR should be done between gates in a package or nearby packages to avoid spikes due to line propagation delay. This does not apply to bus lines which activate only one driver at a time.

FIGURE 29 — USE OF WIRE-OR AND
COMPLEMENTARY OUTPUTS



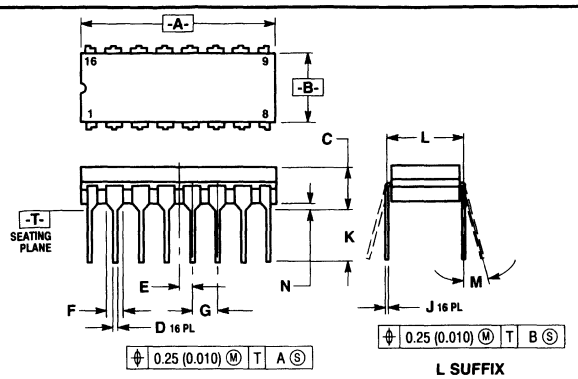
SYSTEM CONSIDERATIONS — A SUMMARY OF RECOMMENDATIONS

	MECL 10H	MECL 10K	MECL III
Power Supply Regulation	±5% (1)	10% (2)	10% (2)
On-Card Temperature Gradient	20°C	Less Than 25°C	Less Than 25°C
Maximum Non-Transmission Line Length (No Damping Resistor)	1″	8″	1″
Unused Inputs	Leave Open (3)	Leave Open (3)	Leave Open (3)
PC Board	Multilayer	Standard 2-Sided or Multilayer	Multilayer
Cooling Requirements	500 lfpm Air	500 lfpm Air	500 lfpm Air
Bus Connection Capability	Yes (Wire-OR)	Yes (Wire-OR)	Yes (Wire-OR)
Maximum Twisted Pair Length (Differential Drive)	Limited By Cable Response Only, Usually >1000′	Limited by Cable Response Only, Usually >1000′	Limited by Cable Response Only, Usually >1000′
The Ground Plane to Occupy Percent Area of Card	>75%	>50%	>75%
Wire Wrap may be used	Not Recommended	Yes	Not Recommended
Compatible with MECL 10,000	Yes	—	Yes

(1) All dc and ac parameters guaranteed for $V_{EE} = -5.2\ V \pm 5\%$.
(2) At the devices (functional only).
(3) Except special functions without input pull-down resistors.

PACKAGE OUTLINE DIMENSIONS

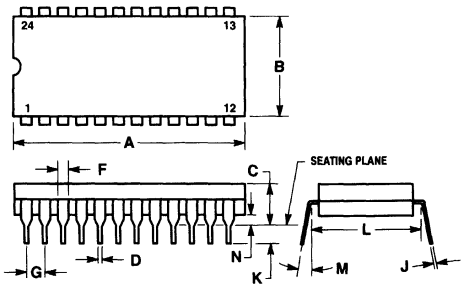
A letter suffix to the MECL logic function part number is used to specify the package style (see drawings below). See appropriate selector guide for specific packaging available for a given device type.



L SUFFIX
CERAMIC PACKAGE
CASE 620-09

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

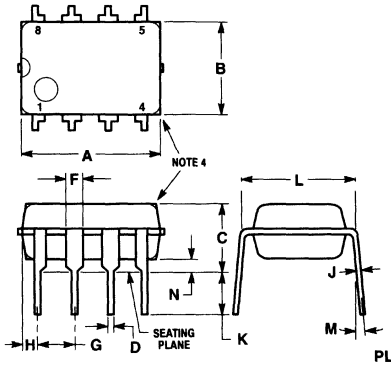
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035



L SUFFIX
CERAMIC PACKAGE
CASE 623-05

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

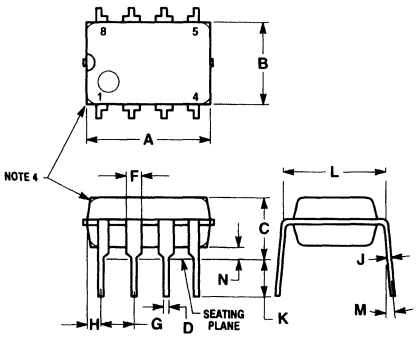


P SUFFIX
PLASTIC PACKAGE
CASE 626-04

NOTES:
1. LEAD POSITIONAL TOLERANCE:
   ϕ 0.13 (0.005) M T A M B M
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.51	0.76	0.020	0.030

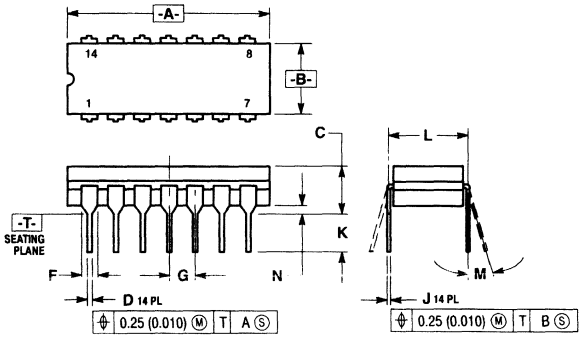
PACKAGE OUTLINE DIMENSIONS (continued)



P SUFFIX
PLASTIC PACKAGE
CASE 626-05

NOTES:
1. LEAD POSITIONAL TOLERANCE:
   ⌖ | φ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

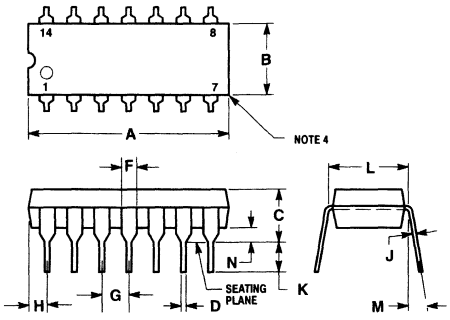
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040



L SUFFIX
CERAMIC PACKAGE
CASE 632-08

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. 632-01 THRU -07 OBSOLETE, NEW STANDARD 632-08.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

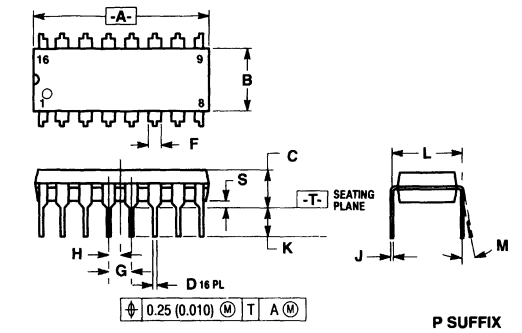


P SUFFIX
PLASTIC PACKAGE
CASE 646-06

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.
5. 646-05 OBSOLETE, NEW STANDARD 646-06.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

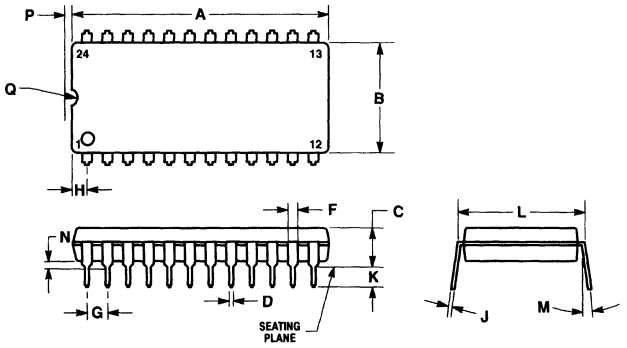
PACKAGE OUTLINE DIMENSIONS (continued)



P SUFFIX
PLASTIC PACKAGE
CASE 648-08

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

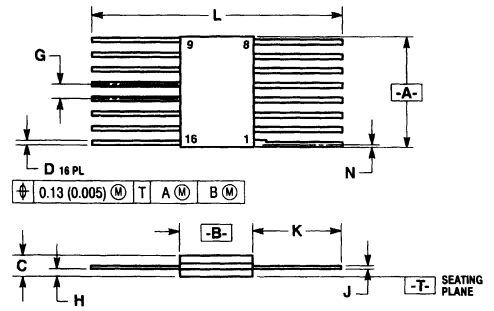
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040



P SUFFIX
PLASTIC PACKAGE
CASE 649-03

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. 649-02 OBSOLETE, NEW STD 649-03 SEE ISSUE "C" FOR REFERENCE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

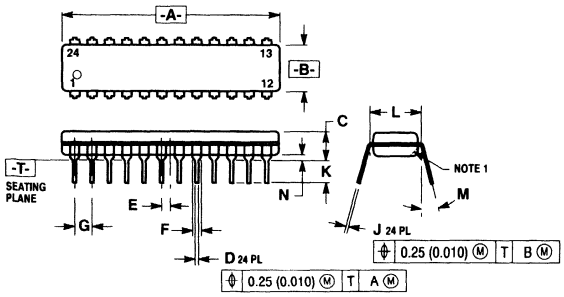


F SUFFIX
CERAMIC PACKAGE
CASE 650-05

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "A" AND "B" ALLOW FOR LID MISALIGNMENT, AND GLASS MINISCUS.
4. DIMENSION "H" SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
5. LEAD NUMBER 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
6. DIMENSION "J" INCLUDES SOLDER LEAD FINISH.
7. LEAD NUMBERS SHOWN FOR REFERENCE ONLY.
8. 650-01 THRU -04 OBSOLETE, NEW STANDARD 650-05.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	9.90	0.370	0.390
B	6.23	6.60	0.245	0.260
C	1.53	2.15	0.060	0.085
D	0.36	0.48	0.014	0.019
G	1.27 BSC		0.050 BSC	
H	0.64	1.01	0.025	0.040
J	0.11	0.17	0.004	0.007
K	6.35	9.39	0.250	0.370
L	18.93	—	0.745	—
N	—	0.50	—	0.020

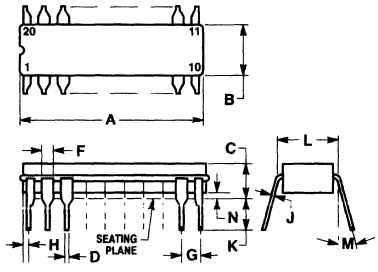
PACKAGE OUTLINE DIMENSIONS (continued)



NOTES:
1. CHAMFERRED CONTOUR OPTIONAL.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

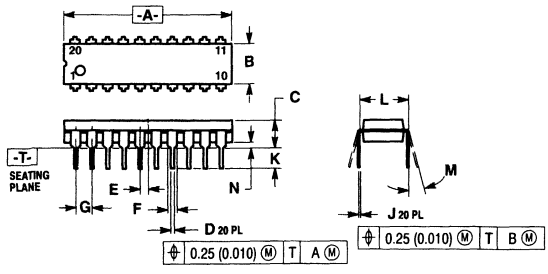
P SUFFIX
PLASTIC PACKAGE
CASE 724-03



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

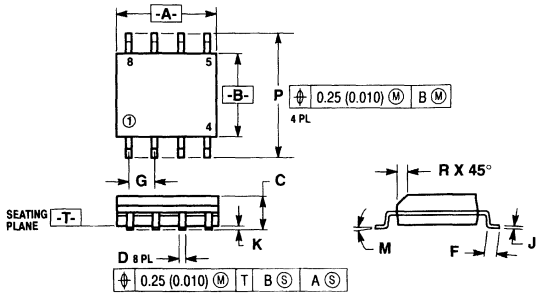
L SUFFIX
CERAMIC PACKAGE
CASE 732-03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. 738-02 OBSOLETE, NEW STANDARD 738-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

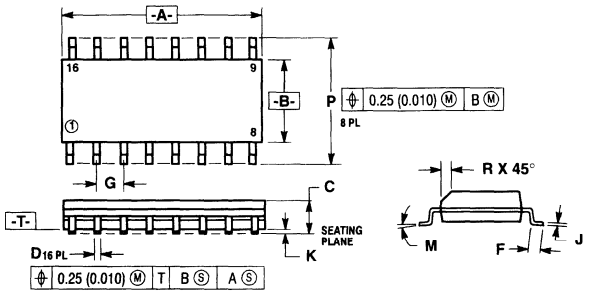
P SUFFIX
PLASTIC PACKAGE
CASE 738-03



D SUFFIX
PLASTIC PACKAGE
CASE 751-03

NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIM: MILLIMETER.
4. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
6. 751-01 AND -02 OBSOLETE, NEW STANDARD 751-03.

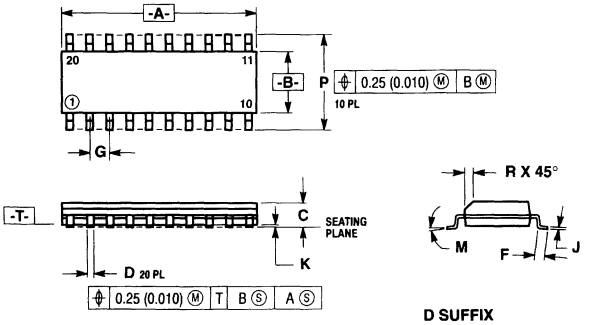
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019



D SUFFIX
PLASTIC PACKAGE
CASE 751B-04

NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
6. 751B-03 IS OBSOLETE, NEW STANDARD 751B-04.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

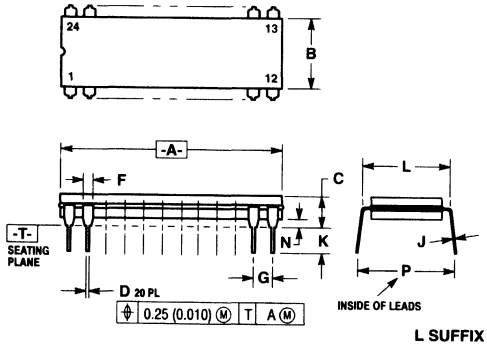


D SUFFIX
PLASTIC PACKAGE
CASE 751D-03

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751D-01, AND -02 OBSOLETE, NEW STANDARD 751D-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

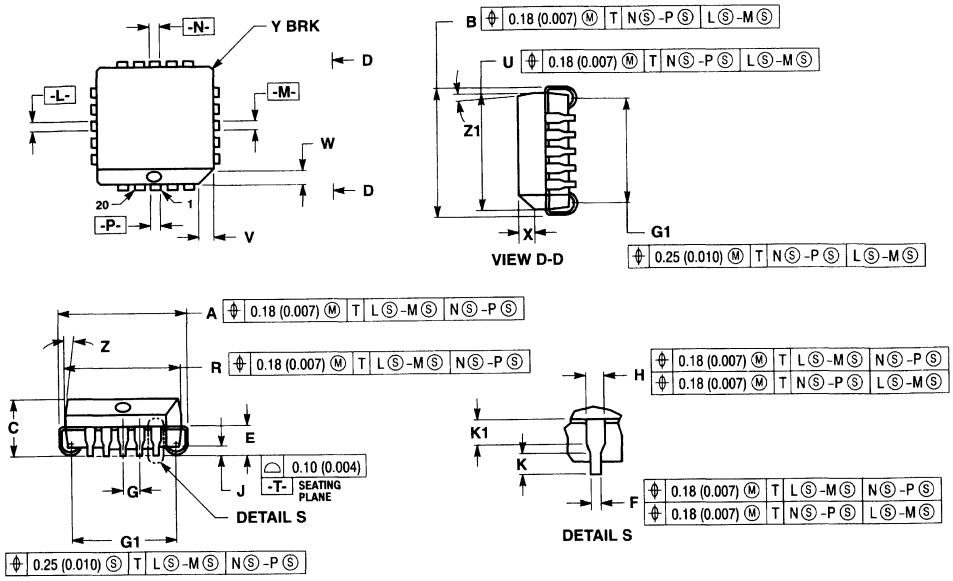
PACKAGE OUTLINE DIMENSIONS (continued)



L SUFFIX
CERAMIC PACKAGE
CASE 758-01

NOTES:
1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.50	32.64	1.240	1.285
B	7.24	7.75	0.285	0.305
C	3.68	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.14	1.57	0.045	0.062
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	7.62	7.87	0.300	0.310
N	0.51	1.27	0.020	0.050
P	9.14	10.16	0.360	0.400

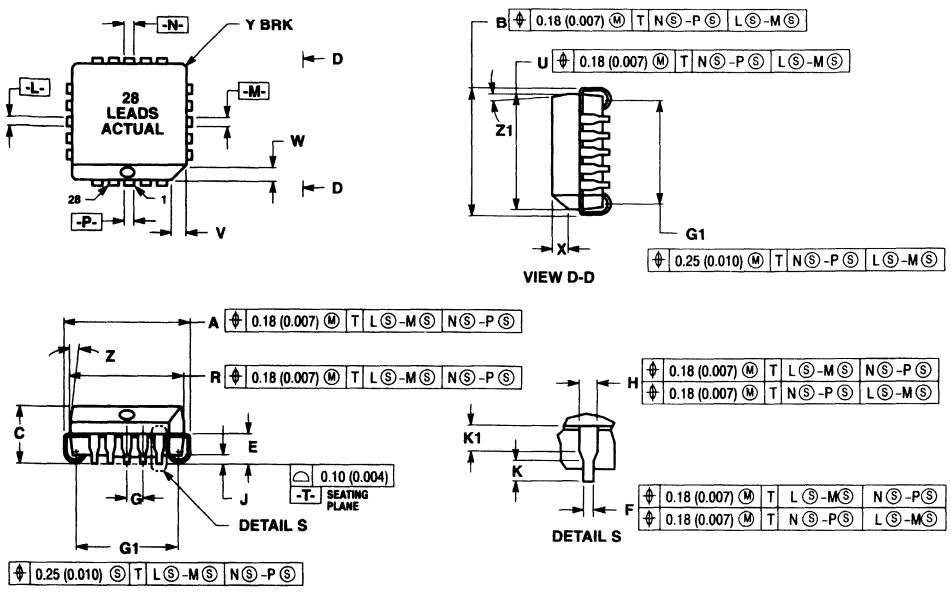


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.78	10.03	0.385	0.395
B	9.78	10.03	0.385	0.395
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	7.88	8.38	0.310	0.330
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
2. DIM GI, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. 775-01 IS OBSOLETE, NEW STANDARD 775-02.

FN SUFFIX
PLASTIC PACKAGE
CASE 775-02

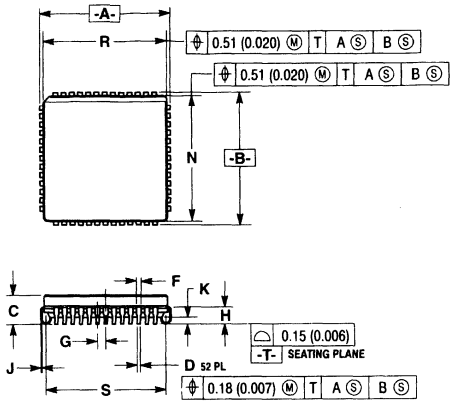
PACKAGE OUTLINE DIMENSIONS (continued)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. 776-01 IS OBSOLETE, NEW STANDARD 776-02.

FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

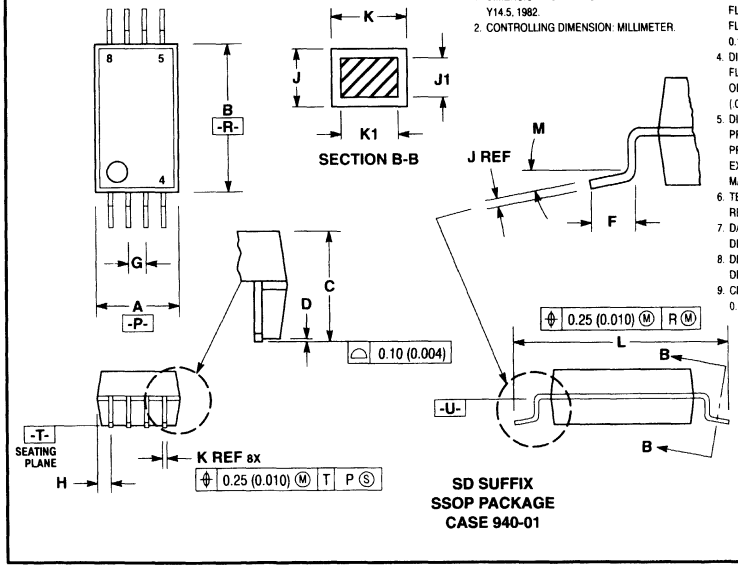


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM R AND N DO NOT INCLUDE GLASS PROTRUSION. GLASS PROTRUSION TO BE 0.25 (0.010) MAXIMUM.
4. ALL DIMENSIONS AND TOLERANCES INCLUDE LEAD TRIM OFFSET AND LEAD FINISH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.94	20.19	0.785	0.795
B	19.94	20.19	0.785	0.795
C	4.20	5.08	0.165	0.200
D	0.44	0.53	0.017	0.021
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	2.29	3.30	0.090	0.130
J	0.16	0.25	0.006	0.010
K	0.89	1.14	0.035	0.045
N	18.67	19.20	0.735	0.756
R	18.67	19.20	0.735	0.756
S	17.53	18.54	0.690	0.730

FJ SUFFIX
J-LEAD CERQUAD
CASE 778B-01

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (.006) PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (.010) PER SIDE.
5. DIMENSION "K" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (.003) TOTAL IN EXCESS OF THE "K" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DATUMS -P- AND -R- ARE TO BE DETERMINED AT DATUM PLANE -U-.
8. DIMENSION "A" AND "B" ARE TO BE DETERMINED AT DATUM PLANE -U-.
9. CROSS SECTION B-B TO BE DETERMINED AT 0.10 (.004) TO 0.25 (.010) FROM THE LEADTIP.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.87	3.13	0.113	0.123
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.55	0.95	0.022	0.037
G	0.65 BSC		0.026 BSC	
H	0.50	—	0.020	—
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.22	0.38	0.009	0.015
K1	0.22	0.33	0.009	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

SD SUFFIX
SSOP PACKAGE
CASE 940-01

MECL Logic Surface Mount

WHY SURFACE MOUNT?

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the State-of-the-Art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

MECL AVAILABILITY IN SURFACE MOUNT

Motorola is now offering MECL 10K and MECL 10H in the PLCC (Plastic Leaded Chip Carrier) packages.

MECL in PLCC may be ordered in conventional plastic rails or on Tape and Reel. Refer to the Tape and Reel section for ordering details.

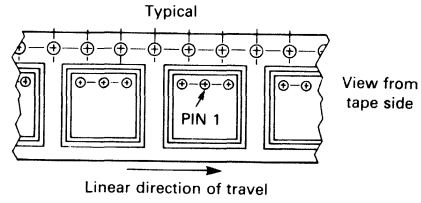
TAPE AND REEL

Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. The packaging fully conforms to the latest EIA RS-481A specification. The antistatic embossed tape provides a secure cavity sealed with a peel-back cover tape.

GENERAL INFORMATION

- Reel Size 13 inch (330 mm) Suffix: R2
- Tape Width 16 mm
- Units/Reel 1000

MECHANICAL POLARIZATION



ORDERING INFORMATION

- Minimum Lot Size/Device Type = 3000 Pieces.
- No Partial Reel Counts Available.
- To order devices which are to be delivered in Tape and Reel, add the appropriate suffix to the device number being ordered.

EXAMPLE:

ORDERING CODE	SHIPMENT METHOD
MC10100FN	Magazines (Rails)
MC10100FNR2	13 inch Tape and Reel
MC10H100FN	Magazines (Rails)
MC10H100FNR2	13 inch Tape and Reel
MC12015D	Magazines (Rails)
MC12015DR2	13 inch Tape and Reel

DUAL-IN-LINE PACKAGE TO PLCC PIN CONVERSION DATA

The following tables give the equivalent I/O pinouts of Dual-In-Line (DIL) packages and Plastic Leaded Chip Carrier (PLCC) packages.

Conversion Tables

8 PIN DIL	1	2	3	4	5	6	7	8
20 PIN PLCC	2	5	7	10	12	15	17	20

14 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14
20 PIN PLCC	2	3	4	6	8	9	10	12	13	14	16	18	19	20

16 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
20 PIN PLCC	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

20 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
20 PIN PLCC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

24 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
28 PIN PLCC	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28

Logic Literature Listing

For additional information, refer to the following Motorola Logic Documents available through the Literature Distribution Centers listed on the back cover of this document.

1

LOGIC NEW PRODUCT CALENDAR

BR1332/D Logic New Product Calendar

SELECTOR GUIDES

SG73/D Motorola Semiconductor Master Selection Guide

SG127/D Surface Mount Products Selector Guide

SG366/D TTL, ECL, CMOS and Special Logic Circuits Selector Guide

DATA BOOKS

DL121/D FAST and LS TTL Data

DL122/D MECL Device Data

DL129/D High-Speed CMOS Logic Data

DL131/D CMOS Logic Data

DL138/D FACT Device Data

DL140/D ECLinPS Data

DESIGN HANDBOOKS

HB205/D MECL Systems Design Handbook

OTHER LITERATURE

BR1330/D ECLinPS Lite™ (Single Gate ECL Devices and Translators)

BR1333/D Motorola Timing Solutions

BR1334/D High Performance Frequency Control Products

BR1409/D Motorola ECL300™ LogicArray

EB48/D A Time Base and Control Logic Subsystem for High Frequency, High Resolution Counters

APPLICATION NOTES

AN270/D Nanosecond Pulse Handling Techniques

AN535/D Phase-Locked Loop Design Fundamentals

AN556/D Interconnection Techniques for Motorola's MECL 10K Series Emitter Coupled Logic

AN567/D MECL Positive and Negative Logic

AN701/D Understanding MECL 10K DC and AC Data Sheet Specifications

AN720/D Interfacing with MECL 10K Integrated Circuits

AN726/D Bussing with MECL 10K Integrated Circuits

AN730A/D A High-Speed FIFO Memory Using the MECL MCM10143 Register File

AN827/D Technique of Direct Programming Using Two-Modulus Prescaler

AN1091/D Low Skew Clock Drivers and Their System Design Considerations

AN1092/D Driving High Capacitance DRAMs in an ECL System

AN1400/D H64x Clock Driver I/O SPICE Modelling Kit

AN1401/D Using SPICE to Analyze the Effects of Board Layout on System Skew When Designing With the MC10/100640 Family of Clock Drivers

AN1402/D MC10/100H600 Translator Family I/O SPICE Modelling Kit

AN1403/D FACT™ I/O Model Kit

AN1404/D ECLinPS™ Circuit Performance at Non-Standard VIH Levels

AN1405/D ECL Clock Distribution Techniques

AN1406/D Designing With PECL (ECL at +5.0 V)

AN1407/D Performance Testing With the ALExIS™ Mini-Evaluation Boards

AN1503/D ECLinPS™ I/O SPICE Modelling Kit

AN1504/D Metastability and the ECLinPS™ Family

APPLICATIONS ASSISTANCE FORM

In the event that you have any questions or concerns about the performance of any Motorola device listed in this catalog, please contact your local Motorola sales office or the Motorola Help line for assistance. If further information is required, you can request direct factory assistance.

Please fill out as much of the form as is possible if you are contacting Motorola for assistance or are sending devices back to Motorola for analysis. Your information can greatly improve the accuracy of analysis and can dramatically improve the correlation response and resolution time.

Items 4 thru 8 of the following form contain important questions that can be invaluable in analyzing application or device problems. It can be used as a self-help diagnostic guideline or for a baseline of information gathering to begin a dialog with Motorola representatives.

MOTOROLA Device Correlation/Component Analysis Request Form

— Please fill out entire form and return with devices to MOTOROLA INC., R&QA DEPT., 2200 W. Broadway, Mesa, AZ 85202.

1) Name of Person Requesting Correlation: _____

   Phone No: _____ Job Title: _____ Company: _____

2) Alternate Contact: _____ Phone/Position: _____

3) Device Type (user part number): _____

4) Industry Generic Device Type: _____

5) # of devices tested/sampled: _____

   # of devices in question*: _____

   # returned for correlation: _____

   * In the event of 100% failure, does Customer have other date codes of Motorola devices that pass inspection?

   Yes _____ No _____ Please specify passing date code(s) if applicable _____

   If none, does customer have viable alternate vendor(s) for device type?

   Yes _____ No _____ Alternate vendor's name _____

6) Date code(s) and Serial Number(s) of devices returned for correlation — If possible, please provide one or two "good" units (Motorola's and/or other vendor) for comparison: _____

7) Describe USER process that device(s) are questionable in:

   ____ Incoming component inspection {test system = ?}: _____

   ____ Design prototyping: _____

   ____ Board test/burn-in: _____

   ____ Other (please describe): _____

   _____

8) Please describe the device correlation operating parameters as completely as possible for device(s) in question:

> Describe all pin conditions (e.g. floating, high, low, under test, stimulated but not under test, whatever ...), including any input or output loading conditions (resistors, caps, clamps, driving devices or devices being driven ...). Potentially critical information includes:

   ____ Input waveform timing relationships

   ____ Input edge rates

   ____ Input Overshoot or Undershoot — Magnitude and Duration

   ____ Output Overshoot or Undershoot — Magnitude and Duration

> Photographs, plots or sketches of relevent inputs and outputs with voltages and time divisions clearly identified for all waveforms are greatly desirable.

> V_{CC} and Ground waveforms should be carefully described as these characteristics vary greatly between applications and test systems. Dynamic characteristics of Ground and V_{CC} during device switching can dramatically effect input and internal operating levels. Ground & V_{CC} measurements should be made as physically close to the device in question as possible.

> Are there specific circumstances that seem to make the questionable unit(s) worse? Better?

   ____ Temperature _____

   ____ V_{CC} _____

   ____ Input rise/fall time _____

   ____ Output loading (current/capacitance) _____

   ____ Others _____

> ATE functional data should include pattern with decoding key and critical parameters such as V_{CC}, input voltages, Func step rate, voltage expected, time to measure.

MECL 10H

Selector Guide | **Data Sheets** | **2**

MECL 10H
INTEGRATED CIRCUITS

MC10H100 Series
0 to 75°C

2

Function Selection — (0 to +75°C)

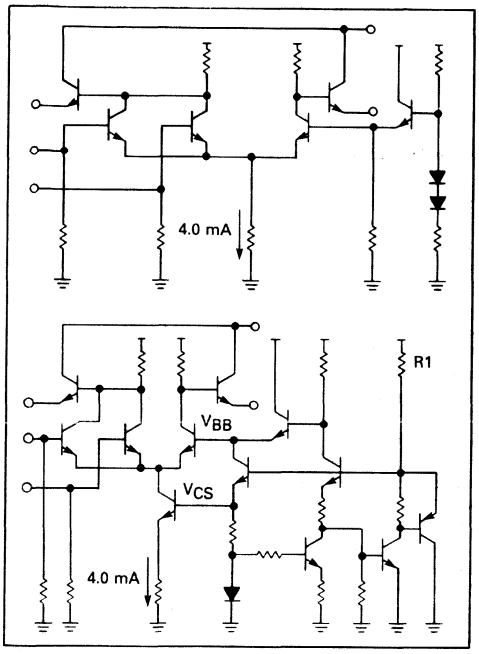
Function	Device	Case
NOR Gate		
Quad 2-Input with Strobe	MC10H100	620, 648, 775
Quad 2-Input	MC10H102	620, 648, 775
Triple 4-3-3 Input	MC10H106	620, 648, 775
Dual 3-Input 3-Output	MC10H211	620, 648, 775
OR Gate		
Quad 2-Input	MC10H103	620, 648, 775
Dual 3-Input 3-Output	MC10H210	620, 648, 775
AND Gates		
Quad AND	MC10H104	620, 648, 775
Complex Gates		
Quad OR/NOR	MC10H101	620, 648, 775
Triple 2-3-2 Input OR/NOR	MC10H105	620, 648, 775
Triple Exclusive OR/NOR	MC10H107	620, 648, 775
Dual 4-5 Input OR/NOR	MC10H109	620, 648, 775
Quad Exclusive OR	MC10H113	620, 648, 775
Dual 2-Wide OR-AND/OR-AND INVERT	MC10H117	620, 648, 775
Dual 2-Wide 3-Input OR/AND	MC10H118	620, 648, 775
4-Wide 4-3-3-3 Input OR-AND	MC10H119	620, 648, 775
4-Wide OR-AND/OR-AND INVERT	MC10H121	620, 648, 775
Hex Buffer w/Enable	MC10H188	620, 648, 775
Hex Inverter w/Enable	MC10H189	620, 648, 775
Translators		
Quad TTL to MECL	MC10H124	620, 648, 775
Quad MECL to TTL	MC10H125	620, 648, 775
Quad MECL-to-TTL Translator, Single Power Supply (−5.2 V or +5.0 V)	MC10H350	620, 648, 775
Quad TTL/NMOS to MECL Translator	MC10H351	732, 738, 775
Quad CMOS to MECL Translator	MC10H352	732, 738, 775
Quad TTL to MECL, ECL Strobe	MC10H424	620, 648, 775
9-Bit TTL-ECL Translator	MC10H/100H600	776
9-Bit ECL-TTL Translator	MC10H/100H601	776
9-Bit Latch/TTL-ECL Translator	MC10H/100H602	776
9-Bit Latch/ECL-TTL Translator	MC10H/100H603	776
Registered Hex TTL-ECL Translator	MC10H/100H604	776
Registered Hex ECL-TTL Translator	MC10H/100H605	776
Registered Hex TTL-PECL Translator	MC10H/100H606	776
Registered Hex PECL-TTL Translator	MC10H/100H607	776
Receivers		
Quad Line Receiver	MC10H115	620, 648, 775
Triple Line Receiver	MC10H116	620, 648, 775
Flip-Flop Latches		
Dual D Master Slave Flip-Flop	MC10H131	620, 648, 775
Dual J-K Master Slave Flip-Flop	MC10H135	620, 648, 775
Hex D Flip-Flop	MC10H176	620, 648, 775
Dual D Latch	MC10H130	620, 648, 775
Quint Latch	MC10H175	620, 648, 775
Hex D Flip-Flop w/Common Reset	MC10H186	620, 648, 775
Parity Checker		
12-Bit Parity Generator/Checker	MC10H160	620, 648, 775
Encoders Decoders		
Binary to 1-8 (Low)	MC10H161	620, 648, 775
Binary to 1-8 (High)	MC10H162	620, 648, 775
Dual Binary to 1-4 (Low)	MC10H171	620, 648, 775
Dual Binary to 1-4 (High)	MC10H172	620, 648, 775
8-Input Priority Encoder	MC10H165	620, 648, 775

Function	Device	Case
Transceivers		
4-Bit Differential ECL Bus to TTL Bus Transceiver	MC10/100H680	776
Hex ECL-TTL Transceiver w/Latches	MC10/100H681	776
Data Selector Multiplexer		
Quad Bus Driver/Receiver with 2-to-1 Output Multiplexers	MC10H330	758, 724, 776
Dual Bus Driver/Receiver with 4-to-1 Output Multiplexers	MC10H332	732, 738, 775
Quad 2-Input Multiplexers (Noninverting)	MC10H158	620, 648, 775
Quad 2-Input Multiplexers (Inverting)	MC10H159	620, 648, 775
8-Line Multiplexer	MC10H164	620, 648, 775
Quad 2-Input Multiplexer Latch	MC10H173	620, 648, 775
Dual 4-1 Multiplexer	MC10H174	620, 648, 775
Counters		
Universal Hexadecimal	MC10H136	620, 648, 775
Binary Counter	MC10H016	620, 648, 775
Arithmetic Functions		
Look Ahead Carry Block	MC10H179	620, 648, 775
Dual High Speed Adder/Subtractor	MC10H180	620, 648, 775
4-Bit ALU	MC10H181	623, 649 724, 758, 776
Special Function		
4-Bit Universal Shift Register	MC10H141	620, 648, 775
16 x 4 Bit Register File	MC10H145	620, 648, 775
5-Bit Magnitude Comparator	MC10H166	620, 648, 775
Quad Bus Driver/Receiver with Transmit and Receiver Latches	MC10H334	732, 738, 775
4-Bit ECL-TTL Load Reducing DRAM Driver	MC10H/100H660	776
Memories		
16 x 4 Bit Register File	MC10H145	620, 648, 775
Bus Driver (25 ohm outputs)		
Triple 4-3-3 Input Bus Driver (25 Ohms)	MC10H123	620, 648, 775
Quad Bus Driver/Receiver with 2-to-1 Output Multiplexers	MC10H330	724, 758, 776
Dual Bus Driver/Receiver with 4-to-1 Output Multiplexers	MC10H332	732, 738, 775
Quad Bus Driver/Receiver with Transmit and Receiver Latches	MC10H334	732, 738, 775
Triple 3-Input Bus Driver with Enable (25 Ohm)	MC10H423	620, 648, 775
OR/NOR Gate		
Dual 4-5 Input OR/NOR Gate	MC10H209	620, 648, 775
Clock Drivers		
68030/40 ECL-TTL Clock Driver	MC10/100H640	776
Single Supply PECL-ECL 1:9 Clock Distribution	MC10/100H641	776
68030/40 ECL-TTL Clock Driver	MC10/100H642	776
Dual Supply ECT-TTL 1:8 Clock Driver	MC10/100H643	776
68030/40 PECL-TTL Clock Driver	MC10/100H644	775
1:9 TTL Clock Driver	MC10H645	776
PECL-TTL-TTL 1:8 Clock Distribution Chip	MC10/100H646	776

MECL 10H INTRODUCTION

Motorola's new MECL 10H family features 100% improvement in propagation delay and clock speeds while maintaining power supply current equal to MECL 10K. This new MECL family is voltage compensated which allows guaranteed dc and switching parameters over a ±5% power supply range. Noise margins of MECL 10H are 75% better than the MECL 10K series over the ±5% power supply range. MECL 10H is compatible with MECL 10K and MECL III, a key element in allowing users to enhance existing systems by increasing the speed in critical timing areas. Also, many MECL 10H devices are pinout/functional duplications of the MECL 10K series devices.

FIGURE 1 — MECL 10K versus MECL 10H GATE DESIGN



The schematics in Figure 1 compare the basic gate structure of the MECL 10H to that of MECL 10K devices. The gate switch current is established with a current source in the MECL 10H family as compared to a resistor source in MECL 10K. The bias generator in the MECL 10K device has been replaced with a voltage regulator in the MECL 10H series. The advantages of these design changes are: current-sources permit-matched collector resistors that yield correspondingly better matched delays, less variation in the output-voltage level with power supply changes, and matched output-tracking rates with temperature. These circuit changes increase complexity at the gate level; however, the added performance more than compensates.

The MECL 10H family is being fabricated using Motorola's MOSAIC I (Motorola Oxide Self Aligned Implanted Circuits). The switching transistor's geometries obtained in the MOSAIC I process show a two-fold improvement in f_T, a reduction of more than 50% in parasitic capacitance and a decrease in device area of almost 76%.

FIGURE 2 — MOSAIC versus MECL 10K SWITCHING TRANSISTOR GEOMETRY

With improved geometry, the MECL 10H switching transistors (left) are one-seventh the size of the older MECL 10K transistors (right). Along with the smaller area comes an improved f_T and reduced parasitic capacitances.

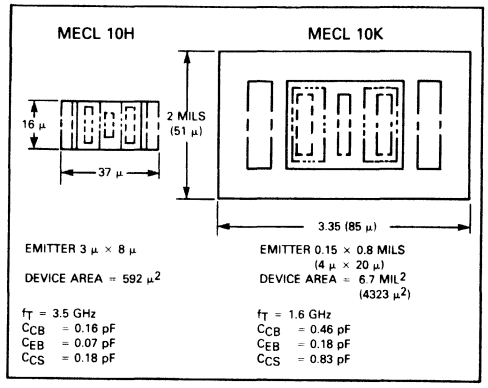


Figure 2 illustrates the relative size difference between the junction isolated transistor of MECL 10K and the MOSAIC I transistor of MECL 10H. This suggests that performance could be improved twofold at lower power levels. However, at the gate level, the power of the output transistor cannot be reduced without sacrificing output characteristics because of the 50 ohm drive requirements of MECL. In more complex functions, where part of the delay is associated with internal gates, MECL 10H devices use less power than the equivalent MECL 10K devices and provide an even more significant improvement in ac performance.

Table 1. — TYPICAL FAMILY CHARACTERISTICS FOR 10K AND 10H CIRCUITS

	10K	10H
Propagation delay (ns)	2.0	1.0
Power (mW)	25	25
Power-speed product (pJ)	50	25
Rise/fall times (ns) (20–80%)	2.0	1.0
Temperature range (°C)	−30 to +85	0 to +75
Voltage regulated	No	Yes
Technology	Junction isolated	Oxide isolated
V_{EE} = −5.2 V		

Supply & Temperature Variation

MECL 10H temperature and voltage compensation is designed to guarantee compatibility with MECL 10K, MECL III, MECL Memories and the MC10900 and Macrocell Array products. Table 1 summarizes some performance characteristics of the MECL 10K and 10H logic families in a 16-pin DIP. The MECL 10H devices offer typical propagation delays of 1.0 ns at 25 mW per gate when operated from a V_{EE} of −5.2 V. The resulting speed-power product of 25 picojoules is the best of any ECL logic family available today.

The operating temperature range is changed from −30°C to +85°C of the MECL 10K family to the narrower range of 0°C to 75°C for MECL 10H. This change matches the constraints established by the memory and array products. Operation at −30°C would require compromises in performance and power. With few exceptions, commercial applications are satisfied by 0°C min.

Table 2. — MECL 10H AC SPECIFICATIONS AND TRACKING

Parameter	0°C Min	0°C Typ	0°C Max	25°C Min	25°C Typ	25°C Max	75°C Min	75°C Typ	75°C Max	Units
t_{PD}	0.4	1.0	1.5	0.4	1.0	1.6	0.4	1.0	1.7	ns
	Min		Max	Min		Max	Min		Max	
t_R (20–80%)	0.5		1.5	0.5		1.6	0.5		1.7	ns
t_F (20–80%)	0.5		1.5	0.5		1.6	0.5		1.7	ns

V_{EE} = −5.2 V ±5%

Parameter		Propagation delay (ns)* Typ	Propagation delay (ns)* Max	Delay variation vs temp (ps/°C) Typ	Delay variation vs temp (ps/°C) Max	Delay variation vs supply (ps/V) Typ	Delay variation vs supply (ps/V) Max
t_{PD}	10K	2.0	2.9	2.0	7.0	80	
	10H	1.0	1.5	0.5	4.0	0	0

*V_{EE} = −5.2 V, Temp = 25°C

AC specifications of MECL 10H products appear in Table 2. In the MECL 10H family, all ac specifications have guaranteed minimums and maximums for extremes of both temperature and supply — a first in ECL logic. In addition, flip flops, latches and counters will have guaranteed limits for setup time, hold time, and clock pulse width. The limits in Table 2 are guaranteed for a power supply variation of ±5%. MECL 10K typically has a propagation delay (t_{PD}) variation of 80 ps/V with no guaranteed maximum. The typical variation in t_{PD} for MECL 10H circuits is only 38 ps typically over the entire specified temperature range and power-supply tolerance, and is guaranteed not to exceed 300 ps.

The improved performance in temperature over MECL 10K are a result of the internal voltage regulator. The primary difference being the flatter tracking rate of the output "0" level voltage (V_{OL}). This difference does not affect the compatibility with existing MECL families.

Changes in output "1" level voltages (V_{OH}) with supply variations are 10 mV/V less for the MECL 10H family. V_{OH} varies with the supply, primarily because of changes in chip temperature caused by the changes in power dissipation. However, the current in the MECL 10H circuits remains almost constant with supply changes, since the circuits are voltage compensated and use current sources for all internal emitter followers. Threshold voltage (V_{BB}) and output "0" level voltage (V_{OL}) variations are shown with respect to MECL 10K in Table 3. In both cases voltage compensation has reduced the variations significantly.

Table 3. — LOGIC LEVEL DC TRACKING RATE FOR 10K AND 10H CIRCUITS

		Min	Typ	Max
$\Delta V_{OH}/\Delta T$ (mV/°C)	10H	1.2	1.3	1.5
	10K	1.2	1.3	1.5
$\Delta V_{BB}/\Delta T$ (mV/°C)	10H	0.8	1.0	1.2
	10K	0.8	1.0	1.2
$\Delta V_{OL}/\Delta T$ (mV/°C)	10H	0	0.4	0.6
	10K	0.35	0.5	0.75
		0.75	1.0	1.55
$\Delta V_{OH}/\Delta V_{EE}$ (mV/V)	10H	−20		0
	10K	−30		0
$\Delta V_{BB}/\Delta V_{EE}$ (mV/V)	10H	0	10	25
	10K	110	150	190
$\Delta V_{OL}/\Delta V_{EE}$ (mV/V)	10H	0	20	50
	10K	200	250	320

Noise Margin Considerations

Specification of input voltage levels (V_{IHA}, V_{ILA}) are changed from those of MECL 10K resulting in improved noise margins for MECL 10H.

The MECL 10K circuits have two sets of output voltage specifications (V_{OH}, V_{OHA} and V_{OL}, V_{OLA}). The first output voltage specification in each set (V_{OH} and V_{OL}) are guaranteed maximum and minimum output levels for typical input levels. The second specification in each set (V_{OHA} and V_{OLA}) is the guaranteed worst-case output level for input threshold voltages. System analysis for worst-case noise margin considers V_{OHA} and V_{OLA} only. The MECL 10H family has only one set of output voltages (V_{OH} and V_{OL}) with minimum and maximum values specified. The minimum value of V_{OH} and the maximum value for V_{OL} of the MECL 10H family is synonomous with the V_{OHA} and V_{OLA} specifications of MECL 10K family.

The V_{OH} values for the MECL 10H circuits are equal to or better than the MECL 10K levels at all temperatures. Input threshold voltages (V_{IHA} and V_{ILA}, which are synonymous with V_{IH} min and V_{IL} max for 10H) are also improved and guaranteed V_{IHA} has been decreased by 25 mV over the entire operating temperature range, resulting in a "1" level noise margin of 150 mV (compared to

Table 4. — NOISE MARGIN versus POWER-SUPPLY CONDITIONS

Parameter		V_{EE} −10% Typ	V_{EE} −10% Min	V_{EE} −5% Typ	V_{EE} −5% Min	V_{EE} Typ	V_{EE} Min	V_{EE} +5% Typ	V_{EE} +5% Min
Noise Margin High V_{NH} (mV)	10H	224	150	227	150	230	150	233	150
	10K	127	47	166	86	205	125	241	164
Noise Margin Low V_{NL} (mV)	10H	264	150	267	150	270	150	273	150
	10K	223	103	249	129	275	155	301	181

*Temp = 0 to 75°C

125 mV for the MECL 10K circuits). V_{ILA} has been decreased by 5.0 mV, providing a "0" level noise margin equal to the "1" level noise margin. The V_{OL} minimum of the MECL 10H is more negative than for MECL 10K (−1950 mV instead of −1850 mV). The V_{OL} level for the MECL 10K family was selected to ensure that the gate would not saturate at high temperatures and high supply voltages. The reduction in operating temperature range for the MECL 10H family and the improvement in tracking rate allow the lower V_{OL} level. The change in this level does not affect system noise margins. Although some of the interface levels change with temperature, the changes in voltage levels are well within the tolerance ranges that would keep the families compatible. Table 4 lists some noise margins for V_{EE} supply variations.

The compatibility of MECL 10H with MECL 10K may be demonstrated by applying the tracking rates in Table 3 to the dc specifications. The method for determining compatibility is to show acceptable noise margins for MECL 10H, MECL 10K and mixed MECL 10K/MECL 10H systems. The assumption is that the families are compatible if the noise margin for a mixed system is equal to or better than the same system using only the MECL 10K series.

Using an all MECL 10K system as a reference, three possible logic mixes must be considered: MECL 10K driving MECL 10H; MECL 10H driving MECL 10K; and MECL 10H driving MECL 10H. The system noise margin for the three configurations can now be calculated for the following cases (See Figure 3):

In Case 1, the system uses multiple power supplies, each independently voltage regulated to some percentage tolerance. Worst-case is where one device is at the plus extreme and the other device is at the minus extreme of the supply tolerance.

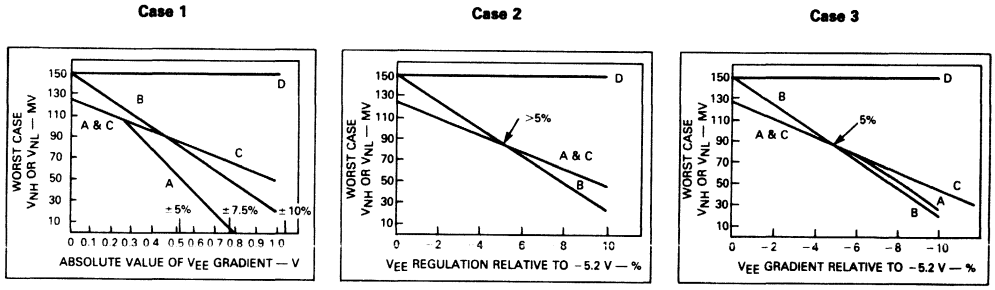
In Case 2, a system operates on a single supply or several supplies slaved to a master supply. The entire system can drift, but all devices are at the same supply voltage.

In Case 3, a system has excessive supply drops throughout. Supply gradients are due to resistive drops in V_{EE} bus.

The analysis indicates that the noise margins for a MECL 10K/10H system equal or exceed the margins for an all 10K system for supply tolerance up to ±5%. The results of the analysis are shown in Figure 3.

2

FIGURE 3 — NOISE MARGIN versus POWER-SUPPLY VARIATION



A. MECL 10K DRIVING MECL 10K B. MECL 10K DRIVING MECL 10H C. MECL 10H DRIVING MECL 10K D. MECL 10H DRIVING MECL 10H

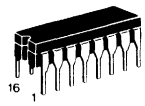
MOTOROLA

MC10H016

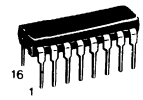
4-BIT BINARY COUNTER

The MC10H016 is a high-speed synchronous, presettable, cascadable 4-bit binary counter. It is useful for a large number of conversion, counting and digital integration applications.

- Counting Frequency, 200 MHz Minimum
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible
- Positive Edge Triggered



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

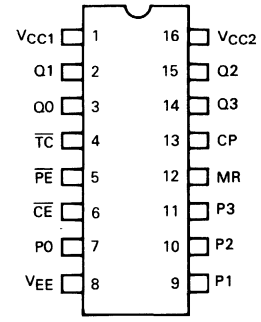
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	126	—	115	—	126	mA
Input Current High All Except MR Pin 12 MR	I_{inH}	 — —	 450 1190	 — —	 265 700	 — —	 265 700	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Clock to Q Clock to $\overline{TC}$ MR to Q	t_{pd}	 1.0 0.7 0.7	 2.4 2.4 2.4	 1.0 0.7 0.7	 2.5 2.5 2.5	 1.0 0.7 0.7	 2.7 2.6 2.6	ns
Set-up Time P_n to Clock $\overline{CE}$ or $\overline{PE}$ to Clock	t_{set}	 2.0 2.5	 — —	 2.0 2.5	 — —	 2.0 2.5	 — —	ns
Hold Time Clock to P_n Clock to $\overline{CE}$ or $\overline{PE}$	t_{hold}	 1.0 0.5	 — —	 1.0 0.5	 — —	 1.0 0.5	 — —	ns
Counting Frequency	f_{count}	200	—	200	—	200	—	MHz
Rise Time	t_r	0.5	2.0	0.5	2.1	0.5	2.2	ns
Fall Time	t_f	0.5	2.0	0.5	2.1	0.5	2.2	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

DIP
PIN ASSIGNMENT



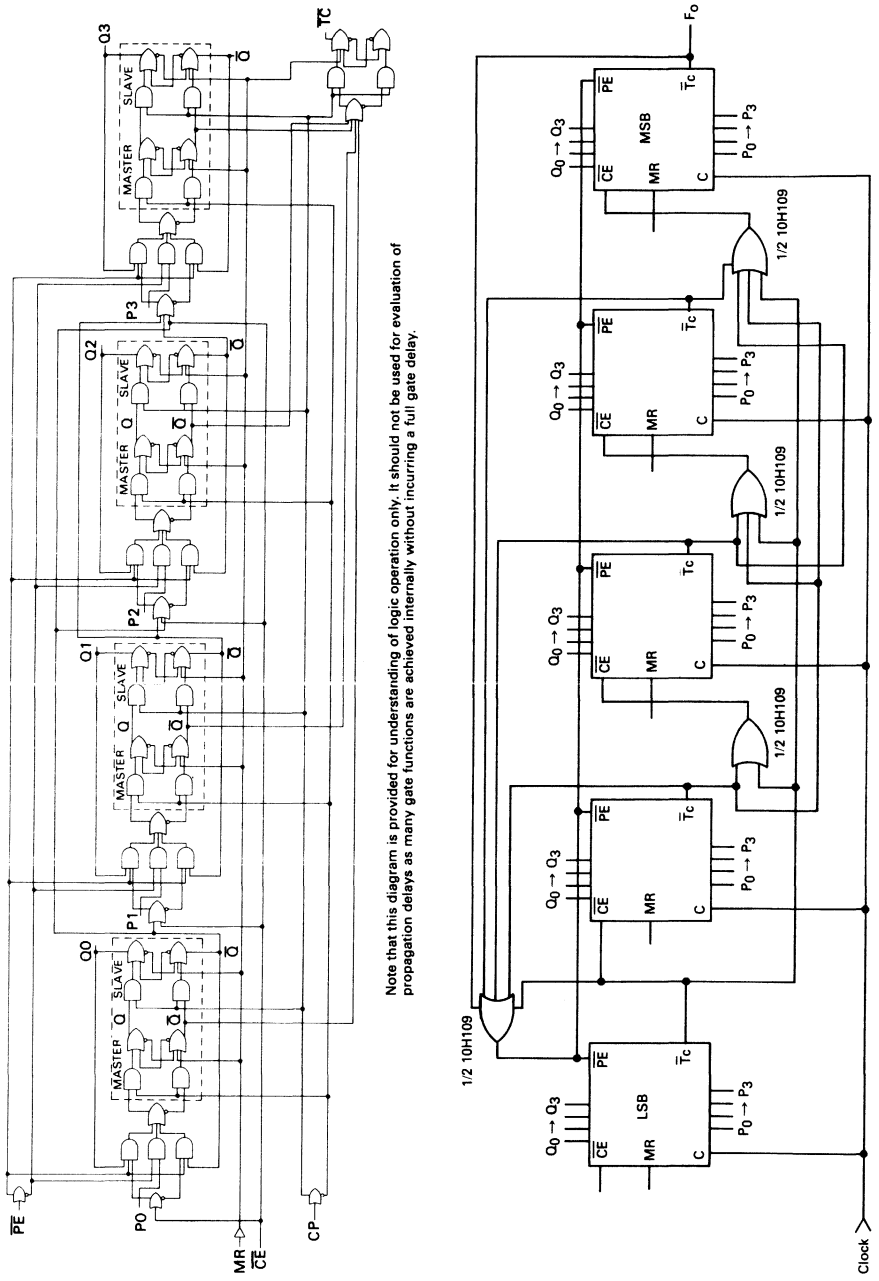
Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

TRUTH TABLE

$\overline{CE}$	$\overline{PE}$	MR	CP	Function
L	L	L	Z	Load Parallel (P_n to Q_n)
H	L	L	Z	Load Parallel (P_n to Q_n)
L	H	L	Z	Count
H	H	L	Z	Hold
X	X	L	ZZ	Masters Respond; Slaves Hold
X	X	H	X	Reset (Q_n = LOW, $\overline{T}_C$ = HIGH)

Z = Clock Pulse (Low to High); ZZ = Clock Pulse (High to Low)

Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.


4-BIT BINARY COUNTER LOGIC DIAGRAM
Q0
Q1
Q2
Q3
P0
P1
P2
P3
MASTER
SLAVE
PE
CP
MR
CE
TC
Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.
1/2 10H109
LSB
MSB
Q0 → Q3
P0 → P3
Fo
Clock
÷ N Counter 1 → 16^5
MC10H016 Cascaded for 5 Stage Presettable Counter
Max freq. is only OR gate delay below max when counting alone.

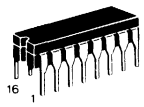
MOTOROLA

MC10H100

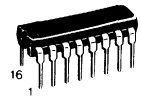
QUAD 2-INPUT NOR GATE WITH STROBE

The MC10H100 is a quad NOR gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates.

- Propagation Delay, 1.0 ns Typical
- 25 mW Typ/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

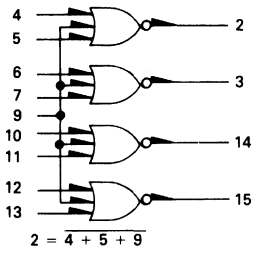
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	29	—	26	—	29	mA
Input Current High Pin 9 All Other Inputs	I_{inH}	 — —	 900 500	 — —	 560 310	 — —	 560 310	µA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Pin 9 Only Exclude Pin 9	t_{pd}	 0.65 0.4	 1.6 1.3	 0.7 0.45	 1.7 1.35	 0.7 0.5	 1.8 1.5	ns
Rise Time	t_r	0.5	2.0	0.5	2.1	0.5	2.2	ns
Fall Time	t_f	0.5	2.0	0.5	2.1	0.5	2.2	ns

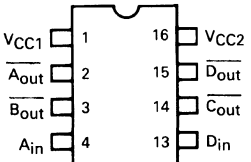
NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

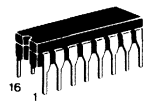
MOTOROLA

MC10H101

QUAD OR/NOR GATE

The MC10H101 is a quad 2-input OR/NOR gate with one input from each gate common to pin 12. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 25 mW/Gate (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

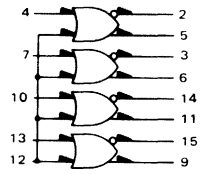
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	29	—	26	—	29	mA
Input Current High (Pin 12 only)	I_{inH}	— —	425 850	— —	265 535	— —	265 535	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Pin 12 Only Exclude Pin 12	t_{pd}	 0.5 0.5	 1.6 1.45	 0.5 0.5	 1.6 1.5	 0.5 0.5	 1.7 1.6	ns
Rise Time	t_r	0.5	2.1	0.5	2.2	0.5	2.3	ns
Fall Time	t_f	0.5	2.1	0.5	2.2	0.5	2.3	ns

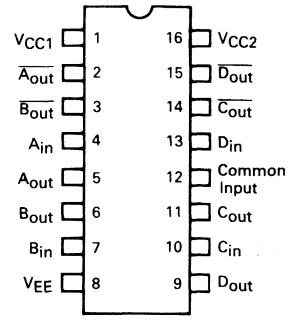
NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

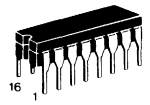
MOTOROLA

MC10H102

QUAD 2-INPUT NOR GATE

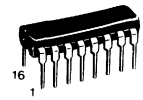
The MC10H102 is a quad 2-input NOR gate. The MC10H102 provides one gate with OR/NOR outputs. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 25 mW/Gate (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

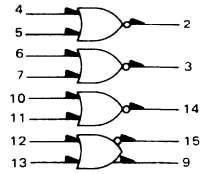
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	29	—	26	—	29	mA
Input Current High	I_{inH}	—	425	—	265	—	265	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.4	1.25	0.4	1.25	0.4	1.4	ns
Rise Time	t_r	0.5	1.5	0.5	1.6	0.55	1.7	ns
Fall Time	t_f	0.5	1.5	0.5	1.6	0.55	1.7	ns

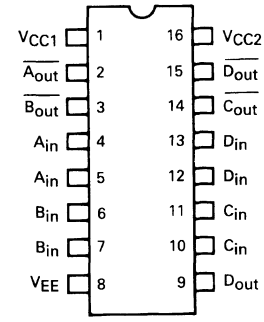
NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

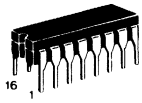
MOTOROLA

MC10H103

QUAD 2-INPUT OR GATE

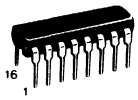
The MC10H103 is a quad 2-input OR gate. The MC10H103 provides one gate with OR/NOR outputs. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 25 mW/Gate (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

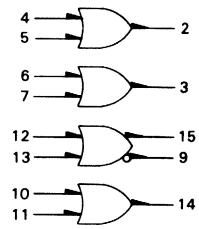
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

2

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–+75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

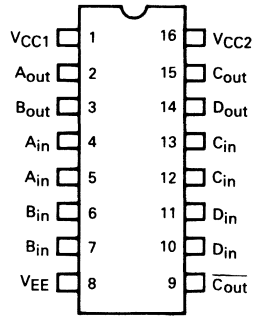
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	29	—	26	—	29	mA
Input Current High	I_{inH}	—	425	—	265	—	265	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.4	1.3	0.4	1.3	0.45	1.45	ns
Rise Time	t_r	0.5	1.7	0.5	1.8	0.5	1.9	ns
Fall Time	t_f	0.5	1.7	0.5	1.8	0.5	1.9	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

DIP
PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

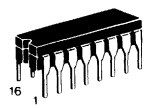
MOTOROLA

MC10H104

QUAD 2-INPUT AND GATE

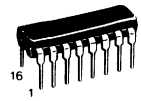
The MC10H104 is a quad 2-input AND gate. One of the gates has both AND/NAND outputs available. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 25 mW/Gate (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



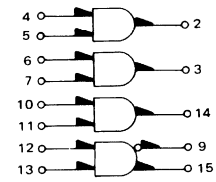
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



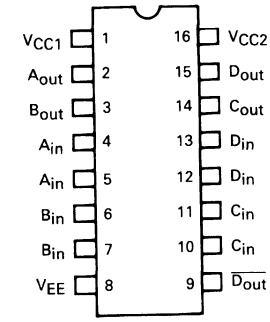
FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	39	—	35	—	39	mA
Input Current High	I_{inH}		425	—	265	—	265	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.4	1.6	0.45	1.75	0.45	1.9	ns
Rise Time	t_r	0.5	1.6	0.5	1.7	0.5	1.8	ns
Fall Time	t_f	0.5	1.6	0.5	1.7	0.5	1.8	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

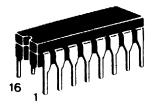
MOTOROLA

MC10H105

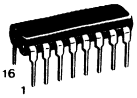
TRIPLE 2-3-2-INPUT OR/NOR GATE

The MC10H105 is a triple 2-3-2-input OR/NOR gate. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 25 mW/Gate (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

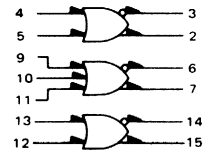
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	23	—	21	—	23	mA
Input Current High	I_{inH}	—	425	—	265	—	265	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.4	1.2	0.4	1.2	0.4	1.3	ns
Rise Time	t_r	0.5	1.5	0.5	1.6	0.5	1.7	ns
Fall Time	t_f	0.5	1.5	0.5	1.6	0.5	1.7	ns

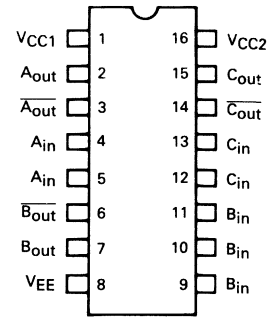
NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

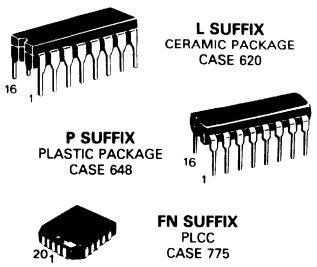
MOTOROLA

MC10H106

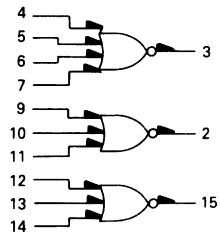
TRIPLE 4-3-3 INPUT NOR GATE

The MC10H106 is a triple 4-3-3 input NOR gate. This 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 – +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

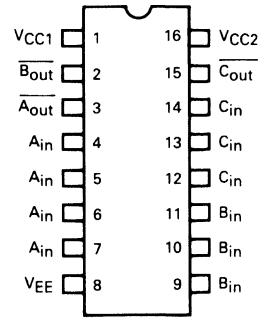
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	23	—	21	—	23	mA
Input Current High	I_{inH}	—	500	—	310	—	310	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.5	1.3	0.5	1.5	0.55	1.55	ns
Rise Time	t_r	0.5	1.7	0.5	1.8	0.55	1.9	ns
Fall Time	t_f	0.5	1.7	0.5	1.8	0.55	1.9	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

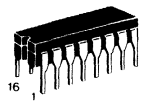
MOTOROLA

MC10H107

TRIPLE 2-INPUT EXCLUSIVE "OR"/EXCLUSIVE "NOR"

The MC10H107 is a triple 2-input exclusive OR/NOR gate. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 35 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



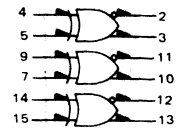
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

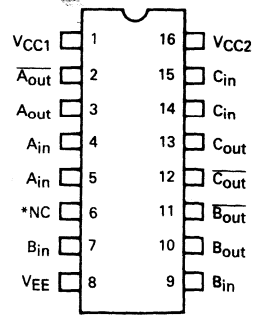
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	31	—	28	—	31	mA
Input Current High	I_{inH}	—	425	—	265	—	265	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.4	1.5	0.4	1.6	0.4	1.7	ns
Rise Time	t_r	0.5	1.5	0.5	1.6	0.5	1.7	ns
Fall Time	t_f	0.5	1.5	0.5	1.6	0.5	1.7	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

*NC = No Connection

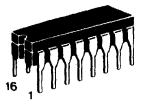
MOTOROLA

MC10H109

DUAL 4-5-INPUT "OR/NOR" GATE

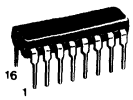
The MC10H109 is a dual 4-5-input OR/NOR gate. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 35 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

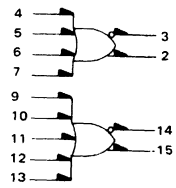
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	15	—	14	—	15	mA
Input Current High	I_{inH}	—	425	—	265	—	265	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.4	1.3	0.4	1.3	0.45	1.45	ns
Rise Time	t_r	0.5	2.0	0.5	2.1	0.5	2.2	ns
Fall Time	t_f	0.5	2.0	0.5	2.1	0.5	2.2	ns

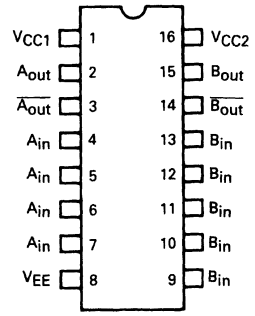
NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

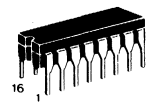
MOTOROLA

MC10H113

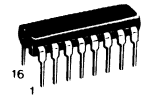
QUAD EXCLUSIVE OR GATE

The MC10H113 is a Quad Exclusive OR Gate with an enable common to all four gates. The outputs may be wire-ORed together to perform a 4-bit comparison function (A = B). The enable is active LOW.

- Propagation Delay, 1.3 ns Typical
- Power Dissipation 175 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

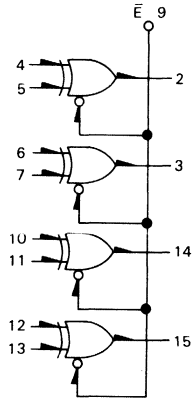
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	46	—	42	—	46	mA
Input Current High	I_{inH}							μA
Pins 5, 7, 11, 13		—	430	—	270	—	270	
Pins 4, 6, 10, 12		—	510	—	320	—	320	
Pin 9		—	1100	—	740	—	740	
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}							ns
Data		0.4	1.7	0.4	1.8	0.5	1.9	
Enable		0.5	2.3	0.5	2.4	0.6	2.5	
Rise Time	t_r	0.5	1.8	0.6	1.9	0.6	2.0	ns
Fall Time	t_f	0.5	1.8	0.6	1.9	0.6	2.0	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM



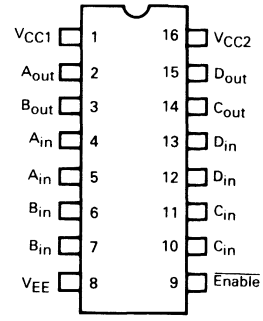
TRUTH TABLE

IN		Ē	OUTPUT
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
ϕ	ϕ	H	L

ϕ = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MOTOROLA

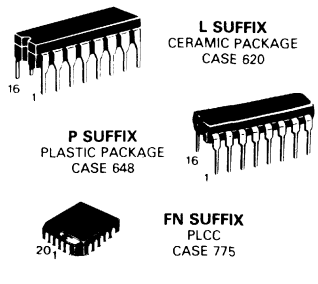
MC10H115

QUAD LINE RECEIVER

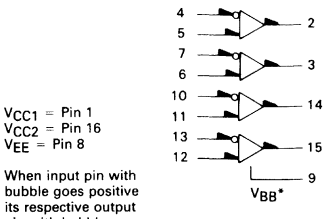
The MC10H115 is a quad differential amplifier designed for use in sensing differential signals over long lines. This 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in counting frequency and no increase in power-supply current.

The base bias supply (V_{BB}) is made available at Pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary. Active current sources provide the MC10H115 with excellent common mode rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (Pin 9) to prevent upsetting the current source bias network.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 110 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

When input pin with bubble goes positive its respective output pin with bubble goes positive.

*V_{BB} to be used to supply bias to the MC10H115 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

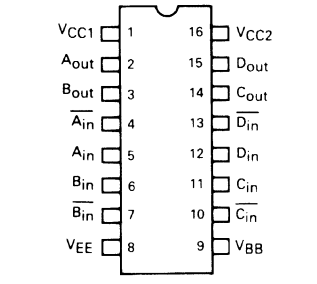
The MC10H115 is designed to be used in sensing differential signals over long lines. The bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide these receivers with excellent common-mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent unbalancing the current-source bias network.

The MC10H115 does not have internal-input pull-down resistors. This provides high impedance to the amplifier input and facilitates differential connections.

Applications:
- Low Level Receiver
- Voltage Level Interface
- Schmitt Trigger

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (2)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	29	—	26	—	29	mA
Input Current High	I_{inH}	—	150	—	95	—	95	μA
Input Leakage Current	I_{CBO}	—	1.5	—	1.0	—	1.0	μA
Reference Voltage	V_{BB}	−1.38	−1.27	−1.35	−1.25	−1.31	−1.19	Vdc
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage (1)	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage (1)	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc
Common Mode Range (3)	V_{CMR}	—	—	−2.85 to −0.8		—	—	Vdc
Input Sensitivity (4)	V_{PP}	—	—	150 typ		—	—	mV_{PP}

AC PARAMETERS

Propagation Delay	t_{pd}	0.4	1.3	0.4	1.3	0.45	1.45	ns
Rise Time	t_r	0.5	1.4	0.5	1.5	0.5	1.6	ns
Fall Time	t_f	0.5	1.4	0.5	1.5	0.5	1.6	ns

NOTES:
1. When V_{BB} is used as the reference voltage.
2. Each MECL 10H series circuit has been designed to meet the specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
3. Differential input not to exceed 1.0 Vdc.
4. 150 mV_{p-p} differential input required to obtain full logic swing on output.

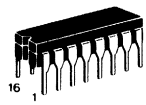
MOTOROLA

MC10H116

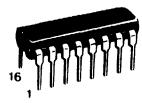
TRIPLE LINE RECEIVER

The MC10H116 is a functional/pinout duplication of the MC10116, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 85 mW Typ/Pkg (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

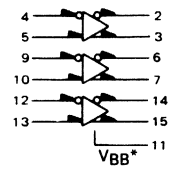


P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

When input pin with bubble goes positive it's respective output pin with bubble goes positive.

*V_{BB} to be used to supply bias to the MC10H116 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

The MC10H116 is designed to be used in sensing differential signals over long lines. The bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide these receivers with excellent common-mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent unbalancing the current-source bias network.

The MC10H116 does not have internal-input pull-down resistors. This provides high impedance to the amplifier input and facilitates differential connections.

Applications:
- Low Level Receiver
- Schmitt Trigger
- Voltage Level Interface

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (2)

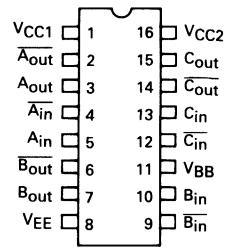
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	23	—	21	—	23	mA
Input Current High	I_{inH}	—	150	—	95	—	95	μA
Input Leakage Current	I_{CBO}	—	1.5	—	1.0	—	1.0	μA
Reference Voltage	V_{BB}	−1.38	−1.27	−1.35	−1.25	−1.31	−1.19	Vdc
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage (1)	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage (1)	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc
Common Mode Range (3)	V_{CMR}	—	—	−2.85 to −0.8		—	—	Vdc
Input Sensitivity (4)	V_{PP}	—	—	150 typ		—	—	mV_{PP}

AC PARAMETERS

Propagation Delay	t_{pd}	0.4	1.3	0.4	1.3	0.45	1.45	ns
Rise Time	t_r	0.5	1.5	0.5	1.6	0.5	1.7	ns
Fall Time	t_f	0.5	1.5	0.5	1.6	0.5	1.7	ns

NOTES:
1. When V_{BB} is used as the reference voltage.
2. Each MECL 10H series circuit has been designed to meet the specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
3. Differential input not to exceed 1.0 Vdc.
4. 150 mV_{p-p} differential input required to obtain full logic swing on output.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

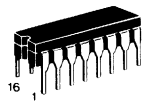
MOTOROLA

MC10H117

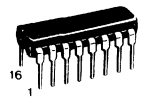
DUAL 2-WIDE 2-3-INPUT "OR-AND/OR-AND-INVERT" GATE

The MC10H117 is a general purpose logic element designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 100 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

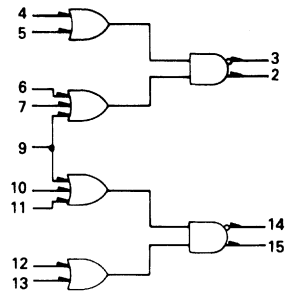
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	29	—	26	—	29	mA
Input Current High	I_{inH}							μA
Pins 4, 5, 12, 13		—	465	—	275	—	275	
Pins 6, 7, 10, 11		—	545	—	320	—	320	
Pin 9		—	710	—	415	—	415	
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.45	1.35	0.45	1.35	0.5	1.5	ns
Rise Time	t_r	0.5	1.5	0.5	1.6	0.5	1.7	ns
Fall Time	t_f	0.5	1.5	0.5	1.6	0.5	1.7	ns

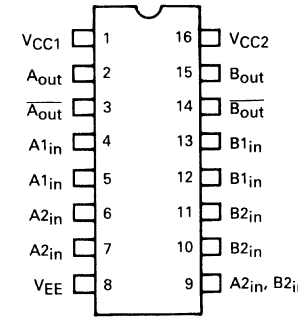
NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

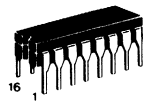
MOTOROLA

MC10H118

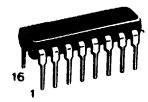
DUAL 2-WIDE 3-INPUT "OR-AND" GATE

The MC10H118 is a basic logic building block providing the OR/AND function, useful in data control and digital multiplexing applications.[1a] This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 100 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

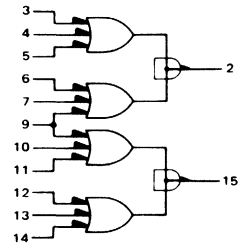


P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

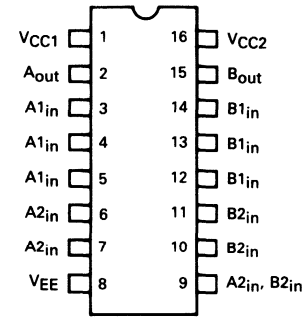
2

LOGIC DIAGRAM



2 = (3 + 4 + 5) • (6 + 7 + 9)
15 = (9 + 10 + 11) • (12 + 13 + 14)
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	29	—	26	—	29	mA
Input Current High Pins 3,4,5,12,13,14 Pins 6,7,10,11 Pin 9	I_{inH}	 — — —	 465 545 710	 — — —	 275 320 415	 — — —	 275 320 415	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage (1)	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage (1)	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.5	1.6	0.5	1.7	0.55	1.85	ns
Rise Time	t_r	0.5	1.5	0.5	1.6	0.5	1.7	ns
Fall Time	t_f	0.5	1.5	0.5	1.6	0.5	1.7	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

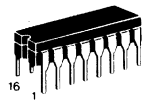
MOTOROLA

MC10H119

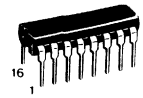
4-WIDE 4-3-3-3-INPUT "OR-AND" GATE

The MC10H119 is a 4-wide 4-3-3-3-input OR/AND gate with one input from two gates common to pin 10. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 100 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

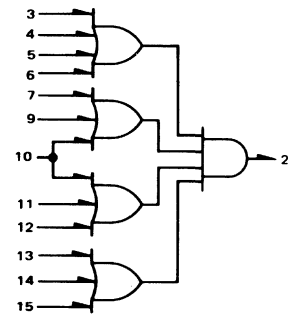


P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

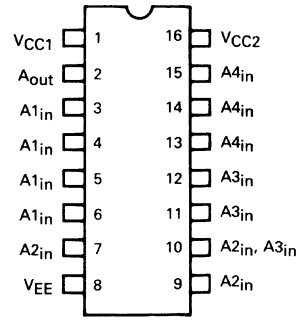
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	29	—	26	—	29	mA
Input Current High Pins 3, 4, 5, 6, 7, 9 11, 12, 13, 14, 15 Pin 10	I_{inH}	 — —	 500 610	 — —	 295 360	 — —	 295 360	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Pin 10 Only Exclude Pin 10	t_{pd}	 0.75 0.75	 2.2 2.0	 0.75 0.75	 2.25 2.0	 0.8 0.8	 2.35 2.15	ns
Rise Time	t_r	0.8	1.9	0.8	2.0	0.8	2.1	ns
Fall Time	t_f	0.8	1.9	0.8	2.0	0.8	2.1	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

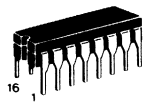
MOTOROLA

MC10H121

4-WIDE "OR-AND/OR-AND-INVERT" GATE

The MC10H121 is a basic logic building block providing the simultaneous OR-AND/OR-AND-INVERT function, useful in data control and digital multiplexing applications. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 100 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

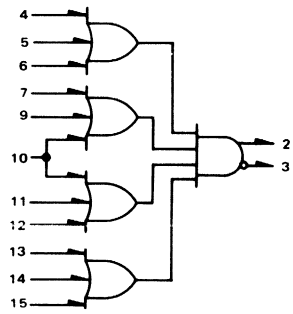
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	29	—	26	—	29	mA
Input Current High Pins 3, 4, 5, 6, 7, 9 11, 12, 13, 14, 15 Pin 10	I_{inH}	 — —	 500 610	 — —	 295 360	 — —	 295 360	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Pin 10 Only Exclude Pin 10	t_{pd}	 0.45 0.55	 1.8 1.95	 0.45 0.6	 1.8 2.0	 0.55 0.7	 2.2 2.4	ns
Rise Time	t_r	0.5	1.7	0.5	1.8	0.5	1.9	ns
Fall Time	t_f	0.5	1.7	0.5	1.8	0.5	1.9	ns

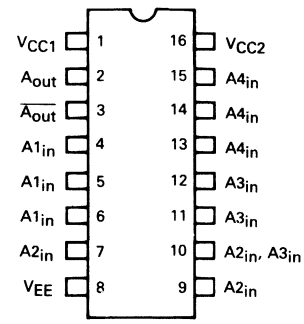
NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MOTOROLA

MC10H123

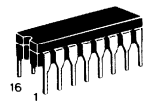
TRIPLE 4-3-3 INPUT BUS DRIVER

The MC10H123 is a triple 4-3-3 Input Bus Driver.

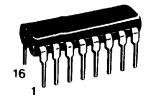
The MC10H123 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with V_{OL} = −2.1 Vdc so that the bus may be terminated to −2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10H123 are "turned-off." This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to −2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10H123, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 1.

- Propagation Delay, 1.5 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



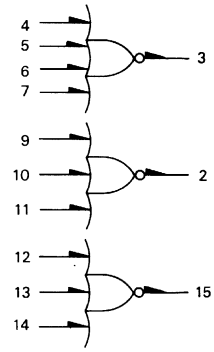
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

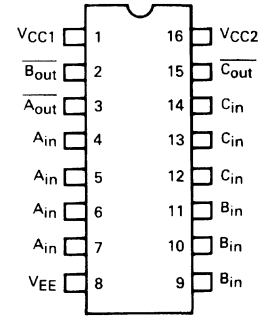
FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

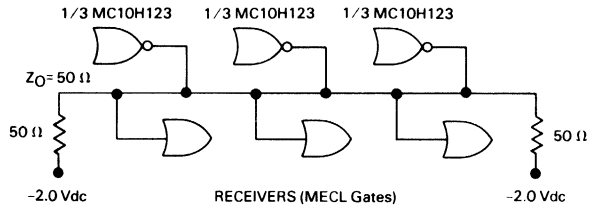
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	60	—	56	—	60	mA
Input Current High	I_{inH}	—	495	—	310	—	310	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−2.1	−2.03	−2.1	−2.03	−2.1	−2.03	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.7	1.5	0.7	1.6	0.7	1.7	ns
Rise Time	t_r	0.7	1.6	0.7	1.7	0.7	1.8	ns
Fall Time	t_f	0.7	1.6	0.7	1.7	0.7	1.8	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.1 volts.

FIGURE 1 — 50-OHM BUS DRIVER (25-OHM LOAD)



MOTOROLA

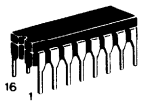
MC10H124

QUAD TTL-TO-MECL TRANSLATOR WITH TTL STROBE INPUT

The MC10H124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

Outputs of unused translators will go to low state when their inputs are left open.

- Propagation Delay, 1.5 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

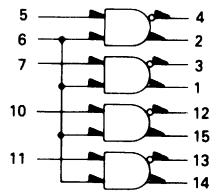


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

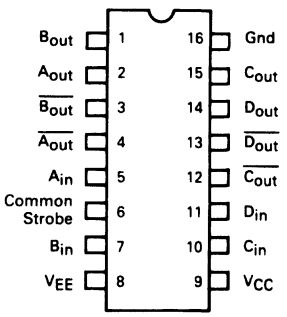
FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (−5.2 Vdc) = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 5.0 V)	V_{EE}	−8.0 to 0	Vdc
Power Supply (V_{EE} = −5.2 V)	V_{CC}	0 to +7.0	Vdc
Input Voltage (V_{CC} = 5.0 V) TTL	V_I	0 to V_{CC}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%, V_{CC} = 5.0 V ± 5.0%)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Negative Power Supply Drain Current	I_E	—	72	—	66	—	72	mA
Positive Power Supply Drain Current	I_{CCH}	—	16	—	16	—	18	mA
	I_{CCL}	—	25	—	25	—	25	mA
Reverse Current Pin 6 Pin 7	I_R	 — —	 200 50	 — —	 200 50	 — —	 200 50	μA
Forward Current Pin 6 Pin 7	I_F	 — —	 −12.8 −3.2	 — —	 −12.8 −3.2	 — —	 −12.8 −3.2	mA
Input Breakdown Voltage	$V_{(BR)in}$	5.5	—	5.5	—	5.5	—	Vdc
Input Clamp Voltage	V_I	—	−1.5	—	−1.5	—	−1.5	Vdc
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	2.0	—	2.0	—	2.0	—	Vdc
Low Input Voltage	V_{IL}	—	0.8	—	0.8	—	0.8	Vdc

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%, V_{CC} = 5.0 V ± 5.0%)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
AC PARAMETERS								
Propagation Delay	t_{pd}	0.55	2.25	0.55	2.4	0.85	2.95	ns
Rise Time	t_r	0.5	1.5	0.5	1.6	0.5	1.7	ns
Fall Time	t_f	0.5	1.5	0.5	1.6	0.5	1.7	ns

APPLICATIONS INFORMATION

The MC10H124 has TTL-compatible inputs and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low-logic level, it forces all true outputs to a MECL low-logic state and all inverting outputs to a MECL high-logic state.

An advantage of this device is that TTL-level information can be transmitted differentially, via balanced twisted pair lines, to MECL equipment, where the signal can be received by the MC10H115 or MC10H116 differential line receivers. The power supply requirements are ground, +5.0 volts, and −5.2 volts.

MOTOROLA

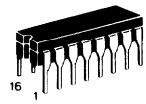
MC10H125

QUAD MECL-TO-TTL TRANSLATOR

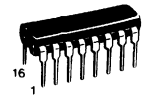
The MC10H125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic section of digital systems. The 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

Outputs of unused translators will go to low state when their inputs are left open.

- Propagation Delay, 2.5 ns Typical
- Voltage Compensated
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 5.0 V)	V_{EE}	−8.0 to 0	Vdc
Power Supply (V_{EE} = −5.2 V)	V_{CC}	0 to +7.0	Vdc
Input Voltage (V_{CC} = 5.0 V)	V_I	0 to V_{EE}	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%; V_{CC} = 5.0 V ± 5.0%) (See Note)

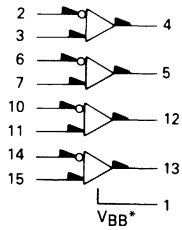
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Negative Power Supply Drain Current	I_E	—	44	—	40	—	44	mA
Positive Power Supply Drain Current	I_{CCH}	—	63	—	63	—	63	mA
	I_{CCL}	—	40	—	40	—	40	mA
Input Current	I_{inH}	—	225	—	145	—	145	μA
Input Leakage Current	I_{CBO}	—	1.5	—	1.0	—	1.0	μA
High Output Voltage I_{OH} = −1.0 mA	V_{OH}	2.5	—	2.5	—	2.5	—	Vdc
Low Output Voltage I_{OL} = +20 mA	V_{OL}	—	0.5	—	0.5	—	0.5	Vdc
High Input Voltage(1)	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage(1)	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc
Short Circuit Current	I_{OS}	60	150	60	150	50	150	mA
Reference Voltage	V_{BB}	−1.38	−1.27	−1.35	−1.25	−1.31	−1.19	Vdc
Common Mode Range (3)	V_{CMR}	—	—	−2.85 to −0.3				V
		Typical						
Input Sensitivity (4)	V_{PP}	150						mV

AC PARAMETERS

Propagation Delay	t_{pd}	0.8	3.3	0.85	3.35	0.9	3.4	ns
Rise Time(5)	t_r	0.3	1.2	0.3	1.2	0.3	1.2	ns
Fall Time(5)	t_f	0.3	1.2	0.3	1.2	0.3	1.2	ns

NOTES:
1. When V_{BB} is used as the reference voltage.
2. Each MECL 10H series circuit has been designed to meet the specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
3. Differential input not to exceed 1.0 Vdc.
4. 150 mV_{p-p} differential input required to obtain full logic swing on output.
5. 1.0 V to 2.0 V w/25 pF into 500 Ω.

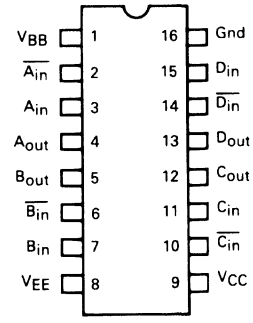
LOGIC DIAGRAM



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (−5.2 Vdc) = Pin 8

*V_{BB} to be used to supply bias to the MC10H125 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

APPLICATION INFORMATION

The MC10H125 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on Pin 1 for use in single-ended input biasing. The outputs of the MC10H125 go to a low-logic level whenever the inputs are left floating, and a high-logic output level is achieved with a minimum input level of 150 mV_{p-p}.

An advantage of this device is that MECL-level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL-logic from the noisy TTL environment. Power supply requirements are ground, +5.0 volts and −5.2 volts.

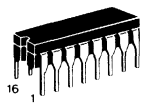
MOTOROLA

MC10H130

DUAL LATCH

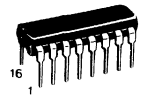
The MC10H130 is a MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 155 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

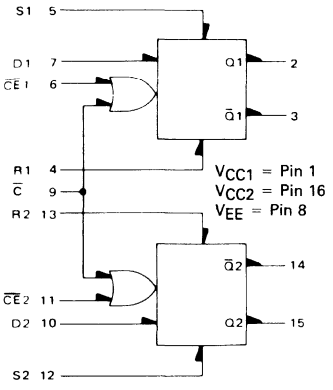
Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	I_E	—	38	—	35	—	38	mA
Input Current High Pins 6, 11 Pins 7, 9, 10 Pins 4, 5, 12, 13	I_{inH}	 — — —	 468 545 434	 — — —	 275 320 255	 — — —	 275 320 255	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Data Set, Reset Clock, $\overline{CE}$	t_{pd}	 0.4 0.6 0.5	 1.6 1.7 1.6	 0.4 0.7 0.5	 1.7 1.8 1.7	 0.4 0.8 0.6	 1.8 1.9 1.8	ns
Rise Time	t_r	0.5	1.6	0.5	1.7	0.5	1.8	ns
Fall Time	t_f	0.5	1.6	0.5	1.7	0.5	1.8	ns
Set-up Time	t_{set}	2.2	—	2.2	—	2.2	—	ns
Hold Time	t_{hold}	0.7	—	0.7	—	0.7	—	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM

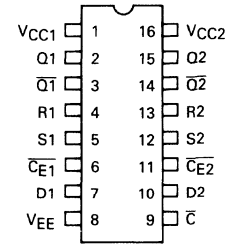


TRUTH TABLE

D	$\overline{C}$	$\overline{CE}$	Q_{n+1}
L	L	L	L
H	L	L	H
Φ	L	H	Q_n
Φ	H	L	Q_n
Φ	H	H	Q_n

Φ = Don't Care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

APPLICATION INFORMATION

The MC10H130 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\overline{C}$).

Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

The set and reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

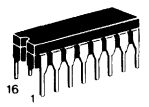
MOTOROLA

MC10H131

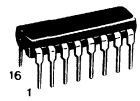
DUAL TYPE D MASTER-SLAVE FLIP-FLOP

The MC10H131 is a MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 235 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

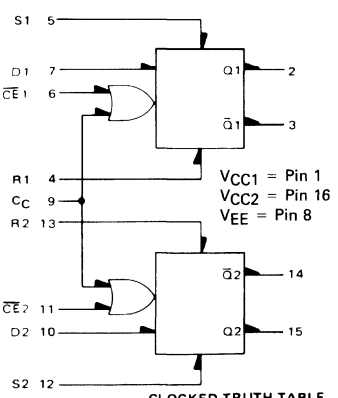
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	62	—	56	—	62	mA
Input Current High Pins 6, 11 Pin 9 Pins 7, 10 Pins 4, 5, 12, 13	I_{inH}	 — — — —	 530 660 485 790	 — — — —	 310 390 285 465	 — — — —	 310 390 285 465	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Clock, $\overline{CE}$ Set, Reset	t_{pd}	 0.8 0.6	 1.6 1.6	 0.8 0.7	 1.7 1.7	 0.8 0.7	 1.8 1.8	ns
Rise Time	t_r	0.6	2.0	0.6	2.0	0.6	2.2	ns
Fall Time	t_f	0.6	2.0	0.6	2.0	0.6	2.2	ns
Set-up Time	t_{set}	0.7	—	0.7	—	0.7	—	ns
Hold Time	t_{hold}	0.8	—	0.8	—	0.8	—	ns
Toggle Frequency	f_{tog}	250	—	250	—	250	—	MHz

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM



R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

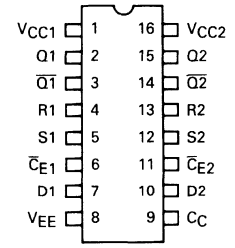
N.D. = Not Defined

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

ϕ = Don't Care
$C = \overline{C}_E + C_C$
A clock H is a clock transition from a low to a high state.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

APPLICATION INFORMATION

The MC10H131 is a dual master-slave type D flip-flop. Asynchronous Set ($\overline{S}$) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the new low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

MOTOROLA

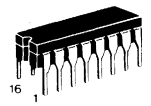
MC10H135

DUAL J-K MASTER SLAVE FLIP-FLOP

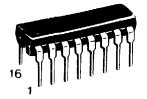
The MC10H135 is a dual J-K master slave flip-flop. The device is provided with an asynchronous set(s) and reset(R). These set and reset inputs overide the clock.

A common clock is provided with separate $\overline{J}$-$\overline{K}$ inputs. When the clock is static, the $\overline{JK}$ inputs do not effect the output. The output states of the flip flop change on the positive transition of the clock.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 280 mW Typical/Pkg. (No Load)
- f_{tog} 250 MHz Max
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

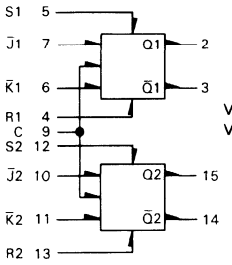
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	75	—	68	—	75	mA
Input Current High Pins 6, 7, 10, 11 Pins 4, 5, 12, 13 Pin 9	I_{inH}	 — — —	 460 800 675	 — — —	 285 500 420	 — — —	 285 500 420	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Set, Reset, Clock	t_{pd}	0.7	2.6	0.7	2.6	0.7	2.6	ns
Rise Time	t_r	0.7	2.2	0.7	2.2	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.2	0.7	2.2	ns
Set-up Time	t_{set}	1.5	—	1.5	—	1.5	—	ns
Hold Time	t_{hold}	1.0	—	1.0	—	1.0	—	ns
Toggle Frequency	f_{tog}	—	250	—	250	—	250	MHz

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM



R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

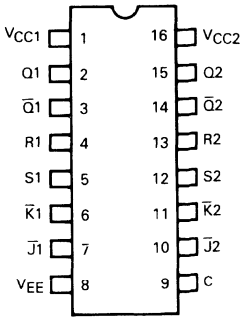
N.D. = Not Defined

CLOCK J-K TRUTH TABLE*

$\overline{J}$	$\overline{K}$	Q_{n+1}
L	L	$\overline{Q_n}$
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transition of clock for $\overline{J}$-$\overline{K}$ input condition present.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

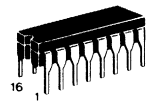
MOTOROLA

MC10H136

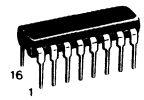
UNIVERSAL HEXADECIMAL COUNTER

The MC10H136 is a high speed synchronous hexadecimal counter. This 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in counting frequency and no increase in power-supply current.

- Counting Frequency, 250 MHz Minimum
- Power Dissipation, 625 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

FUNCTION SELECT TABLE

$\overline{CIN}$	S1	S2	Operating Mode
ϕ	L	L	Preset (Program)
L	L	H	Increment (Count Up)
H	L	H	Hold Count
L	H	L	Decrement (Count Down)
H	H	L	Hold Count
ϕ	H	H	Hold (Stop Count)

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	I_E	—	165	—	150	—	165	mA
Input Current High Pins 5, 6, 11, 12, 13 Pin 9 Pin 7 Pin 10	I_{inH}	 — — — —	 430 670 535 380	 — — — —	 275 420 335 240	 — — — —	 275 420 335 240	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{Carry\ In}$	Clock **	Q0	Q1	Q2	Q3	$\overline{Carry\ Out}$
L	L	L	L	H	H	ϕ	H	L	L	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	H	ϕ	L	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	H	ϕ	H	H	H	H	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	H
H	H	L	L	L	L	L	H	L	L	L	L	H
H	H	L	L	L	L	L	H	H	L	L	L	H
H	H	L	L	L	L	H	ϕ	L	H	L	L	H
H	H	L	L	L	L	H	ϕ	H	H	L	L	H
H	H	H	H	H	H	L	H	L	H	L	L	H
H	H	H	H	H	H	L	H	H	H	L	L	H
H	H	H	H	H	H	H	ϕ	L	H	L	L	H
H	H	H	H	H	H	H	ϕ	H	H	L	L	H

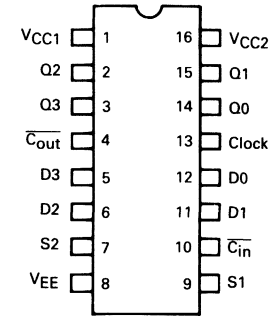
ϕ = Don't care
* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
** A clock H is defined as a clock input transition from a low to a high logic level.

AC PARAMETERS

		0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	
Propagation Delay Clock to Q Clock to Carry Out Carry in to Carry Out	t_{pd}	 0.7 1.0 0.7	 2.3 4.8 2.5	 0.7 1.0 0.7	 2.4 4.9 2.6	 0.7 1.0 0.7	 2.5 5.0 2.7	ns
Set-up Time Data (D0 to C) Select (S to C) Carry In (C_{in} to C) (C to C_{in})	t_{set}	 2.0 3.5 2.0 0	 — — — —	 2.0 3.5 2.0 0	 — — — —	 2.0 3.5 2.0 0	 — — — —	ns
Hold Time Data (C to D0) Select (C to S) Carry In (C to C_{in}) (C_{in} to C)	t_{hold}	 0 −0.5 0 2.2	 — — — —	 0 −0.5 0 2.2	 — — — —	 0 −0.5 0 2.2	 — — — —	ns
Counting Frequency	f_{count}	250	—	250	—	250	—	MHz
Rise Time	t_r	0.5	2.3	0.5	2.4	0.5	2.5	ns
Fall Time	t_f	0.5	2.3	0.5	2.4	0.5	2.5	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

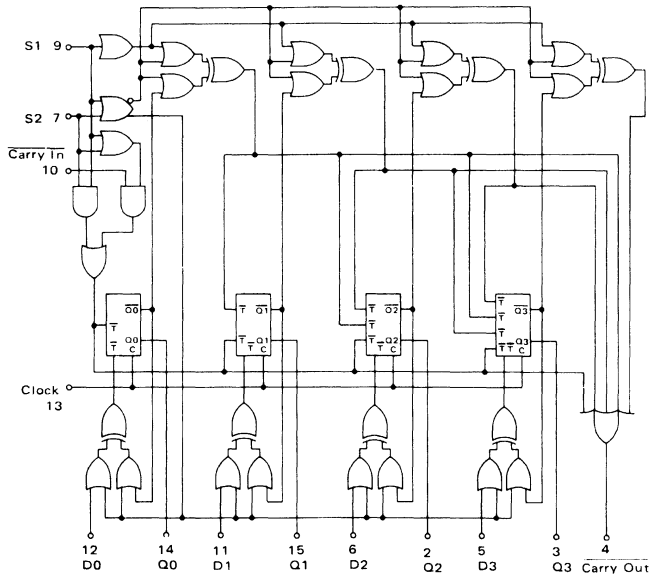
DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

2

LOGIC DIAGRAM



NOTE: FLIP FLOPS WILL TOGGLE WHEN ALL $\overline{T}$ INPUTS ARE LOW.

APPLICATION INFORMATION

The MC10H136 is a high speed synchronous counter that operates at 250 MHz. Counter operating modes include count up, count down, pre-set and hold count. This device allows the designer to use one basic counter for many applications.

The S1, S2, control lines determine the operating modes of the counter. In the pre-set mode, a clock pulse is necessary to load the counter with the information present on the data inputs (D0, D1, D2, and D3). Carry out goes low on the terminal count or when the counter is being pre-set.

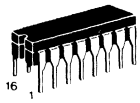
MOTOROLA

MC10H141

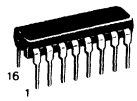
FOUR-BIT UNIVERSAL SHIFT REGISTER

The MC10H141 is a four-bit universal shift register. This device is a functional/pinout duplication of the standard MECL 10K part with 100% improvement in propagation delay and operation frequency and no increase in power supply current.

- Shift frequency, 250 MHz Min
- Power Dissipation, 425 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	112	—	102	—	112	mA
Input Current High Pins 5,6,9,11,12,13 Pins 7,10 Pin 4	I_{inH}	 — — —	 405 416 510	 — — —	 255 260 320	 — — —	 255 260 320	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	1.0	2.0	1.0	2.0	1.1	2.1	ns
Hold Time — Data, Select	t_{hold}	1.0	—	1.0	—	1.0	—	ns
Set-up Time Data Select	t_{set}	 1.5 3.0	 — —	 1.5 3.0	 — —	 1.5 3.0	 — —	ns
Rise Time	t_r	0.5	2.4	0.5	2.4	0.5	2.4	ns
Fall Time	t_f	0.5	2.4	0.5	2.4	0.5	2.4	ns
Shift Frequency	f_{shift}	250	—	250	—	250	—	MHz

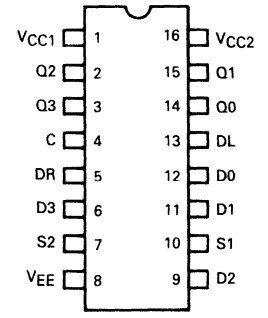
NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

TRUTH TABLE

SELECT		OPERATING	OUTPUTS			
S1	S2	MODE	$Q0_{n+1}$	$Q1_{n+1}$	$Q2_{n+1}$	$Q3_{n+1}$
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	$Q1_n$	$Q2_n$	$Q3_n$	DR
H	L	Shift Left*	DL	$Q0_n$	$Q1_n$	$Q2_n$
H	H	Stop Shift	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$

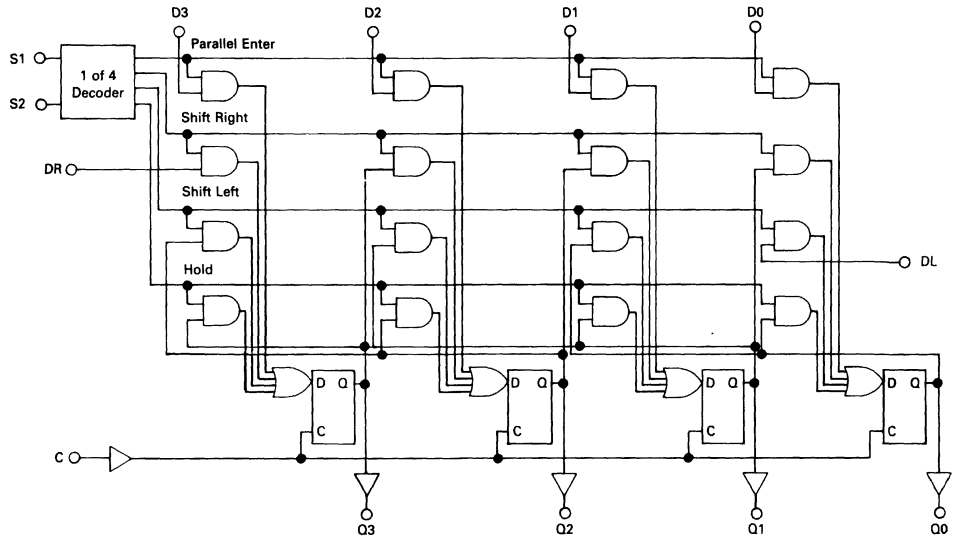
* Outputs as exist after pulse appears at "C" input with input conditions as shown (Pulse Positive transition of clock input).

DIP
PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

APPLICATION INFORMATION

The MC10H141 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

MOTOROLA

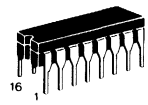
MC10H145

16 x 4 BIT REGISTER FILE (RAM)

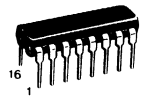
The MC10H145 is a 16 x 4 bit register file. The active-low chip select allows easy expansion.

The operating mode of the register file is controlled by the $\overline{WE}$ input. When $\overline{WE}$ is "low" the device is in the write mode, the outputs are "low" and the data present at D_n input is stored at the selected address, when $\overline{WE}$ is "high," the device is in the read mode — the data state at the selected location is present at the Q_n outputs.

- Address Access Time, 4.5 ns Typical
- Power Dissipation, 700 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ± 5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	160	—	163	—	165	mA
Input Current High	I_{inH}	—	375	—	220	—	220	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

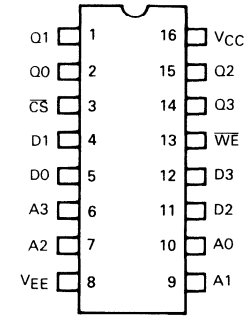
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care

Q-State of Addressed Cell

DIP PIN ASSIGNMENT



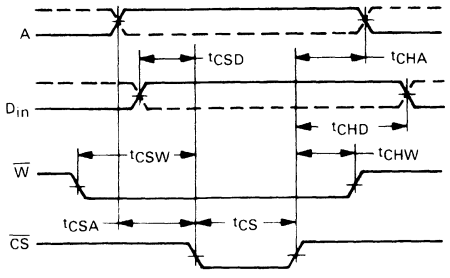
Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

AC PARAMETERS

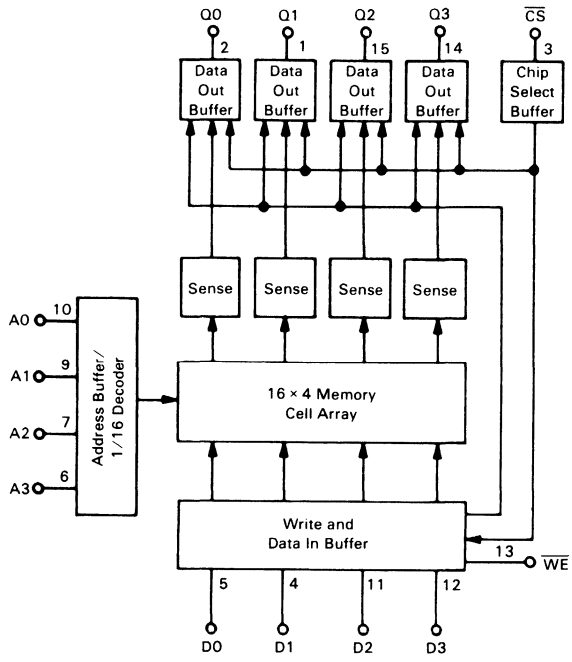
Characteristics	Symbol	MC10H145 T_A = 0 to +75°C, V_{EE} = -5.2 Vdc ±5% Min	Max	Unit	Conditions
Read Mode				ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	0	4.0		
Chip Select Recovery Time	t_{RCS}	0	4.0		
Address Access Time	t_{AA}	0	6.0		
Write Mode				ns	t_{WSA} = 3.5 ns Measured at 50% of input to 50% of output. t_W = 6.0 ns.
Write Pulse Width	t_W	6.0	—		
Data Setup Time Prior to Write	t_{WSD}	0	—		
Data Hold Time After Write	t_{WHD}	1.5	—		
Address Setup Time Prior to Write	t_{WSA}	3.5	—		
Address Hold Time After Write	t_{WHA}	1.5	—		
Chip Select Setup Time Prior to Write	t_{WSCS}	0	—		
Chip Select Hold Time After Write	t_{WHCS}	1.5	—		
Write Disable Time	t_{WS}	1.0	4.0		
Write Recovery Time	t_{WR}	1.0	4.0		
Chip Enable Strobe Mode				ns	Guaranteed but not tested on standard product. See Figure 1.
Data Setup Prior to Chip Select	t_{CSD}	0	—		
Write Enable Setup Prior to Chip Select	t_{CSW}	0	—		
Address Setup Prior to Chip Select	t_{CSA}	0	—		
Data Hold Time After Chip Select	t_{CHD}	1.0	—		
Write Enable Hold Time After Chip Select	t_{CHW}	0	—		
Address Hold Time After Chip Select	t_{CHA}	2.0	—		
Chip Select Minimum Pulse Width	t_{CS}	4.0	—		
Rise and Fall Time	t_r, t_f			ns	Measured between 20% and 80% points.
Address to Output		0.6	2.5		
CS to Output		0.6	2.5		
Capacitance				pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	6.0		
Output Capacitance	C_{out}	—	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MC10H145. $C_L \leq 5.0$ pF (including jig and Stray Capacitance). Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
3. For proper use of MECL in a system environment, consult MECL System Design Handbook.

FIGURE 1 — CHIP ENABLE STROBE MODE



BLOCK DIAGRAM



2

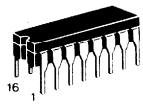
MOTOROLA

MC10H158

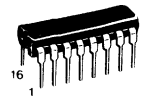
QUAD 2-INPUT MULTIPLEXER (NON-INVERTING)

The MC10H158 is a quad two channel multiplexer with common input select. A "high" level select enables input D00, D10, D20 and D30 and a "low" level select enables input D01, D11, D21 and D31. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 197 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

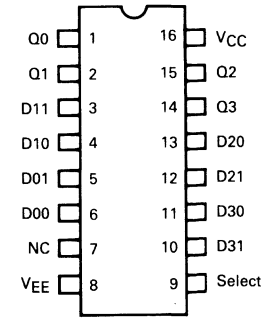
FN SUFFIX
PLCC
CASE 775

TRUTH TABLE

Select	D0	D1	Q
L	ϕ	L	L
L	ϕ	H	H
H	L	ϕ	L
H	H	ϕ	H

ϕ = Don't care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%)

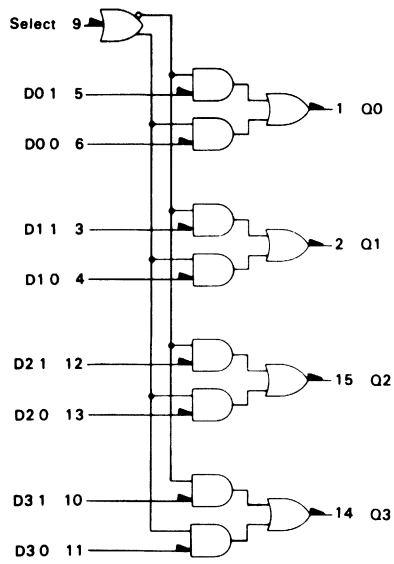
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	53	—	48	—	53	mA
Input Current High Pin 9 Pins 3–6 and 10–13	I_{inH}	 — —	 475 515	 — —	 295 320	 — —	 295 320	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Data Select	t_{pd}	 0.5 1.0	 1.9 2.9	 0.5 1.0	 1.9 2.9	 0.5 1.0	 2.0 2.9	ns
Rise Time	t_r	0.7	2.2	0.7	2.2	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.2	0.7	2.2	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM



V_{CC} = Pin 16
V_{EE} = Pin 8

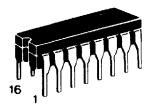
MOTOROLA

MC10H159

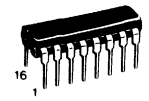
QUAD 2-INPUT MULTIPLEXER (INVERTING)

The MC10H159 is a quad 2-input multiplexer with enable. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 218 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

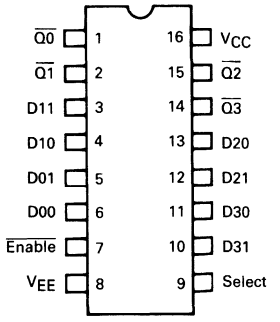
FN SUFFIX
PLCC
CASE 775

TRUTH TABLE

Enable	Select	D0	D1	Q
L	L	Φ	L	H
L	L	Φ	H	L
L	H	L	Φ	H
L	H	H	Φ	L
H	Φ	Φ	Φ	L

Φ = Don't Care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	58	—	53	—	58	mA
Input Current High Pin 9 Pins 3–7 and 10–13	I_{inH}	 — —	 475 515	 — —	 295 320	 — —	 295 320	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

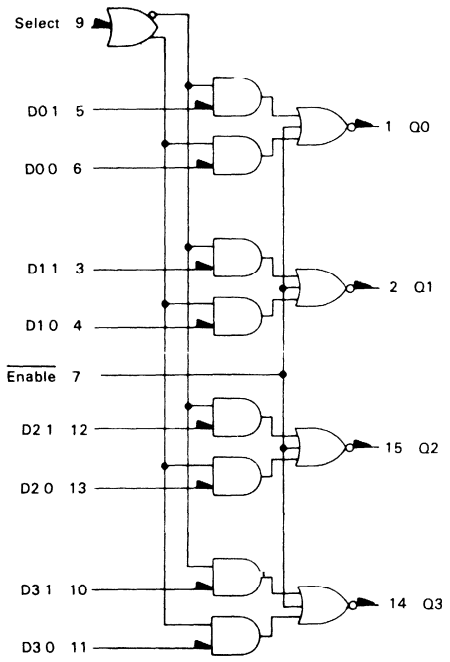
Propagation Delay Data Select Enable	t_{pd}	 0.5 1.0 1.0	 2.2 3.2 3.2	 0.5 1.0 1.0	 2.2 3.2 3.2	 0.5 1.0 1.0	 2.2 3.2 3.2	ns
Rise Time	t_r	0.5	2.2	0.5	2.2	0.5	2.2	ns
Fall Time	t_f	0.5	2.2	0.5	2.2	0.5	2.2	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

APPLICATION INFORMATION

The MC10H159 is a quad two channel multiplexer with enable. It incorporates common enable and common data select inputs. The select input determines which data inputs are enabled. A high (H) level enables data inputs D0 0, D1 0, D2 0, and D3 0. A low (L) level enables data inputs D0 1, D1 1, D2 1, and D3 1. Any change on the data inputs will be reflected at the outputs while the enable is low. Input levels are inverted at the output.

LOGIC DIAGRAM



V_{CC} Pin 16
V_{EE} Pin 8

2

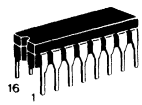
MOTOROLA

MC10H160

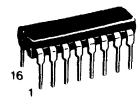
12-BIT PARITY GENERATOR-CHECKER

The MC10H160 is a 12-bit parity generator-checker. The output goes high when an odd number of inputs are high providing the odd parity function. Unconnected inputs are pulled to a logic low allowing parity detection and generation for less than 12 bits. The MC10H160 is a functional pin duplication of the standard 10K family part with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 2.5 ns Typical
- Power Dissipation, 320 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



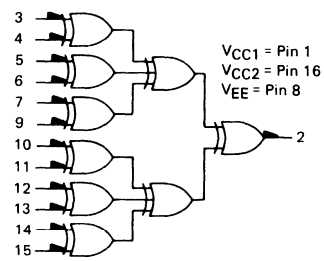
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

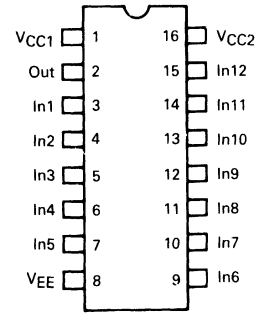
LOGIC DIAGRAM



TRUTH TABLE

INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–+75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	88	—	78	—	88	mA
Input Current High Pins 3,5,7,10,12,14 Pins 4,6,9,11,13,15	I_{inH}	 — —	 391 457	 — —	 246 285	 — —	 246 285	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	1.1	3.1	1.1	3.3	1.2	3.5	ns
Rise Time	t_r	0.55	1.5	0.55	1.6	0.75	1.7	ns
Fall Time	t_f	0.55	1.5	0.55	1.6	0.75	1.7	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

MOTOROLA

MC10H161

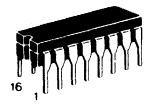
BINARY TO 1-8 DECODER (LOW)

The MC10H161 provides parallel decoding of a three bit binary word to one of eight lines. The MC10H161 is useful in high-speed multiplexer/demultiplexer applications.

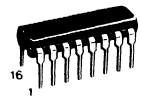
The MC10H161 is designed to decode a three bit input word to one of eight output lines. The MC10H161 output will be low when selected while all other output are high. The enable inputs, when either or both are high, force all outputs high.

The MC10H161 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. These devices are ideally suited for multiplexer/demultiplexer applications.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 315 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

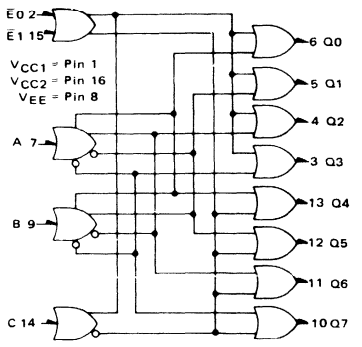
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	84	—	76	—	84	mA
Input Current High	I_{inH}	—	465	—	275	—	275	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}							ns
Data		0.6	2.0	0.65	2.1	0.7	2.2	
Enable		0.8	2.3	0.8	2.4	0.9	2.5	
Rise Time	t_r	0.55	1.7	0.65	1.8	0.7	1.9	ns
Fall Time	t_f	0.55	1.7	0.65	1.8	0.7	1.9	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM

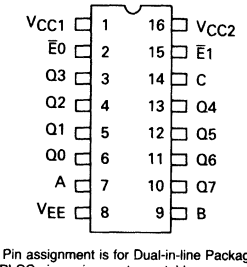


TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\bar{E}1$	$\bar{E}0$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	Φ	Φ	Φ	Φ	H	H	H	H	H	H	H	H
Φ	H	Φ	Φ	Φ	H	H	H	H	H	H	H	H

Φ = Don't Care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

TYPICAL APPLICATIONS

FIGURE 1 — HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER

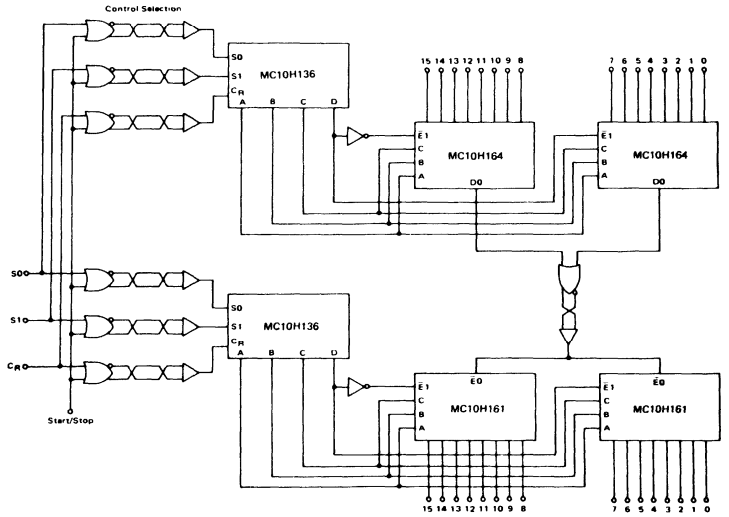
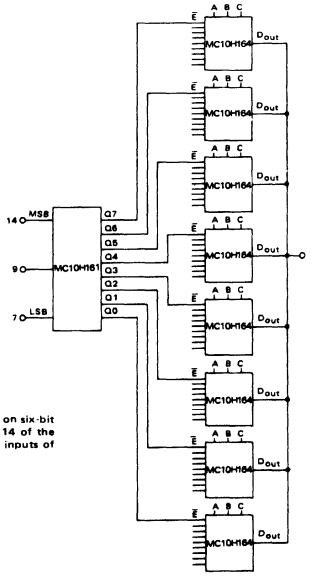


FIGURE 2 — 1-OF-64 LINE MULTIPLEXER



The Bit chosen is dependent on six-bit code present on inputs 7, 9, 14 of the MC10H161 and the A, B, C inputs of the MC10H164.

MOTOROLA

MC10H162

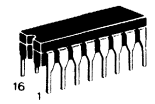
BINARY TO 1-8 DECODER (HIGH)

The MC10H162 provides parallel decoding of a three bit binary word to one of eight lines. The MC10H162 is useful in high-speed multiplexer/demultiplexer applications.

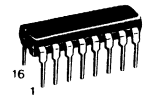
The MC10H162 is designed to decode a three bit input word to one of eight output lines. The MC10H162 output will be high when selected while all other output are low. The enable inputs, when either or both are high, force all outputs low.

The MC10H162 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. These devices are ideally suited for multiplexer/demultiplexer applications.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 315 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

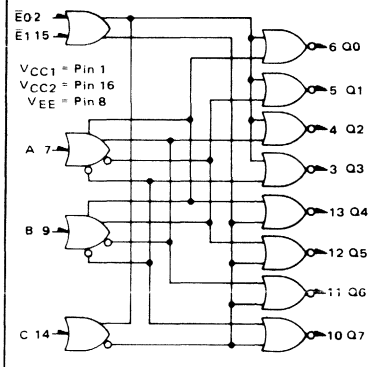
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	84	—	76	—	84	mA
Input Current High	I_{inH}	—	465	—	275	—	275	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Pins 7, 9, 14 Only Pins 2, 15 Only	t_{pd}	 0.7 0.8	 2.0 2.3	 0.7 0.8	 2.1 2.4	 0.8 0.9	 2.5 2.6	ns
Rise Time	t_r	0.6	1.8	0.6	1.9	0.6	2.0	ns
Fall Time	t_f	0.6	1.8	0.6	1.9	0.6	2.0	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM

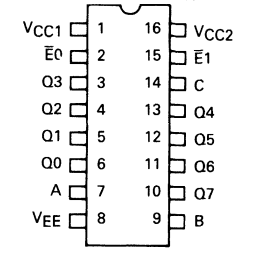


TRUTH TABLE

INPUTS					OUTPUTS						
E0	E1	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	Φ	Φ	Φ	Φ	L	L	L	L	L	L	L	L
Φ	H	Φ	Φ	Φ	L	L	L	L	L	L	L	L

Φ = Don't Care

DIP PIN ASSIGNMENT

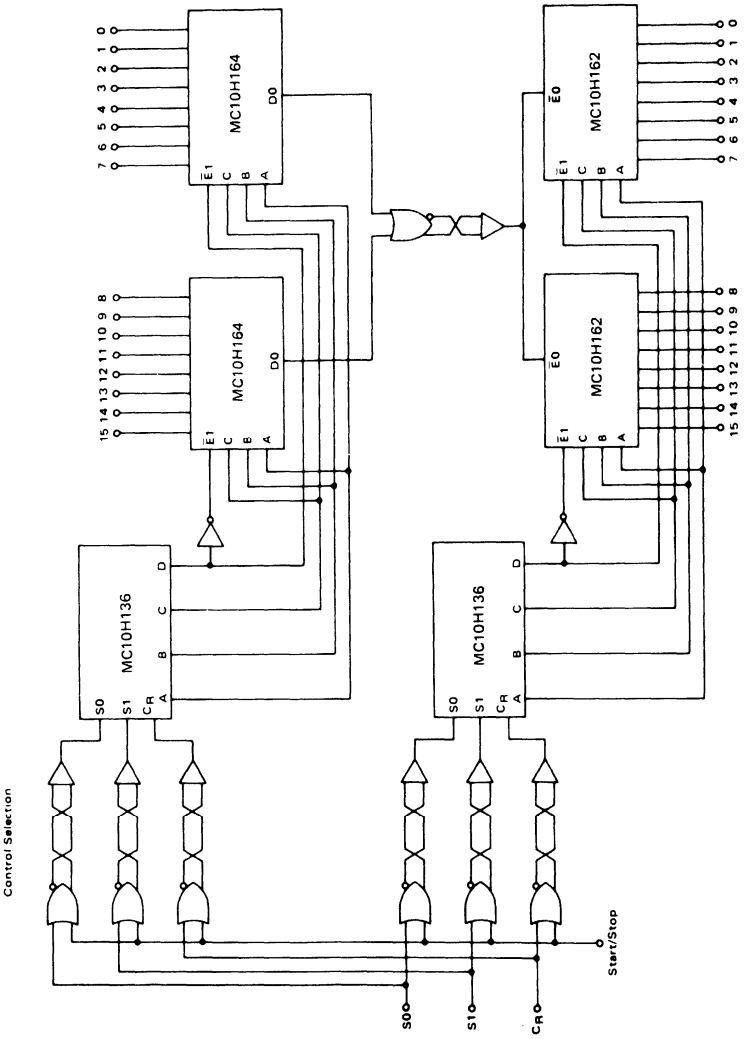


Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

2

TYPICAL APPLICATIONS

FIGURE 1 — HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER



MOTOROLA

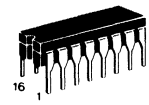
MC10H164

8-LINE MULTIPLEXER

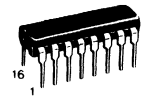
The MC10H164 is a MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power supply current.

The MC10H164 is designed to be used in data multiplexing and parallel to serial conversion applications. Full parallel gating provides equal delays through any data path. The MC10H164 incorporates an output buffer, eight inputs and an enable. A high on the enable forces the output low. The open emitter output allows the MC10H164 to be connected directly to a data bus. The enable line allows an easy means of expanding to more than 8 lines using additional MC10H164's.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 310 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

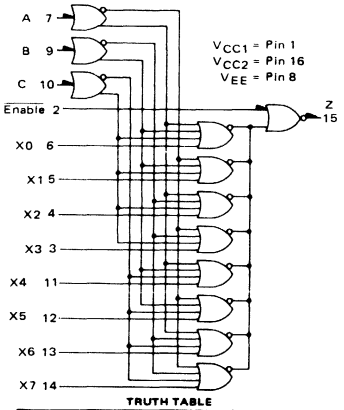
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	83	—	75	—	83	mA
Input Current High	I_{inH}	—	512	—	320	—	320	μA
Input Current Low	I_{inL}	0.7	—	0.7	—	0.7	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}							ns
Enable		0.4	1.45	0.4	1.5	0.5	1.7	
Data		0.7	2.4	0.8	2.5	0.9	2.6	
Address		1.0	2.8	1.1	2.9	1.2	3.2	
Rise Time	t_r	0.5	1.5	0.5	1.6	0.5	1.7	ns
Fall Time	t_f	0.5	1.5	0.5	1.6	0.5	1.7	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM

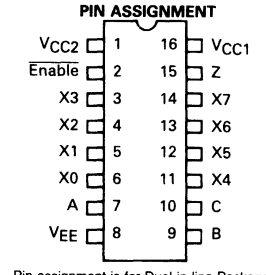


TRUTH TABLE

ENABLE	ADDRESS INPUTS C	B	A	Z
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	ϕ	ϕ	ϕ	L

ϕ = Don't Care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

TYPICAL APPLICATIONS

FIGURE 1 — HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER

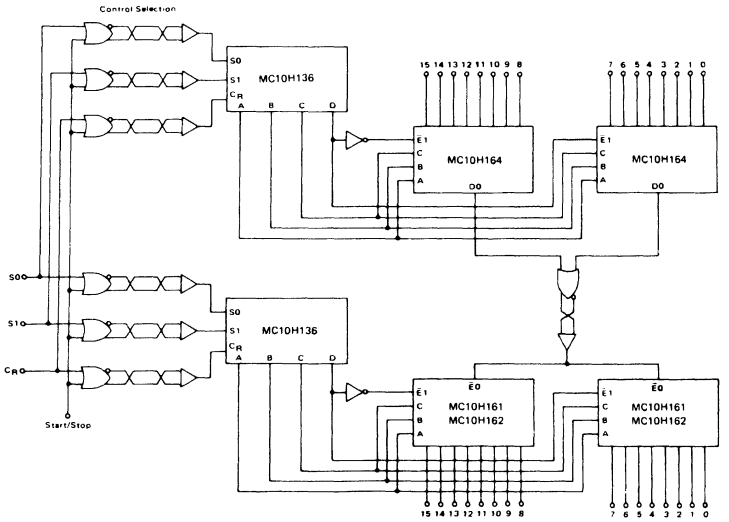
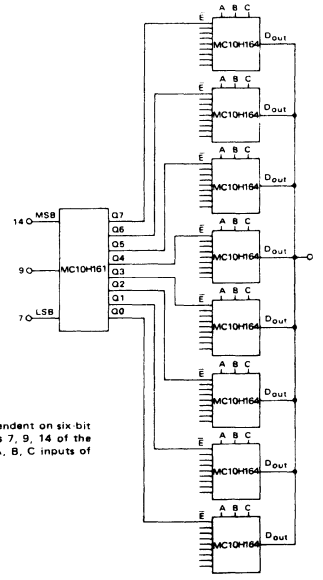


FIGURE 2 — 1-OF-64 LINE MULTIPLEXER



The Bit chosen is dependent on six bit code present on inputs 7, 9, 14 of the MC10H161 and the A, B, C inputs of the MC10H164.

MOTOROLA

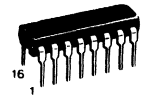
MC10H165

8-INPUT PRIORITY ENCODER

The MC10H165 is an 8-Input Priority Encoder. This 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power-supply current.

- Propagation Delay, Data-to-Output, 2.2 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	I_E	—	144	—	131	—	144	mA
Input Current High Pin 4 Data Inputs	I_{inH}	 — —	 510 600	 — —	 320 370	 — —	 320 370	μAdc
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Data Input → Output Clock Input → Output	t_{pd}	 0.7 0.7	 3.4 2.2	 0.7 0.7	 3.4 2.2	 0.7 0.7	 3.4 2.2	ns
Set-up Time	t_{set}	3.0	—	3.0	—	3.0	—	ns
Hold Time	t_{hold}	0.5	—	0.5	—	0.5	—	ns
Rise Time	t_r	0.5	2.4	0.5	2.4	0.5	2.4	ns
Fall Time	t_f	0.5	2.4	0.5	2.4	0.5	2.4	ns

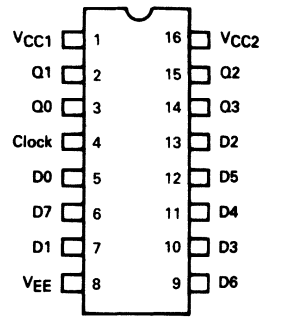
NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

TRUTH TABLE

DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	L
L	H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	H
L	L	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	H	L
L	L	L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H
L	L	L	L	H	ϕ	ϕ	ϕ	H	H	L	L
L	L	L	L	L	H	ϕ	ϕ	H	H	L	H
L	L	L	L	L	L	H	ϕ	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

ϕ = Don't Care

DIP PIN ASSIGNMENT



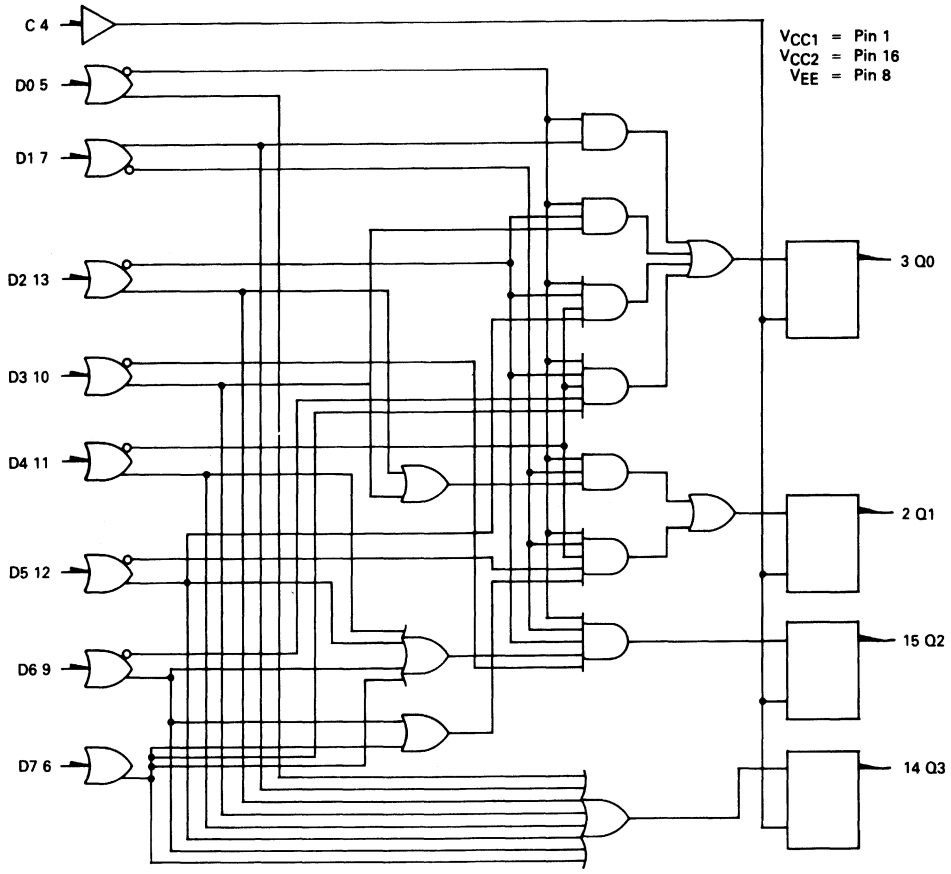
Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

8-INPUT PRIORITY ENCODER

The MC10H165 is a device designed to encode eight inputs to a binary coded output. The output code is that of the highest order input. Any input of lower priority is ignored. Each output incorporates a latch allowing synchronous operation. When the clock is low the outputs follow the inputs and latch when the clock goes high. This device is very useful for a variety of applications in checking system status in control processors, peripheral controllers, and testing systems.

The input is active when high, (e.g., the three binary outputs are low when input D0 is high). The Q3 output is high when any input is high. This allows direct extension into another priority encoder when more than eight inputs are necessary. The MC10H165 can also be used to develop binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.

LOGIC DIAGRAM

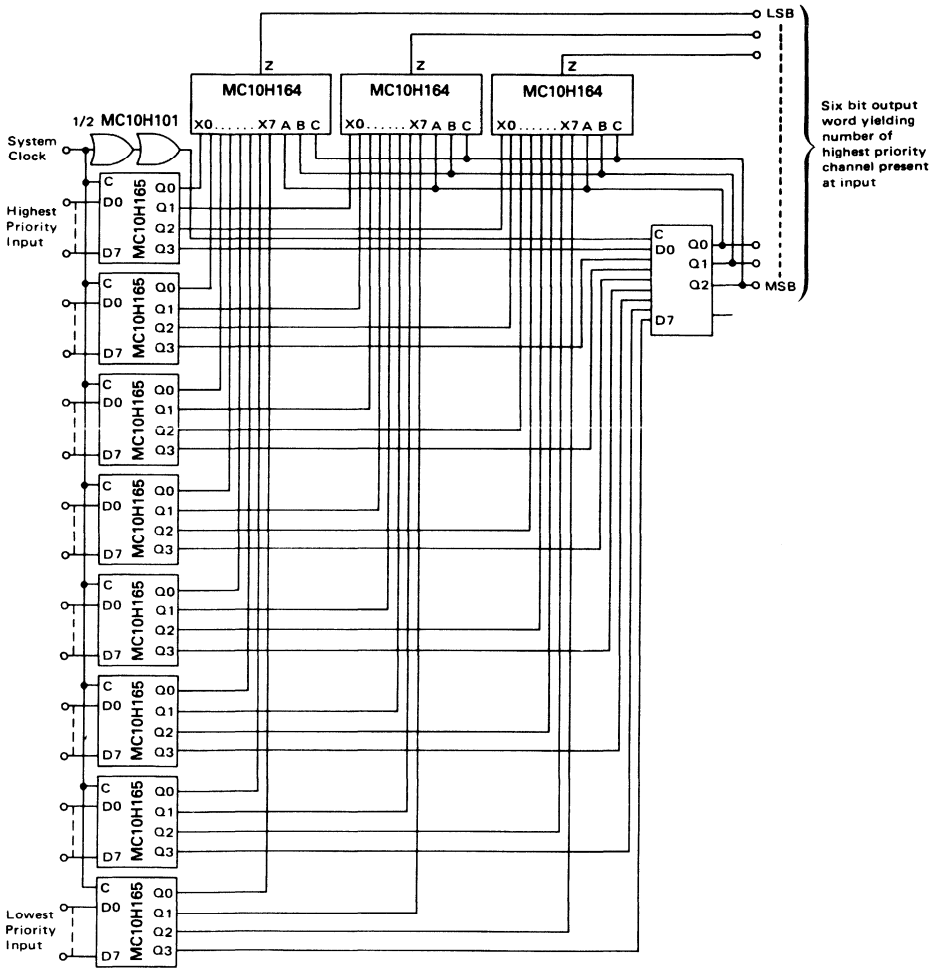


Numbers at ends of terminals denote pin numbers for L and P packages.

APPLICATION INFORMATION

A typical application of the MC10H165 is the decoding of system status on a priority basis. A 64-line priority encoder is shown in the figure below. System status lines are connected to this encoder such that, when a given condition exists, the respective input will be at a logic high level. This scheme will select the one of 64 different system conditions, as represented at the encoder inputs, which has priority in determining the next system operation to be performed. The binary code showing the address of the highest priority input present will appear at the encoder outputs to control other system logic functions.

64-LINE PRIORITY ENCODER



MOTOROLA

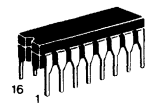
MC10H166

5-BIT MAGNITUDE COMPARATOR

The MC10H166 is a 5-Bit Magnitude Comparator and is a functional/pinout duplication of the standard MECL 10K part with 100% improvement in propagation delay and no increase in power-supply current.

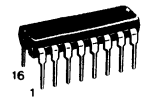
The MC10H166 is a high-speed expandable 5-bit comparator for comparing the magnitude of two binary words. Two outputs are provided: A<B and A>B. The A=B function can be obtained by wire-ORing these outputs (a low level indicates A=B) or by wire-NORing the outputs (a high level indicates A=B). A high level on the enable function forces both outputs low.

- Propagation Delay, Data-to-Output, 2.0 ns Typical
- Power Dissipation 440 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

TRUTH TABLE

Inputs			Outputs	
$\overline{E}$	A	B	A < B	A > B
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A > Word B		L	H
L	Word A < Word B		H	L

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

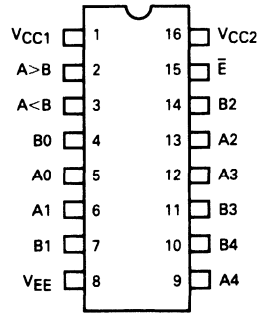
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	117	—	106	—	117	mA
Input Current High	I_{inH}	—	350	—	220	—	220	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Data-to-Output Enable-to-Output	t_{pd}	 1.1 0.6	 3.5 1.7	 1.1 0.7	 3.7 1.7	 1.2 0.7	 4.1 1.8	ns
Rise Time	t_r	0.6	1.5	0.6	1.6	0.6	1.7	ns
Fall Time	t_f	0.6	1.5	0.6	1.6	0.6	1.7	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

DIP
PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

LOGIC DIAGRAM

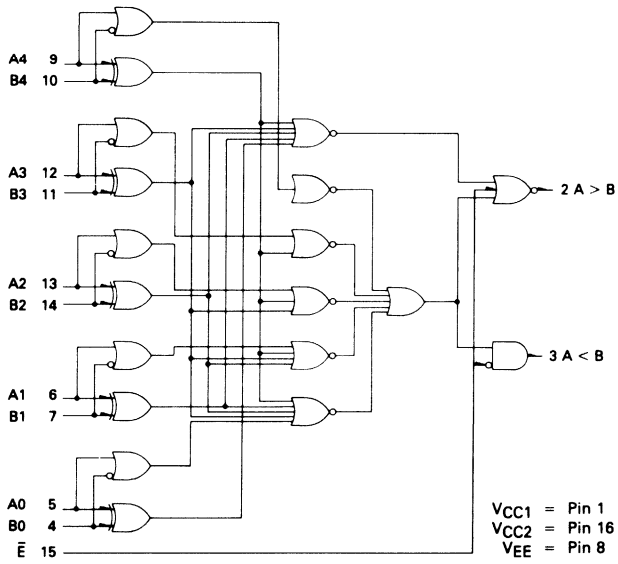
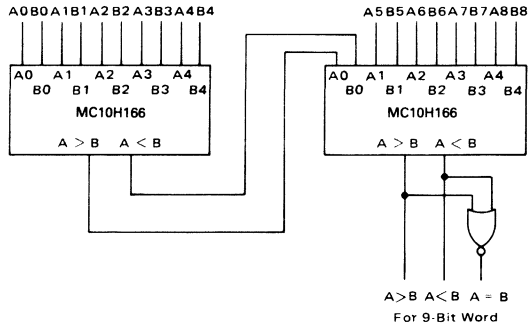
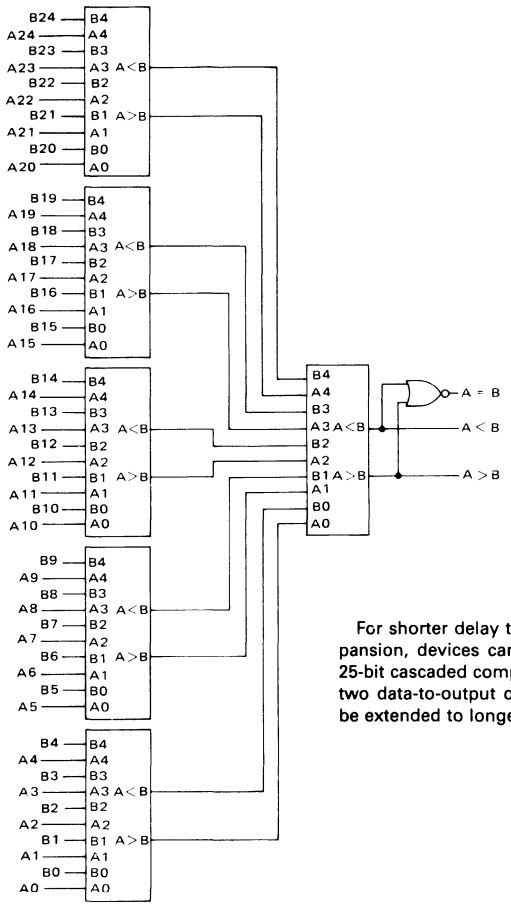


FIGURE 1 — 9-BIT MAGNITUDE COMPARATOR



For longer word lengths, the MC10H166 can be serially expanded or cascaded. Figure 1 shows two devices in a serial expansion for a 9-bit word length. The A >B and A <B outputs are fed to the A0 and B0 inputs respectively of the next device. The connection for an A = B output is also shown. The worst case delay time of serial expansion is equal to the number of comparators times the data-to-output delay.

FIGURE 2 — 25-BIT MAGNITUDE COMPARATOR



For shorter delay times than possible with serial expansion, devices can be cascaded. Figure 2 shows a 25-bit cascaded comparator whose worst case delay is two data-to-output delays. The cascaded scheme can be extended to longer word lengths.

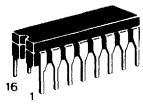
MOTOROLA

MC10H171

DUAL BINARY TO 1-4-DECODER (LOW)

The MC10H171 is a binary coded 2 line to dual 4 line decoder with selected outputs low. With either $\overline{E0}$ or $\overline{E1}$ high, the corresponding selected 4 outputs are high. The common enable $\overline{E}$, when high, forces all outputs high.

- Propagation Delay, 2 ns Typical
- Power Dissipation 325 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

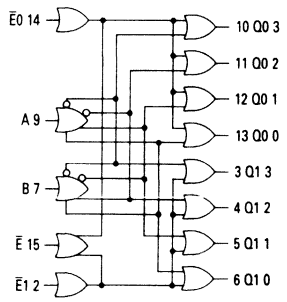
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	85	—	77	—	85	mA
Input Current High	I_{inH}	—	425	—	265	—	265	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Propagation Delay	t_{pd}							ns
Data		0.5	2.0	0.5	2.1	0.5	2.2	
Select		0.5	2.6	0.5	2.7	0.5	2.8	
Rise Time	t_r	0.5	1.7	0.5	1.8	0.5	1.9	ns
Fall Time	t_f	0.5	1.7	0.5	1.8	0.5	1.9	ns

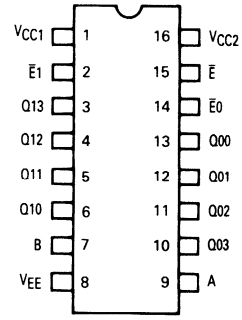
NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

TRUTH TABLE

Enable Inputs			Inputs		Outputs							
$\overline{E}$	$\overline{E}0$	$\overline{E}1$	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H

ϕ = Don't Care

2

MOTOROLA

MC10H172

DUAL BINARY TO 1–4-DECODER (HIGH)

The MC10H172 is a binary coded 2 line to dual 4 line decoder with selected outputs high. With either $\overline{E}0$ or $\overline{E}1$ low, the corresponding selected 4 outputs are low. The common enable $\overline{E}$, when high, forces all outputs low.

- Propagation Delay, 2 ns Typical
- Power Dissipation 325 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

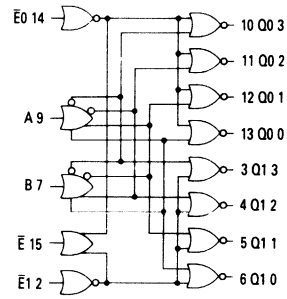
Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	85	—	77	—	85	mA
Input Current High	I_{inH}	—	425	—	265	—	265	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Propagation Delay	t_{pd}							ns
Data		0.5	2.0	0.5	2.1	0.5	2.2	
Select		0.5	2.6	0.5	2.7	0.5	2.8	
Rise Time	t_r	0.5	1.7	0.5	1.8	0.5	1.9	ns
Fall Time	t_f	0.5	1.7	0.5	1.8	0.5	1.9	ns

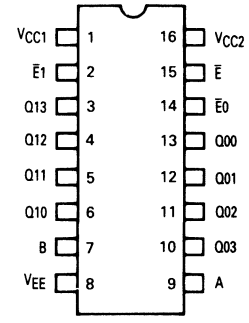
NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

TRUTH TABLE

Enable Inputs			Inputs		Outputs							
$\overline{E}$	$\overline{E}1$	$\overline{E}0$	A	B	Q1 0	Q1 1	Q1 2	Q1 3	Q0 0	Q0 1	Q0 2	Q0 3
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	L	H	L	H	L	L	L	H	L	L
L	H	H	H	L	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	L	L	H	L	L	L	L	L	L	L
H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L

ϕ = Don't Care

2

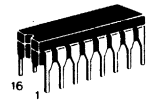
MOTOROLA

MC10H173

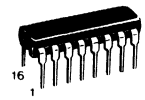
QUAD 2-INPUT MULTIPLEXER/LATCH

The MC10H173 is a quad 2-input multiplexer with latch. This device is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Data Propagation Delay, 1.5 ns Typical
- Power Dissipation, 275 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

TRUTH TABLE

SELECT	CLOCK	$Q0_{n+1}$
H	L	D00
L	L	D01
ϕ	H	$Q0_n$

ϕ = Don't Care

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

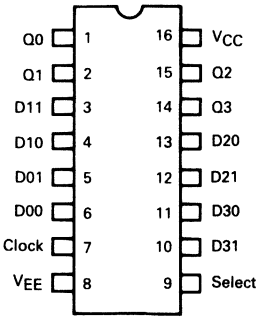
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	73	—	66	—	73	mA
Input Current High Pins 3–7 & 10–13 Pin 9	I_{inH}	 — —	 510 475	 — —	 320 300	 — —	 320 300	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Data Clock Select	t_{pd}	 0.7 1.0 1.0	 2.3 3.7 3.6	 0.7 1.0 1.0	 2.3 3.7 3.6	 0.7 1.0 1.0	 2.3 3.7 3.6	ns
Set-up Time Data Select	t_{set}	 0.7 1.0	 — —	 0.7 1.0	 — —	 0.7 1.0	 — —	ns
Hold Time Data Select	t_{hold}	 0.7 1.0	 — —	 0.7 1.0	 — —	 0.7 1.0	 — —	ns
Rise Time	t_r	0.7	2.4	0.7	2.4	0.7	2.4	ns
Fall Time	t_f	0.7	2.4	0.7	2.4	0.7	2.4	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

DIP PIN ASSIGNMENT



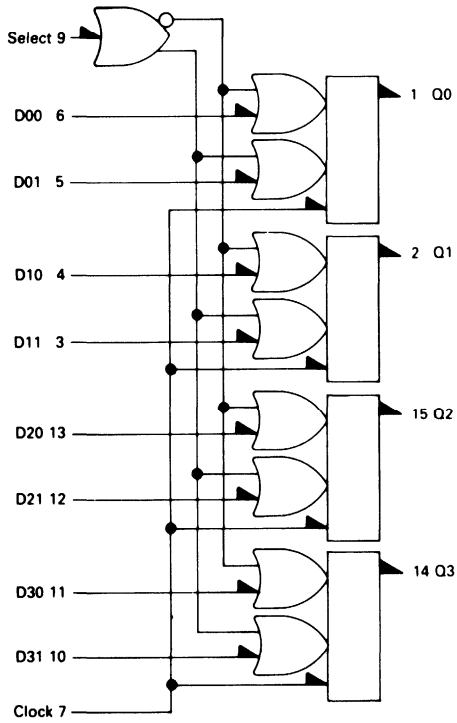
Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

APPLICATION INFORMATION

The MC10173 is a quad two-channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

2

LOGIC DIAGRAM



V_{CC} = Pin 16
V_{EE} = Pin 8

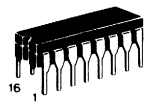
MOTOROLA

MC10H174

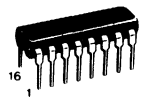
DUAL 4 TO 1 MULTIPLEXER

The MC10H174 is a Dual 4-to-1 Multiplexer. This device is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 305 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	80	—	73	—	80	mA
Input Current High Pins 3–7 & 9–13 Pin 14	I_{inH}	 — —	 475 670	 — —	 300 420	 — —	 300 420	μAdc
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Data Select (A, B) Enable	t_{pd}	 0.7 1.0 0.4	 2.4 2.8 1.45	 0.8 1.1 0.4	 2.5 2.9 1.5	 0.9 1.2 0.5	 2.6 3.2 1.7	ns
Rise Time	t_r	0.5	1.5	0.5	1.6	0.5	1.7	ns
Fall Time	t_f	0.5	1.5	0.5	1.6	0.5	1.7	ns

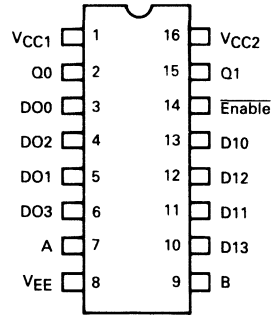
NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
E	B	A	Z	W
H	ϕ	ϕ	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

ϕ = Don't Care

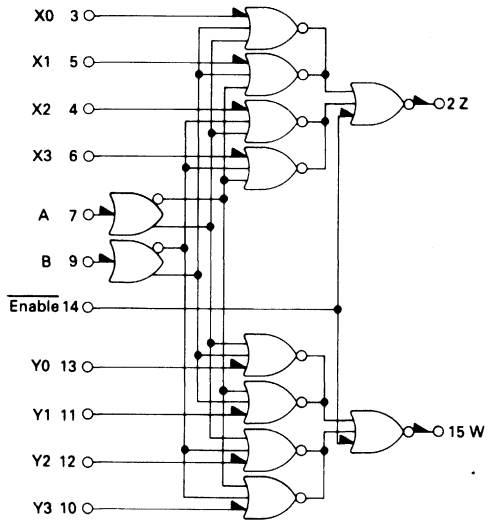
DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

2

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

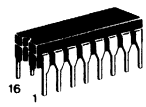
MOTOROLA

MC10H175

QUINT LATCH

The MC10H175 is a quint D type latch with common reset and clock lines. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.2 ns Typical
- Power Dissipation, 400 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

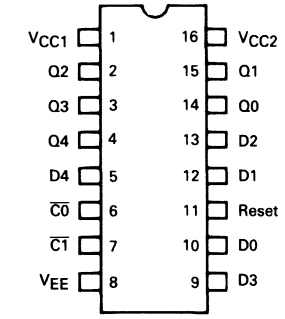
2

TRUTH TABLE

D	$\overline{C0}$	$\overline{C1}$	Reset	Q_{n+1}
L	L	L	ϕ	L
H	L	L	ϕ	H
ϕ	H	ϕ	L	Q_n
ϕ	ϕ	H	L	Q_n
ϕ	H	ϕ	H	L
ϕ	ϕ	H	H	L

ϕ = don't care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	107	—	97	—	107	mA
Input Current High Pins 5,6,7,9,10,12,13 Pin 11	I_{inH}	 — —	 565 1120	 — —	 335 660	 — —	 335 660	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Data Clock Reset	t_{pd}	 0.6 0.7 1.0	 1.6 1.9 2.2	 0.6 0.7 1.0	 1.6 2.0 2.3	 0.6 0.8 1.0	 1.7 2.1 2.4	ns
Set-up Time	t_{set}	1.5	—	1.5	—	1.5	—	ns
Hold Time	t_{hold}	0.8	—	0.8	—	0.8	—	ns
Rise Time	t_r	0.5	1.8	0.5	1.9	0.5	2.0	ns
Fall Time	t_f	0.5	1.8	0.5	1.9	0.5	2.0	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

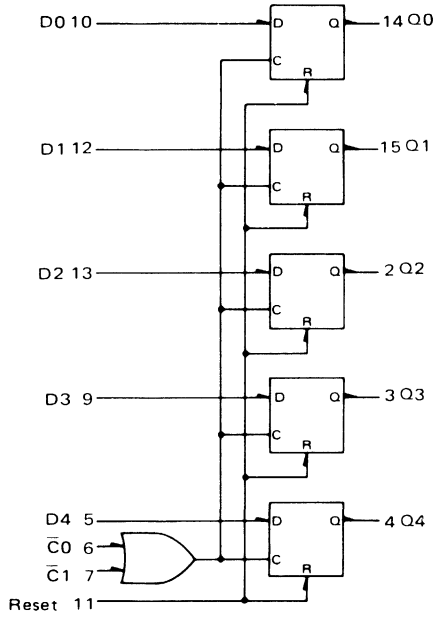
APPLICATION INFORMATION

The MC10H175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. **THE RESET INPUT IS ENABLED ONLY WHEN THE CLOCK IS IN THE HIGH STATE.**

2

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

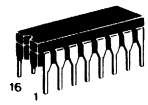
MOTOROLA

MC10H176

HEX "D" MASTER-SLAVE FLIP-FLOP

The MC10H176 contains six master slave type "D" flip-flops with a common clock. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock frequency and propagation delay and no increase in power-supply current.

- Propagation Delay, 1.7 ns Typical
- Power Dissipation, 460 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

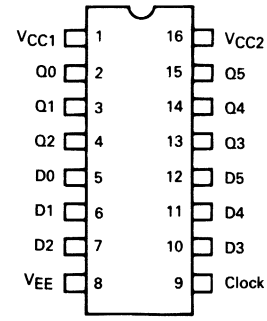
CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H*	L	L
H*	H	H

ϕ = Don't Care

*A clock H is a clock transition from a low to a high state.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to 150 −55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	123	—	112	—	123	mA
Input Current High Pins 5,6,7,10,11,12 Pin 9	I_{inH}	 — —	 425 670	 — —	 265 420	 — —	 265 420	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

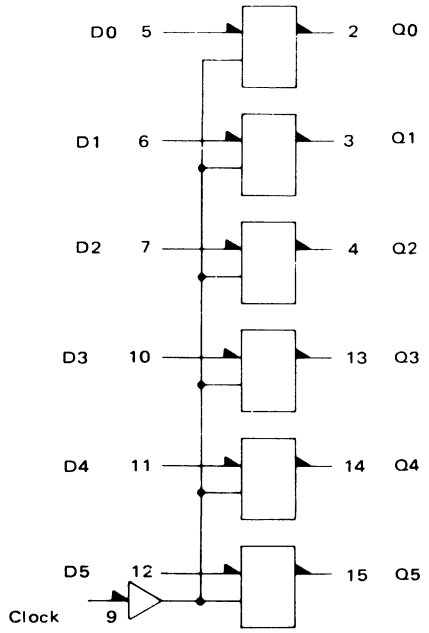
Propagation Delay	t_{pd}	0.9	2.1	0.9	2.2	1.0	2.4	ns
Set-up Time	t_{set}	1.5	—	1.5	—	1.5	—	ns
Hold Time	t_{hold}	0.9	—	0.9	—	1.0	—	ns
Rise Time	t_r	0.5	1.8	0.5	1.9	0.5	2.0	ns
Fall Time	t_f	0.5	1.8	0.5	1.9	0.5	2.0	ns
Toggle Frequency	f_{tog}	250	—	250	—	250	—	MHz

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

APPLICATION INFORMATION

The MC10H176 contains six high-speed, master slave type "D" flip-flops. Data is entered into the master when the clock is low. Master-to-slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

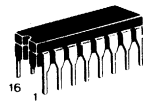
MOTOROLA

MC10H179

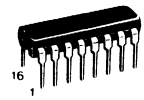
LOOK-AHEAD CARRY BLOCK

The MC10H179 is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Power Dissipation, 300 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

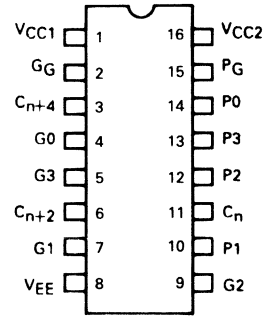


P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

DIP
PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0- +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	79	—	72	—	79	mA
Input Current High	I_{inH}							μA
Pins 5 and 9		—	465	—	275	—	275	
Pins 4, 7 and 11		—	545	—	320	—	320	
Pin 14		—	705	—	415	—	415	
Pin 12		—	790	—	465	—	465	
Pins 10 and 13		—	870	—	510	—	510	
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

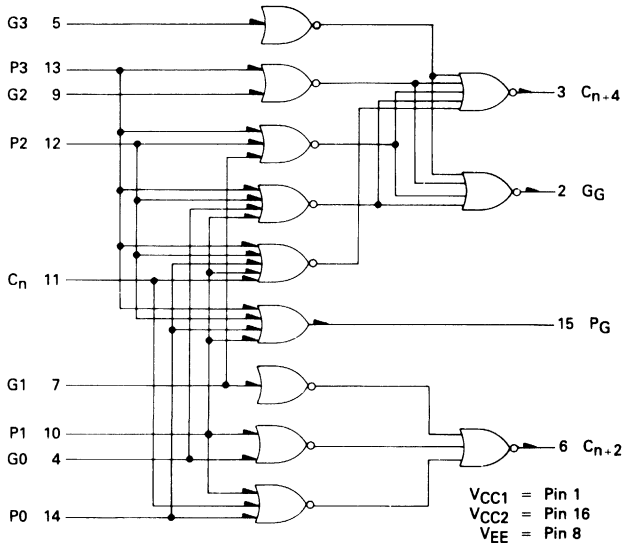
AC PARAMETERS

Propagation Delay	t_{pd}							ns
P to P_G		0.4	1.4	0.4	1.5	0.5	1.7	
G, P, C_n to C_n or G_G		0.6	2.3	0.7	2.4	0.8	2.6	
Rise Time	t_r	0.5	1.7	0.5	1.8	0.5	1.9	ns
Fall Time	t_f	0.5	1.7	0.5	1.8	0.5	1.9	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

2

LOGIC DIAGRAM



$P_G = P0 + P1 + P2 + P3$

$G_G = (G0 + P1 + P2 + P3)(G1 + P2 + P3)(G2 + P3)G3$

$C_{n+2} = (C_n + P0 + P1)(G0 + P1)G1$

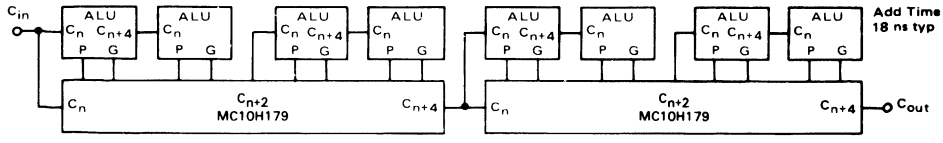
$C_{n+4} = (C_n + P0 + P1 + P2 + P3)(G0 + P1 + P2 + P3)(G1 + P2 + P3)(G2 + P3)G3$

TYPICAL APPLICATIONS

The MC10H179 is a high-speed, low-power, standard MECL complex function that is designed to perform the look-ahead carry function. This device can be used with the MC10H181 4-bit ALU directly, or with the MC10H180 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high speed arithmetic operation on long words.

When used with the MC10H181, the MC10H179 performs a second order or higher look-ahead. Figure 2 shows a 16-bit look-ahead carry arithmetic unit. Second order carry is valuable for longer binary words. As an example, addition of two 32-bit words is improved from 30 nanoseconds with ripple-carry techniques. A block diagram of a 32-bit ALU is shown in Figure 1. The MC10H179 may also be used in many other applications. It can, for example, reduce system package count when used to generate functions of several variables.

FIGURE 1 — 32-BIT ALU WITH CARRY LOOK-AHEAD



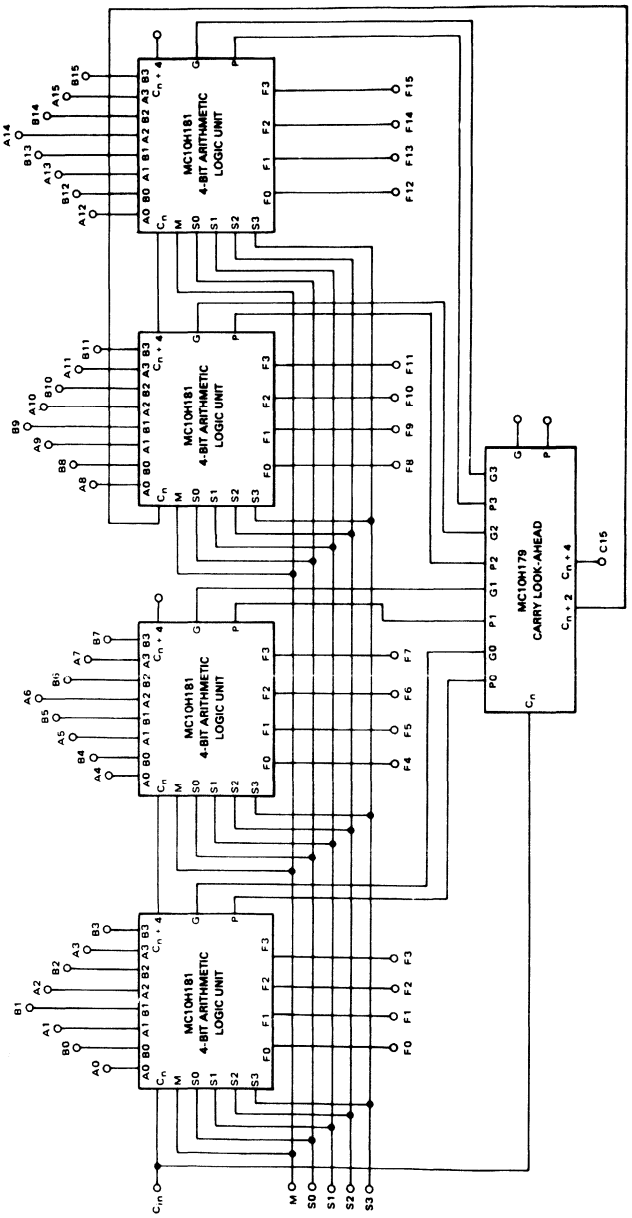


FIGURE 2 — 16-BIT FULL LOOK-AHEAD CARRY ARITHMETIC LOGIC UNIT

MOTOROLA

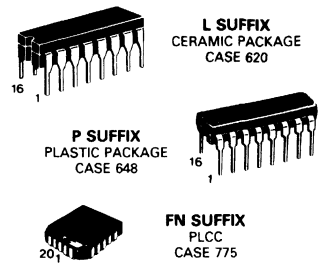
MC10H180

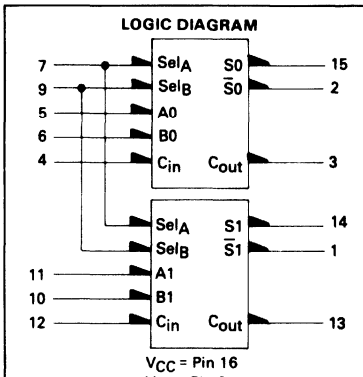
DUAL 2-BIT ADDER/SUBTRACTOR

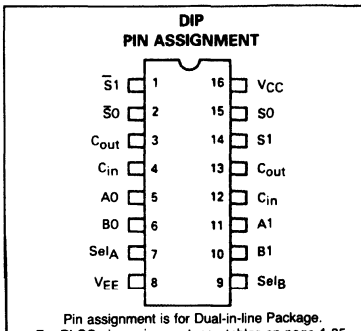
The MC10H180 is a high-speed, low-power, general-purpose adder/subtractor. It is designed to be used in special purpose adders/subtractors or in high-speed multiplier arrays.

Inputs for each adder are Carry-in, Operand A, and Operand B; outputs are Sum, $\overline{\text{Sum}}$ and Carry-out. The common select inputs serve as a control line to Invert A for subtract, and a control line to Invert B.

- Propagation Delay, 1.8 ns Typical, Operand and Select to Output
- Power Dissipation, 360 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible







Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–+75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	I_E	—	95	—	86	—	95	mA
Input Current High Pins 4, 12 Pins 7, 9 Pins 5, 6, 10, 11	I_{inH}	 — — —	 665 515 410	 — — —	 417 320 255	 — — —	 417 320 255	µA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage (1)	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage (1)	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Operand to Output Select to Output Carry-in to Output	t_{pd}	 0.6 0.6 0.4	 2.4 2.2 1.6	 0.7 0.7 0.4	 2.5 2.3 1.7	 0.8 0.8 0.4	 2.8 2.6 1.8	ns
Rise Time	t_r	0.5	2.0	0.5	2.1	0.5	2.2	ns
Fall Time	t_f	0.5	2.0	0.5	2.1	0.5	2.2	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

FUNCTION SELECT TABLE

Sel_A	Sel_B	Function
H	H	S = A plus B
H	L	S = A minus B
L	H	S = B minus A
L	L	S = 0 minus A minus B

TRUTH TABLE

FUNCTION	INPUTS								
	Sel_A	Sel_B	A0	B0	C_{in}	S0	$\overline{S0}$	C_{out}
ADD	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	H	L	L
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	H
	H	H	H	H	H	H	L	H
SUBTRACT	H	L	L	L	L	H	L	L
	H	L	L	L	H	L	H	H
	H	L	L	H	L	L	H	L
	H	L	L	H	H	H	L	H
	H	L	H	L	L	L	H	L
	H	L	H	L	H	H	L	H
	H	L	H	H	L	H	L	H
	H	L	H	H	H	L	H	H

FUNCTION	INPUTS								
	Sel_A	Sel_B	A0	B0	C_{in}	S0	$\overline{S0}$	C_{out}
REVERSE SUBTRACT	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	H	L	H
	L	H	L	H	H	L	H	L
	L	H	H	L	L	H	L	L
	L	H	H	L	H	L	H	H
	L	H	H	H	L	H	L	L
	L	H	H	H	H	L	H	H
	L	L	L	L	L	H	L	H
	L	L	L	L	H	L	H	H
	L	L	L	H	L	H	L	L
	L	L	L	H	H	L	H	L
	L	L	H	L	L	H	L	L
	L	L	H	L	H	L	H	H
	L	L	H	H	L	L	H	L
	L	L	H	H	H	L	H	L

2

MOTOROLA

MC10H181

4-BIT ARITHMETIC LOGIC UNIT/ FUNCTION GENERATOR

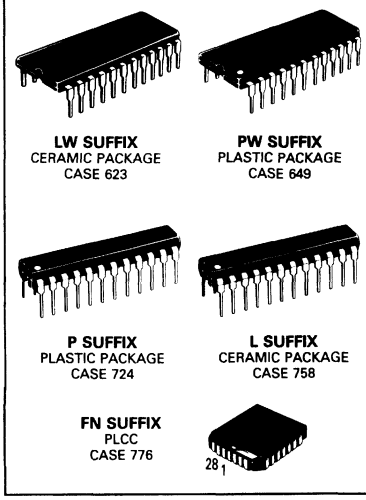
The MC10H181 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation.

Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look-ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the MC10H179, full-carry look-ahead, as a second order look-ahead block, the MC10H181 provides high-speed arithmetic operations on very long words.

This 10H part is a functional/pinout duplication of the standard MECL 10K family part with 100% improvement in propagation delay and no increase in power supply current.

- Improved Noise Margin, 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K – Compatible



LW SUFFIX
CERAMIC PACKAGE
CASE 623

PW SUFFIX
PLASTIC PACKAGE
CASE 649

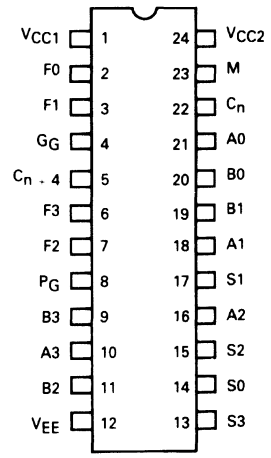
P SUFFIX
PLASTIC PACKAGE
CASE 724

L SUFFIX
CERAMIC PACKAGE
CASE 758

FN SUFFIX
PLCC
CASE 776

28 1

DIP PIN ASSIGNMENT

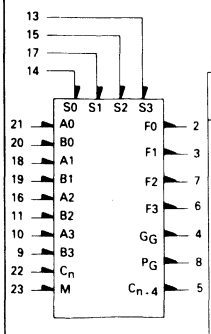


Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

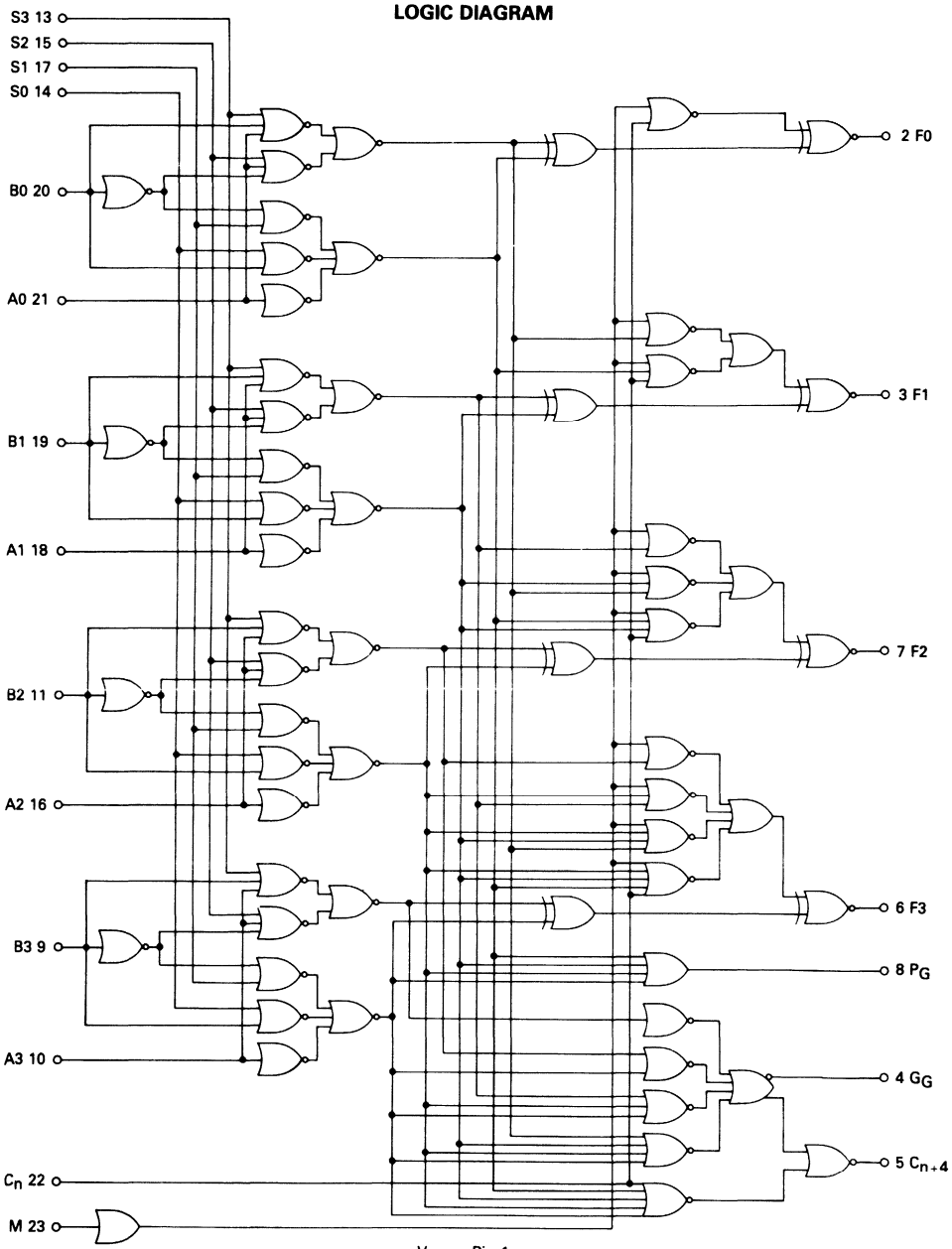
LOGIC DIAGRAM



FUNCTION SELECT TABLE

Function Select S3	S2	S1	S0	Logic Functions M is High C = D.C. F	Arithmetic Operation M is Low C_n is low F
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A} + \overline{B}$	F = A plus (A + $\overline{B}$)
L	L	H	L	$F = \overline{A} + B$	F = A plus (A + B)
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	$F = \overline{A \cdot B}$	F = (A + B) plus 0
L	H	L	H	$F = \overline{B}$	F = (A + B) plus (A + $\overline{B}$)
L	H	H	L	$F = A \oplus B$	F = A plus B
L	H	H	H	$F = A + \overline{B}$	F = A plus (A + B)
H	L	L	L	$F = \overline{A} \cdot B$	F = (A + $\overline{B}$) plus 0
H	L	L	H	$F = A \oplus B$	F = A minus B minus 1
H	L	H	L	$F = B$	F = (A + $\overline{B}$) plus (A • B)
H	L	H	H	$F = A + B$	F = A plus (A + $\overline{B}$)
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	$F = A \cdot \overline{B}$	F = (A + $\overline{B}$) minus 1
H	H	H	L	$F = A \cdot B$	F = (A • B) minus 1
H	H	H	H	F = A	F = A minus 1

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 24
V_{EE} = Pin 12

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5.0%) (See Note)

Characteristic	Symbol	0°		25°		75°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	159	—	145	—	159	mA
Input Current High	I_{inH}							μA
Pin 22		—	720	—	450	—	450	
Pins 14,23		—	405	—	255	—	255	
Pins 13,15,17		—	515	—	320	—	320	
Pins 10,16,18,21		—	475	—	300	—	300	
Pins 9,11,19,20		—	465	—	275	—	275	
Input Current Low Pins 9–11, 13–22	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

2

AC PARAMETERS

Characteristic	Symbol	Input	Output	Conditions†	AC Switching Characteristics						
					0°C		+25°C		+75°C		
					Min	Max	Min	Max	Min	Max	Unit
Propagation Delay	t+ +, t− −	C_n	C_{n+4}	A0,A1,A2,A3	0.7	2.0	0.7	2.0	0.7	2.2	ns
Rise Time, Fall Time	t+, t−	C_n	C_{n+4}	A0,A1,A2,A3	0.6	2.0	0.6	2.0	0.7	2.2	ns
Propagation Delay	t+ +, t+ −,	C_n	F1	A0							ns
	t− +, t− −	C_n	F1		1.0	3.0	1.0	3.0	1.2	3.3	
Rise Time, Fall Time	t+, t−	C_n	F1		0.7	2.2	0.7	2.2	0.7	2.4	
Propagation Delay	t+ +, t+ −,	A1	F1								ns
	t− +, t− −	A1	F1		1.5	3.7	1.5	3.7	1.6	4.0	
Rise Time, Fall Time	t+, t−	A1	F1		0.7	2.0	0.7	2.0	0.7	2.2	
Propagation Delay	t+ +, t− −	A1	P_G	S0,S3	1.5	3.7	1.5	3.7	1.6	4.0	ns
Rise Time, Fall Time	t+, t−	A1	P_G	S0,S3	0.9	2.4	0.9	2.4	0.9	2.6	ns
Propagation Delay	t+ +, t− −	A1	G_G	A0,A2,A3,C_n	1.5	3.7	1.5	3.7	1.6	3.9	ns
Rise Time, Fall Time	t+, t−	A1	G_G	A0,A2,A3,C_n	0.7	2.2	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ −, t− +	A1	C_{n+4}	A0,A2,A3,C_n	1.5	3.6	1.5	3.6	1.6	3.9	ns
Rise Time, Fall Time	t+, t−	A1	C_{n+4}	A0,A2,A3,C_n	0.5	2.0	0.5	2.0	0.5	2.2	ns
Propagation Delay	t+ +, t− +,	B1	F1	S3,C_n	2.0	4.5	2.0	4.5	2.1	4.8	ns
Rise Time, Fall Time	t+, t−	B1	F	S3,C_n	0.7	2.3	0.7	2.3	0.7	2.5	ns
Propagation Delay	t+ +, t− −	B1	P_G	S0,A1	1.5	3.8	1.5	3.8	1.6	4.0	ns
Rise Time, Fall Time	t+, t−	B1	P_G	S0,A1	0.7	2.2	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ +, t− −	B1	G_G	S3,C_n	1.5	3.7	1.5	3.7	1.6	4.0	ns
Rise Time, Fall Time	t+, t−	B1	G_G	S3,C_n	0.7	2.2	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ −, t− +	B1	C_{n+4}	S3,C_n	2.0	4.0	2.0	4.0	2.1	4.3	ns
Rise Time, Fall Time	t+, t−	B1	C_{n+4}	S3,C_n	0.5	2.0	0.5	2.2	0.5	2.2	ns
Propagation Delay	t+ +, t+ −	M	F1	—	1.5	4.2	1.5	4.2	1.6	4.5	ns
Rise Time, Fall Time	t+, t−	M	F1	—	0.8	2.3	0.8	2.3	0.8	2.5	ns
Propagation Delay	t+ −, t− +	S1	F1	A1,B1	1.5	4.5	1.5	4.5	1.6	4.8	ns
Rise Time, Fall Time	t+, t−	S1	F1	A1,B1	0.7	2.0	0.7	2.0	0.7	2.2	ns
Propagation Delay	t− +, t+ −	S1	P_G	A3,B3	1.5	4.0	1.5	4.0	1.6	4.3	ns
Rise Time, Fall Time	t+, t−	S1	P_G	A3,B3	0.7	2.0	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ −, t− +	S1	C_{n+4}	A3,B3	1.5	4.1	1.5	4.1	1.6	4.4	ns
Rise Time, Fall Time	t+, t−	S1	C_{n+4}	A3,B3	0.7	2.2	0.7	2.2	0.7	2.4	ns
Propagation Delay	t+ −, t− +	S1	G_G	A3,B3	1.3	4.5	1.3	4.5	1.4	4.8	ns
Rise Time, Fall Time	t+, t−	S1	G_G	A3,B3	0.5	3.2	0.5	3.2	0.5	3.4	ns

†Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc.
V_{CC1} = V_{CC2} = +2.0 Vdc, V_{EE} = −3.2 Vdc

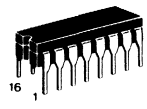
MOTOROLA

MC10H186

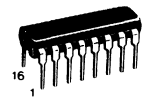
HEX "D" MASTER-SLAVE FLIP-FLOP WITH RESET

The MC10H186 is a hex D type flip-flop with common reset and clock lines. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock toggle frequency and propagation delay and no increase in power-supply current.

- Propagation Delay, 1.7 ns Typical
- Power Dissipation, 460 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

CLOCKED TRUTH TABLE

R	C	Q	Qn+1
L	L	ϕ	Qn
L	H *	L	L
L	H *	H	H
H	L	ϕ	L
H	H *	D	D

ϕ = Don't Care
* A clock H is a clock transition from a low to a high state.

ELECTRICAL CHARACTERISTICS (V_{EE} = 5.2 V ±5%) (See Note)

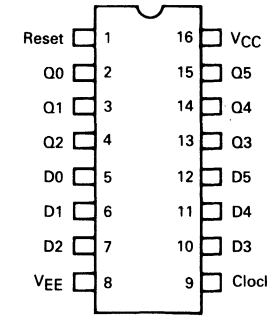
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	121	—	110	—	121	mA
Input Current High Pins 5,6,7,10,11,12 Pin 9 Pin 1	I_{inH}	 — — —	 430 670 1250	 — — —	 265 420 765	 — — —	 265 420 765	µA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.7	3.0	0.7	3.0	0.7	3.0	ns
Set-up Time	t_{set}	1.5	—	1.5	—	1.5	—	ns
Hold Time	t_{hold}	1.0	—	1.0	—	1.0	—	ns
Rise Time	t_r	0.7	2.6	0.7	2.6	0.7	2.6	ns
Fall Time	t_f	0.7	2.6	0.7	2.6	0.7	2.6	ns
Toggle Frequency	f_{tog}	250	—	250	—	250	—	MHz
Reset Recovery Time (t_{1-9+})	t_{rr}	3.0	—	3.0	—	3.0	—	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

DIP PIN ASSIGNMENT

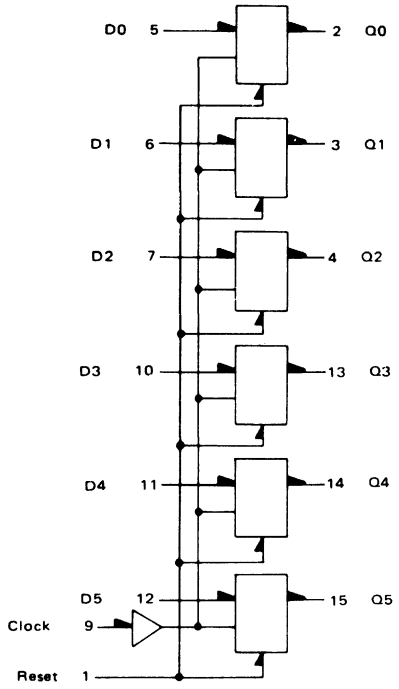


Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

APPLICATION INFORMATION

The MC10H186 contains six high-speed, master slave type "D" flip-flops. Data is entered into the master when the clock is low. Master-to-slave data transfer takes place on the positive-going Clock transition. Thus outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device. A common Reset is included in this circuit. **THE RESET ONLY FUNCTIONS WHEN THE CLOCK IS LOW.**

LOGIC DIAGRAM



V_{CC} = Pin 16
V_{EE} = Pin 8

MOTOROLA

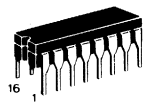
MC10H188

HEX BUFFER WITH ENABLE

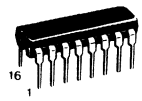
The MC10H188 is a high-speed Hex Buffer with a common Enable input. When Enable is in the high-state, all outputs are in the low-state. When Enable is in the low-state, the outputs take the same state as the inputs.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.3 ns Typical Data-to-Output
- Power Dissipation 180 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–+75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

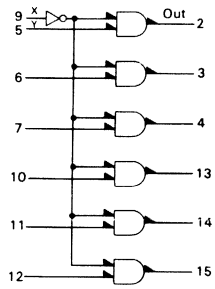
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	46	—	42	—	46	mA
Input Current High	I_{inH}	—	495	—	310	—	310	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Enable Data	t_{pd}	 0.7 0.7	 2.2 1.9	 0.7 0.7	 2.2 1.9	 0.7 0.7	 2.2 1.9	ns
Rise Time	t_r	0.7	2.4	0.7	2.4	0.7	2.4	ns
Fall Time	t_f	0.7	2.4	0.7	2.4	0.7	2.4	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

LOGIC DIAGRAM

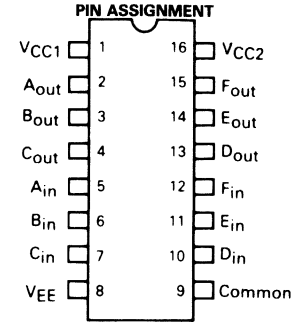


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

Inputs		Output
X	Y	OUT
L	L	L
L	H	H
H	L	L
H	H	L

DIP
PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MOTOROLA

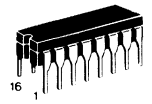
MC10H189

HEX INVERTER WITH ENABLE

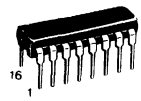
The MC10H189 is a Hex Inverter with a common Enable input. The hex inverting function is provided when Enable is in the low-state. When Enable is in the high-state, all outputs are low.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.3 ns Typical Data-to-Output
- Power Dissipation 180 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



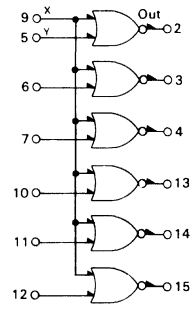
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM

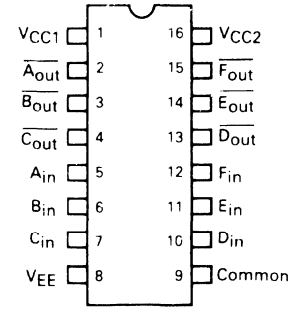


TRUTH TABLE

Inputs		Output
X	Y	OUT
L	L	H
L	H	L
H	L	L
H	H	L

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0-+75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	46	—	42	—	46	mA
Input Current High	I_{inH}	—	495	—	310	—	310	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Enable Data	t_{pd}	 0.7 0.7	 2.2 1.9	 0.7 0.7	 2.2 1.9	 0.7 0.7	 2.3 1.9	ns
Rise Time	t_r	0.7	2.4	0.7	2.4	0.7	2.4	ns
Fall Time	t_f	0.7	2.4	0.7	2.4	0.7	2.4	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

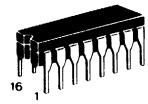
MOTOROLA

MC10H209

DUAL 4-5-INPUT OR/NOR GATE

The MC10H209 is a Dual 4-5-input OR/NOR gate. This MECL part is a functional/pinout duplication of the MECL III part MC1688.

- Propagation Delay Average, 0.75 ns Typical
- Power Dissipation 125 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



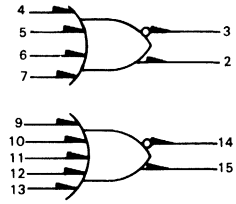
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

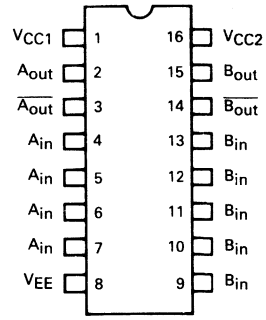
2

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	I_E	—	—	—	30	—	—	mA
Input Current High	I_{inH}	—	640	—	400	—	400	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.4	1.15	0.4	1.15	0.4	1.15	ns
Rise Time	t_r	0.4	1.5	0.4	1.5	0.4	1.6	ns
Fall Time	t_f	0.4	1.5	0.4	1.5	0.4	1.6	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

MOTOROLA

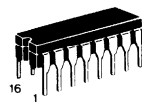
MC10H210

DUAL 3-INPUT 3-OUTPUT "OR" GATE

The MC10H210 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

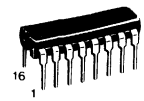
The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10H210 particularly useful in clock distribution applications where minimum clock skew is desired.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 160 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



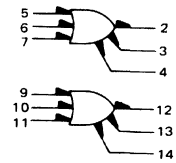
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



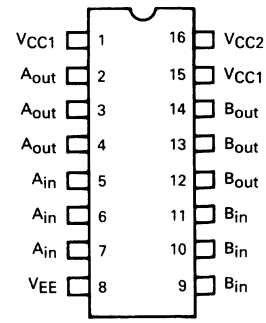
FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM



V_{CC1} = Pins 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	42	—	38	—	42	mA
Input Current High	I_{inH}	—	720	—	450	—	450	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.5	1.55	0.55	1.55	0.6	1.7	ns
Rise Time	t_r	0.75	1.8	0.75	1.9	0.8	2.0	ns
Fall Time	t_f	0.75	1.8	0.75	1.9	0.8	2.0	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

Note: If crosstalk is present, double bypass capacitor to 0.2μF.

MOTOROLA

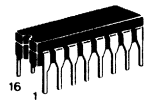
MC10H211

DUAL 3-INPUT 3-OUTPUT "NOR" GATE

The MC10H211 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10H211 particularly useful in clock distribution applications where minimum clock skew is desired.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 160 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



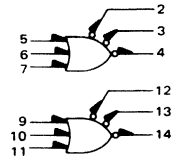
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

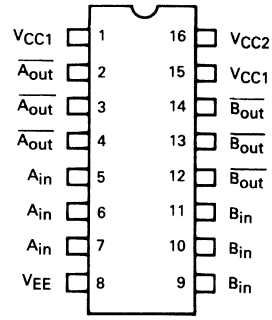
2

LOGIC DIAGRAM



V_{CC1} = Pins 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	42	—	38	—	42	mA
Input Current High	I_{inH}	—	720	—	450	—	450	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.7	1.6	0.7	1.6	0.7	1.7	ns
Rise Time	t_r	0.9	2.0	0.9	2.2	0.9	2.4	ns
Fall Time	t_f	0.9	2.0	0.9	2.2	0.9	2.4	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

Note: If crosstalk is present, double bypass capacitor to 0.2μF.

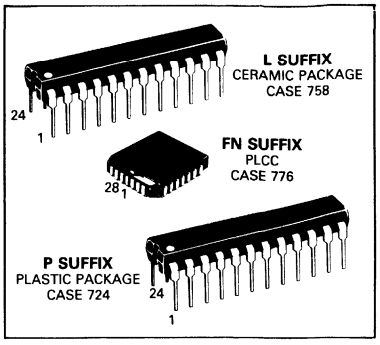
MOTOROLA

MC10H330

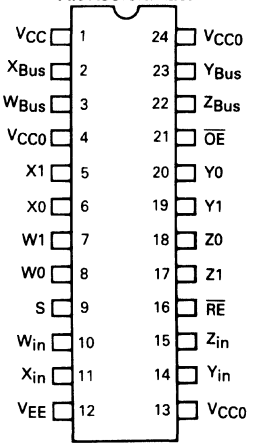
QUAD BUS DRIVER/RECEIVER WITH 2-TO-1 OUTPUT MULTIPLEXERS

The MC10H330 is a Quad Bus Driver/Receiver with two-to-one output multiplexers. These multiplexers have a common select and output enable. When disabled, ($\overline{OE}$ = high) the bus outputs go to −2.0 V. Their output can be brought to a low state (V_{OL}) by applying a high level to the receiver enable ($\overline{RE}$ = High). The parameters specified are with 25 Ω loading on the bus drivers and 50 Ω loads on the receivers.

- Propagation Delay, 1.5 ns Typical Data-to-Output
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



DIP
PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

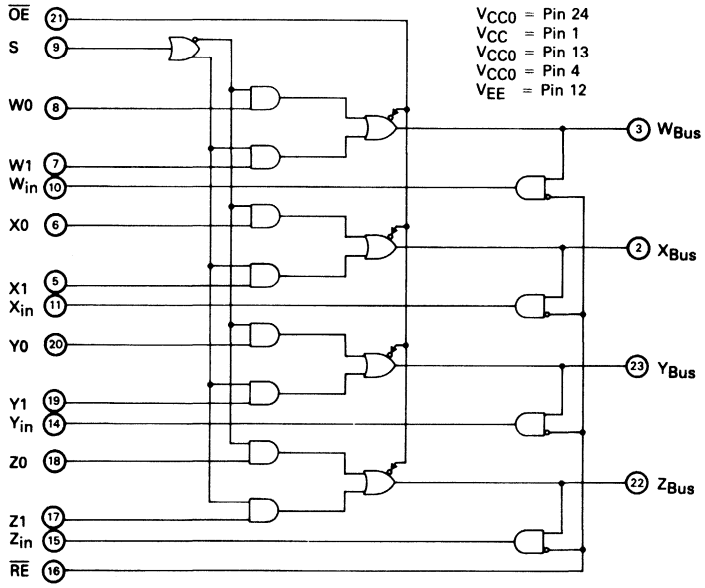
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	157	—	143	—	157	mA
Input Current High Pins 5–8, 17–20 Pins 16, 21 Pin 9	I_{inH}	 — — —	 667 514 475	 — — —	 417 321 297	 — — —	 417 321 297	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Select-to-Input Data-to-Bus Output Select-to-Bus Output $\overline{OE}$-to-Bus Output Bus-to-Input $\overline{RE}$-to-Input Data-to-Receiver Input	t_{pd}	 1.8 0.5 1.0 0.8 0.8 0.5 1.3	 5.3 2.0 3.2 2.2 2.1 2.2 4.0	 1.8 0.5 1.0 0.8 0.8 0.5 1.3	 5.3 2.0 3.2 2.2 2.1 2.2 4.0	 1.8 0.5 1.0 0.8 0.8 0.5 1.3	 5.3 2.0 3.2 2.2 2.4 2.2 4.0	ns
Rise Time	t_r	0.5	2.0	0.5	2.0	0.5	2.0	ns
Fall Time	t_f	0.5	2.0	0.5	2.0	0.5	2.0	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Receiver outputs are terminated through a 50-ohm resistor to −2.0 volts dc. Bus outputs are terminated through a 25-ohm resistor to −2.0 volts dc.

LOGIC DIAGRAM



MULTIPLEXER TRUTH TABLE

$\overline{OE}$	S	W_{Bus}	X_{Bus}	Y_{Bus}	Z_{Bus}
H	X	−2.0 V	−2.0 V	−2.0 V	−2.0 V
L	L	W0	X0	Y0	Z0
L	H	W1	X1	Y1	Z1

X — Don't care

RECEIVER TRUTH TABLE

$\overline{RE}$	W_{in}	X_{in}	Y_{in}	Z_{in}
H	L	L	L	L
L	W_{Bus}	X_{Bus}	Y_{Bus}	Z_{Bus}

2

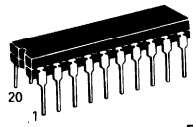
MOTOROLA

MC10H332

DUAL BUS DRIVER/RECEIVER WITH 4-TO-1 OUTPUT MULTIPLEXERS

The MC10H332 is a Dual Bus Driver/Receiver with four-to-one output multiplexers. These multiplexers have common selects and output enable. When disabled, ($\overline{OE}$ = high) the bus outputs go to −2.0 V. The parameters specified are with 25 Ω loading on the bus drivers and 50 Ω loads on the receivers.

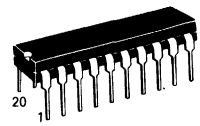
- Propagation Delay, 1.5 ns Typical Data-to-Output
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



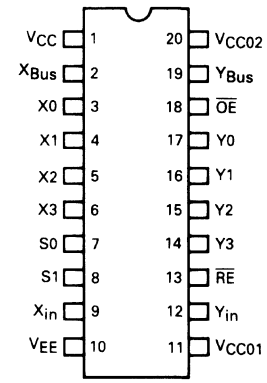
L SUFFIX
CERAMIC CASE
CASE 732

FN SUFFIX
PLCC
CASE 775

P SUFFIX
PLASTIC CASE
CASE 738



DIP & PLCC PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	115	—	110	—	115	mA
Input Current High Pins 3,4,5,6,14, 15,16,17 Pins 7,8 Pins 13,18	I_{inH}	 — — —	 667 437 456	 — — —	 417 273 285	 — — —	 417 273 285	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Data-to-Bus Output Select-to-Bus Output $\overline{OE}$-to-Bus Output Bus-to-Receiver Select-to-Receiver $\overline{RE}$-to-Receiver Data-to-Receiver	t_{pd}	 0.8 0.8 0.8 0.8 1.8 0.8 1.3	 3.0 3.4 2.4 2.1 4.5 2.2 4.0	 0.8 0.8 0.8 0.8 1.8 0.8 1.3	 3.0 3.4 2.4 2.1 4.5 2.2 4.0	 0.8 0.8 0.8 0.8 1.8 0.8 1.3	 3.2 3.8 2.6 2.4 5.0 2.5 4.5	ns
Rise Time	t_r	0.5	2.0	0.5	2.0	0.5	2.1	ns
Fall Time	t_f	0.5	2.0	0.5	2.0	0.5	2.1	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Receiver outputs are terminated through a 50-ohm resistor to −2.0 volts dc. Bus outputs are terminated through a 25-ohm resistor to −2.0 volts dc.

MULTIPLEXER TRUTH TABLE

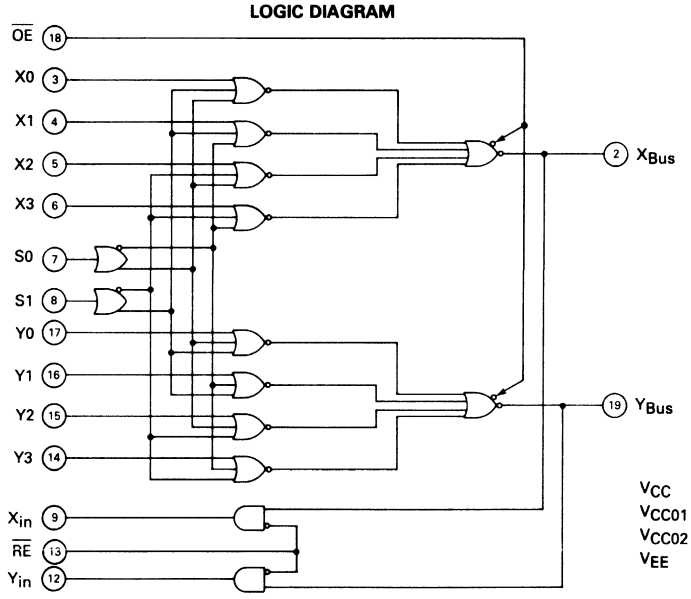
$\overline{OE}$	S1	S0	X_{Bus}	Y_{Bus}
H	X	X	-2.0 V	-2.0 V
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

X — Don't care

RECEIVER TRUTH TABLE

$\overline{RE}$	X_{in}	Y_{in}
H	L	L
L	X_{Bus}	Y_{Bus}

LOGIC DIAGRAM



2

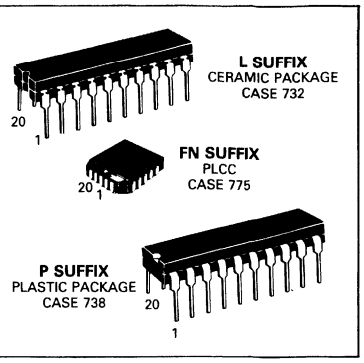
MOTOROLA

MC10H334

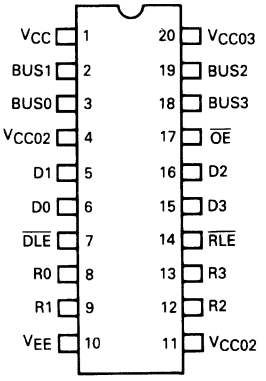
QUAD BUS DRIVER/RECEIVER WITH TRANSMIT AND RECEIVER LATCHES

The MC10H334 is a Quad Bus Driver/Receiver with transmit and receiver latches. When disabled, ($\overline{OE}$ = high) the bus outputs will fall to −2.0 V. Data to be transmitted or received is passed through its respective latch when the respective latch enable ($\overline{DLE}$ and $\overline{RLE}$) is at a low level. Information is latched on the positive transition of $\overline{DLE}$ and $\overline{RLE}$. The parameters specified are with 25 Ω loading on the bus drivers and 50 Ω loads on the receivers.

- Propagation Delay, 1.6 ns Typical Data-to-Output
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



DIP & PLCC PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

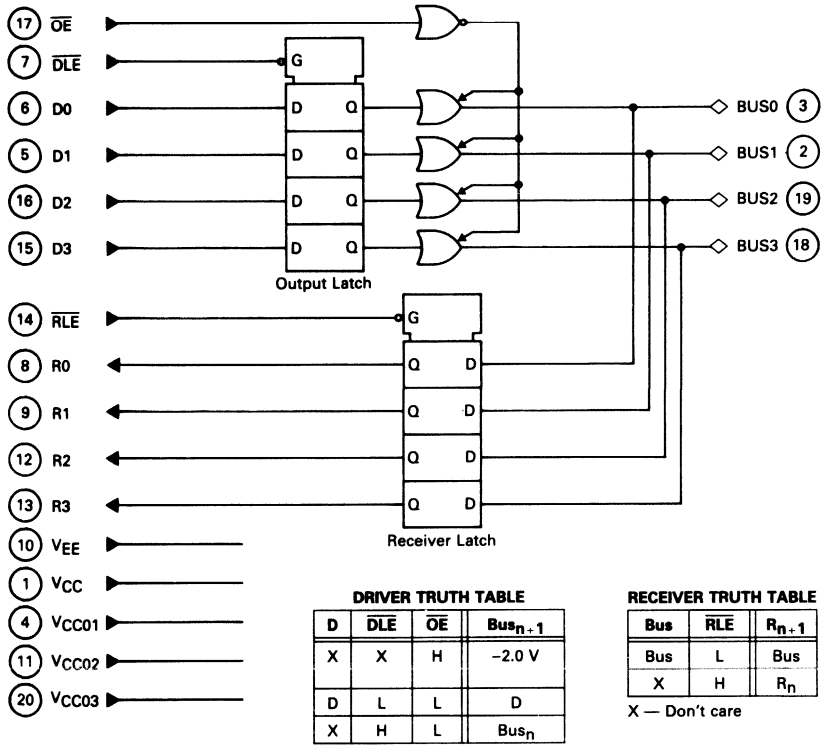
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	161	—	161	—	161	mA
Input Current High Pins 5,6,15,16 Pins 7,14 Pin 17	I_{inH}	 — — —	 397 460 520	 — — —	 273 297 357	 — — —	 273 297 357	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Data-to-Bus Output $\overline{DLE}$-to-Bus Output $\overline{OE}$-to-R0 Bus-to-R0 $\overline{RLE}$-to-R0 Data-to-Receiver R0	t_{pd}	 0.5 1.0 0.5 0.5 0.5 1.0	 2.5 2.7 2.5 1.9 2.1 3.8	 0.5 1.0 0.5 0.5 0.5 1.0	 2.5 2.7 2.5 1.9 2.1 3.8	 0.5 1.0 0.5 0.5 0.5 1.0	 2.5 2.7 2.5 1.9 2.1 3.8	ns
Rise Time	t_r	0.5	2.2	0.5	2.2	0.5	2.2	ns
Fall Time	t_f	0.5	2.2	0.5	2.2	0.5	2.2	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Receiver outputs are terminated through a 50-ohm resistor to −2.0 volts dc. Bus outputs are terminated through a 25-ohm resistor to −2.0 volts dc.

LOGIC DIAGRAM



DRIVER TRUTH TABLE

D	$\overline{DLE}$	$\overline{OE}$	Bus_{n+1}
X	X	H	−2.0 V
D	L	L	D
X	H	L	Bus_n

X — Don't care

RECEIVER TRUTH TABLE

Bus	$\overline{RLE}$	R_{n+1}
Bus	L	Bus
X	H	R_n

X — Don't care

MOTOROLA

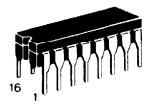
MC10H350

PECL* TO TTL TRANSLATOR
(+5 Vdc Power Supply Only)

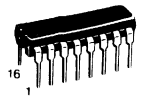
The MC10H350 is a member of Motorola's 10H family of high performance ECL logic. It consists of 4 translators with differential inputs and TTL outputs. The 3-state outputs can be disabled by applying a HIGH TTL logic level on the common OE input.

The MC10H350 is designed to be used primarily in systems incorporating both ECL and TTL logic operating off a common power supply. The separate V_{CC} power pins are not connected internally and thus isolate the noisy TTL V_{CC} runs from the relatively quiet ECL V_{CC} runs on the printed circuit board. The differential inputs allow the H350 to be used as an inverting or noninverting translator, or a differential line receiver. The H350 can also drive CMOS with the addition of a pullup resistor.

- Propagation Delay, 3.5 ns Typical
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

2

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{EE} = Gnd)	V_{CC}	7.0	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range—Plastic —Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

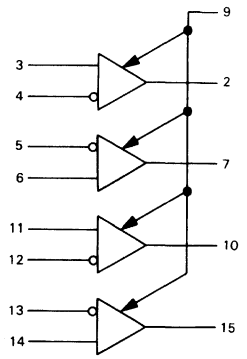
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%) (See Note 1)

Characteristic		Symbol	T_A = 0°C to 75°C Min	Max	Unit
Power Supply Current	TTL ECL	I_{CC}	— —	20 12	mA
Input Current High	Pin 9 Others	I_{IH}	— —	20 50	μA
Input Current Low	Pin 9 Others	I_{IL} I_{INL}	— —	-0.6 50	mA μA
Input Voltage High	Pin 9	V_{IH}	2.0	—	Vdc
Input Voltage Low	Pin 9	V_{IL}	—	0.8	Vdc
Differential Input Voltage (1) Pins 3–6, 11–14 (1)		V_{DIFF}	350	—	mV
Voltage Common Mode Pins 3–6, 11–14		V_{CM}	2.8	5.0	Vdc
Output Voltage High I_{OH} = 3.0 mA		V_{OH}	2.7	—	Vdc
Output Voltage Low I_{OL} = 20 mA		V_{OL}	—	0.5	Vdc
Short Circuit Current V_{OUT} = 0 V		I_{OS}	-60	-150	mA
Output Disable Current High V_{OUT} = 2.7 V		I_{OZH}	—	50	μA
Output Disable Current Low V_{OUT} = 0.5 V		I_{OZL}	—	-50	μA

(1) Common mode input voltage to pins 3–4, 5–6, 11–12, 13–14 must be between the values of 2.8 V and 5.0 V. This common mode input voltage range includes the differential input swing.
(2) For single ended use, apply 3.75 V (V_{BB}) to either input depending on output polarity required. Signal level range to other input is 3.3 V to 4.2 V.
(3) Any unused gates should have the inverting inputs tied to V_{CC} and the non-inverting inputs tied to ground to prevent output glitching.
(4) 1.0 V to 2.0 V w/25 pF into 500 ohms.

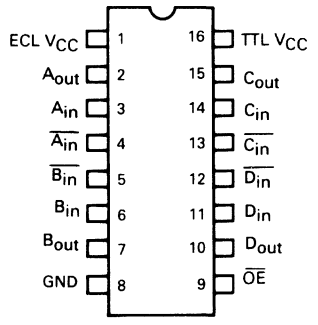
*Positive Emitter Coupled Logic

LOGIC DIAGRAM



V_{CC} (+5.0 Vdc) = Pins 1 and 16
Gnd = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

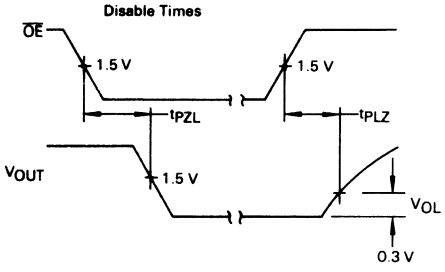
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%) (See Note 1)

Characteristic	Symbol	T_A = 0°C to 75°C Min	Max	Unit
AC PARAMETERS (C_L = 50 pF) (V_{CC} = 5.0 ±5%) (T_A = 0°C to 75°C)				
Propagation Delay Data	t_{pd}	1.5	5.0	ns
Rise Time	t_r	0.3	1.6	ns
Fall Time	t_f	0.3	1.6	ns
Output Disable Time	t_{pdLZ} t_{pdHZ}	2.0 2.0	6.0 6.0	ns
Output Enable Time	t_{pdZL} t_{pdZH}	2.0 2.0	8.0 8.0	ns

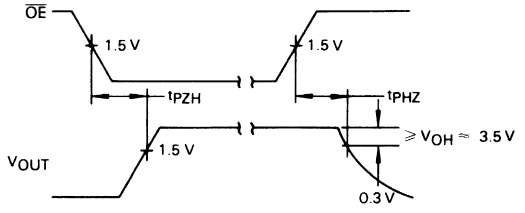
2

3-STATE SWITCHING WAVEFORMS

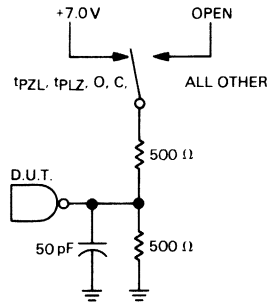
3-State Output Low Enable and Disable Times



3-State Output High Enable and Disable Times



TEST LOAD



*INCLUDES JIG AND PROBE CAPACITANCE

Application Note: Pin 9 is an $\overline{OE}$ and the 10H350 is disabled when $\overline{OE}$ is at V_{IH} or higher.

MOTOROLA

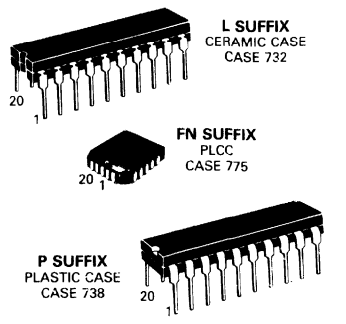
MC10H351

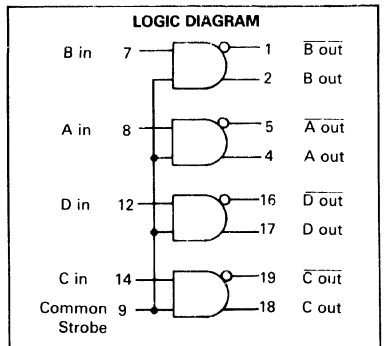
QUAD TTL/NMOS TO PECL* TRANSLATOR

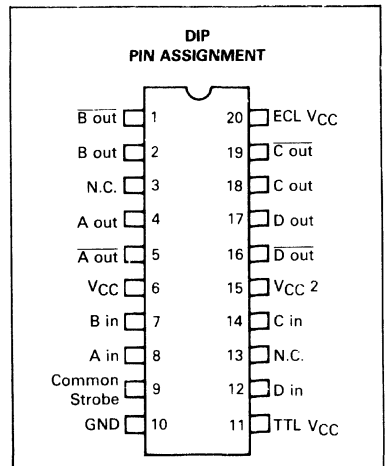
The MC10H351 is a quad translator for interfacing data between a saturated logic section and the PECL section of digital systems when only a +5.0 Vdc power supply is available. The MC10H351 has TTL/NMOS compatible inputs and PECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at a low logic level, it forces all true outputs to the PECL low logic state (≈ +3.2 V) and all inverting outputs to the PECL high logic state (≈ +4.1 V).

The MC10H351 can also be used with the MC10H350 to transmit and receive TTL/NMOS information differentially via balanced twisted pair lines.

- Single +5.0 V Power Supply
- All V_{CC} Pins Isolated On Chip
- Differentially Drive Balanced Lines
- t_{pd} = 1.3 nsec Typical







Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply	V_{CC}	0 to +7.0	Vdc
Input Voltage (V_{CC} = 5.0 V)	V_I	0 to V_{CC}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC1} = V_{CC2} = 5.0 V ± 5.0%)

Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	ECL	—	50	—	45	—	50	mA
	TTL	—	20	—	15	—	20	mA
Reverse Current Pins 7, 8, 12, 14 Pin 9	I_R	 — —	 25 100	 — —	 20 80	 — —	 25 100	μA
Forward Current Pins 7, 8, 12, 14 Pin 9	I_F	 — —	 −0.8 −3.2	 — —	 −0.6 −2.4	 — —	 −0.8 −3.2	mA
Input Breakdown Voltage	$V_{(BR)in}$	5.5	—	5.5	—	5.5	—	Vdc
Input Clamp Voltage (I_{in} = −18 mA)	V_I	—	−1.5	—	−1.5	—	−1.5	Vdc
High Output Voltage (1)	V_{OH}	3.98	4.16	4.02	4.19	4.08	4.27	Vdc
Low Output Voltage (1)	V_{OL}	3.05	3.37	3.05	3.37	3.05	3.37	Vdc
High Input Voltage	V_{IH}	2.0	—	2.0	—	2.0	—	Vdc
Low Input Voltage	V_{IL}	—	0.8	—	0.8	—	0.8	Vdc

(1) With V_{CC} at 5.0 V. V_{OH}/V_{OL} change 1:1 with V_{CC}.
*Positive Emitter Coupled Logic

AC PARAMETERS

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Propagation Delay (1)	t_{pd}	0.4	2.2	0.4	2.2	0.4	2.2	ns
Rise Time (20% to 80%)	t_r	0.4	1.9	0.4	2.0	0.4	2.1	ns
Fall Time (80% to 20%)	t_f	0.4	1.9	0.4	2.0	0.4	2.1	ns
Maximum Operating Frequency	f_{max}	150	—	150	—	150	—	MHz

(1) Propagation delay is measured on this circuit from +1.5 volts on the input waveform to the 50% point on the output waveform.

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to V_{CC} – 2.0 Vdc.

MOTOROLA

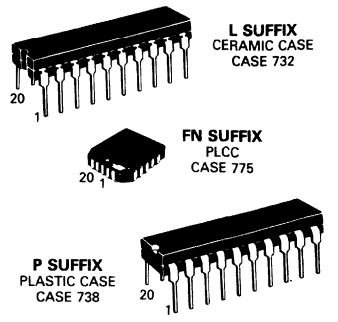
MC10H352

QUAD CMOS TO PECL* TRANSLATOR

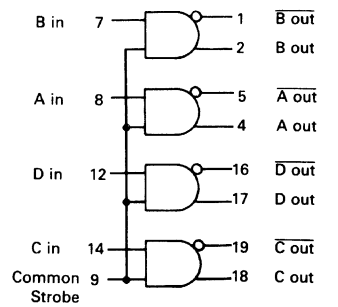
The MC10H352 is a quad translator for interfacing data between a CMOS logic section and the PECL section of digital systems when only a +5.0 Vdc power supply is available. The MC10H352 has CMOS compatible inputs and PECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at a low logic level, it forces all true outputs to the PECL low logic state (≈ +3.2 V) and all inverting outputs to the PECL high logic state (≈ +4.1 V).

The MC10H352 can also be used with the MC10H350 to transmit and receive CMOS information differentially via balanced twisted pair lines.

- Single +5.0 V Power Supply
- All V_{CC} Pins Isolated On Chip
- Differentially Drive Balanced Lines
- t_{pd} = 1.3 nsec Typical



LOGIC DIAGRAM



V_{CC} (+5.0 Vdc) = Pins 6, 11, 15, 20
Gnd = Pin 10

MAXIMUM RATINGS

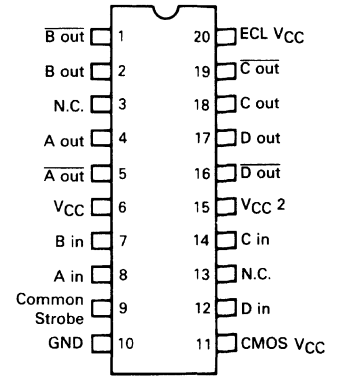
Characteristic	Symbol	Rating	Unit
Power Supply	V_{CC}	0 to +7.0	Vdc
Input Voltage (V_{CC} = 5.0 V)	V_I	0 to V_{CC}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC1} = V_{CC2} = 5.0 V ± 5.0%)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ECL	—	50	—	45	—	50	mA
	TTL	—	20	—	15	—	20	mA
Reverse Current Pins 7, 8, 12, 14 Pin 9	I_R	 — —	 25 100	 — —	 20 80	 — —	 25 100	μA
Forward Current Pins 7, 8, 12, 14 Pin 9	I_F	 — —	 −0.8 −3.2	 — —	 −0.6 −2.4	 — —	 −0.8 −3.2	mA
Input Breakdown Voltage	$V_{(BR)in}$	5.5	—	5.5	—	5.5	—	Vdc
Input Clamp Voltage (I_{in} = −18 mA)	V_I	—	−1.5	—	−1.5	—	−1.5	Vdc
High Output Voltage (1)	V_{OH}	3.98	4.16	4.02	4.19	4.08	4.27	Vdc
Low Output Voltage (1)	V_{OL}	3.05	3.37	3.05	3.37	3.05	3.37	Vdc
High Input Voltage	V_{IH}	3.15	—	3.15	—	3.15	—	Vdc
Low Input Voltage	V_{IL}	—	1.5	—	1.5	—	1.5	Vdc

(1) With V_{CC} at 5.0 V. V_{OH}/V_{OL} change 1:1 with V_{CC}.
*Positive Emitter Coupled Logic

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

AC PARAMETERS

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Propagation Delay (1)	t_{pd}	0.4	1.9	0.4	2.0	0.4	2.1	ns
Rise Time (20% to 80%)	t_r	0.4	1.9	0.4	2.0	0.4	2.1	ns
Fall Time (80% to 20%)	t_f	0.4	1.9	0.4	2.0	0.4	2.1	ns
Maximum Operating Frequency	f_{max}	150	—	150	—	150	—	MHz

(1) Propagation delay is measured on this circuit from $V_{CC}/2$ on the input waveform to the 50% point on the output waveform.

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to V_{CC} – 2.0 Vdc.

MOTOROLA

MC10H423

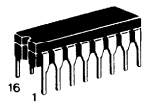
TRIPLE-3 INPUT BUS DRIVER WITH ENABLE

The MC10H423 is a triple 3 Input Bus Driver with a common enable.

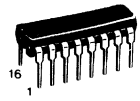
The MC10H423 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with V_{OL} = −2.1 Vdc so that the bus may be terminated to −2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10H423 are "turned off." This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to −2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10H423, higher impedance values may be used with this part. A typical 50 ohm bus is shown in Figure 1.

- Propagation Delay, 1.5 ns Typical
- Voltage Compensated
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- MECL 10K-Compatible



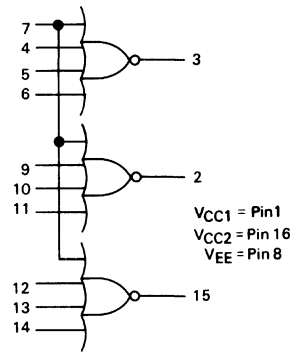
L SUFFIX
CERAMIC PACKAGE
CASE 620



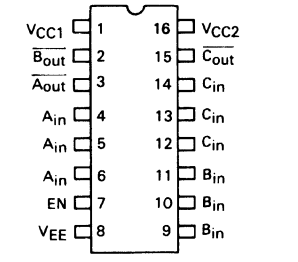
P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

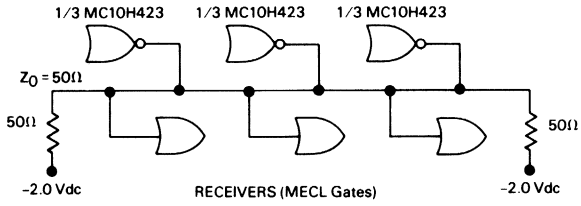
		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	60	—	56	—	60	mA
Input Current High Pins 4,5,6,9,10, 11,12,13,14 Pin 7	I_{inH}	 — —	 495 765	 — —	 310 475	 — —	 310 475	µA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−2.1	−2.03	−2.1	−2.03	−2.1	−2.03	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

AC PARAMETERS

Propagation Delay Pin 7 Only Exclude Pin 7	t_{pd}	 0.95 0.7	 1.85 1.45	 1.0 0.75	 2.0 1.6	 1.1 0.8	 2.1 1.7	ns
Rise Time	t_r	0.55	2.0	0.55	2.1	0.6	2.2	ns
Fall Time	t_f	0.55	2.0	0.55	2.1	0.6	2.2	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been establkished. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.1 volts.

FIGURE 1 — 50-OHM BUS DRIVER (25-OHM LOAD)



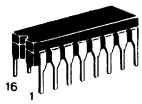
MOTOROLA

MC10H424

QUAD TTL-TO-ECL TRANSLATOR WITH AN ECL STROBE

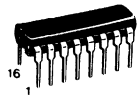
The MC10H424 is a Quad TTL-to-ECL translator with an ECL strobe. Power supply requirements are ground, +5.0 volts, and −5.2 volts.

- Propagation Delay, 1.5 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K — Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

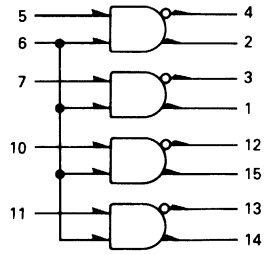
MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 5.0 V)	V_{EE}	−8.0 to 0	Vdc
Power Supply (V_{EE} = −5.2 V)	V_{CC}	0 to +7.0	Vdc
Input Voltage (ECL)	V_I	0 to V_{EE}	Vdc
Input Voltage (TTL)	V_I	0 to V_{CC}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ± 5%, V_{CC} = 5.0 V ± 5.0%)

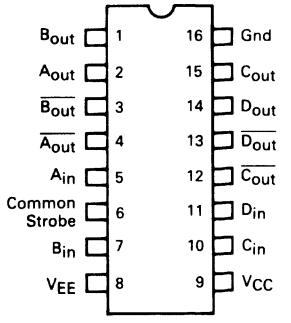
Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75°C Min	75°C Max	Unit
Negative Power Supply Drain Current	I_E	—	72	—	66	—	72	mAdc
Positive Power Supply Drain Current	I_{CCH}	—	16	—	16	—	18	mAdc
	I_{CCL}	—	25	—	25	—	25	mAdc
Reverse Current Pin 5,7,10,11	I_R	—	50	—	50	—	50	μAdc
Forward Current Pin 5,7,10,11	I_F	—	−3.2	—	−3.2	—	−3.2	mAdc
Input HIGH Current Pin 6	I_{inH}	—	450	—	310	—	310	μAdc
Input LOW Current Pin 6	I_{inL}	0.5	—	0.5	—	0.3	—	μAdc
Input Breakdown Voltage	$V_{(BR)in}$	5.5	—	5.5	—	5.5	—	Vdc
Input Clamp Voltage	V_I	—	−1.5	—	−1.5	—	−1.5	Vdc
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage Pin 5,7,10,11	V_{IH}	2.0	—	2.0	—	+2.0	—	Vdc
Low Input Voltage Pin 5,7,10,11	V_{IL}	—	0.8	—	0.8	—	0.8	Vdc
High Input Voltage Pin 6	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage Pin 6	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

LOGIC DIAGRAM



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (−5.2 Vdc) = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

AC PARAMETERS

Propagation Delay	t_{pd}							ns
Data		0.5	2.2	0.5	2.3	0.5	2.4	
Strobe		0.5	2.2	0.5	2.3	0.5	2.4	
Rise Time	t_r	0.5	2.0	0.5	2.0	0.5	2.2	ns
Fall Time	t_f	0.5	2.0	0.5	2.0	0.5	2.2	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been establkished. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

APPLICATIONS INFORMATION

The MC10H424 has TTL-compatible inputs, an ECL strobe and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low-logic level, it forces all true outputs to a MECL low-logic state and all inverting outputs to a MECL high-logic state.

An advantage of this device is that TTL-level information can be transmitted differentially, via balanced twisted pair lines, to MECL equipment, where the signal can be received by the MC10H115 or MC10H116 differential line receivers.

MOTOROLA

MC10H600
MC100H600

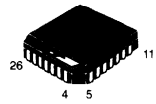
9-Bit TTL/ECL Translator

The MC10H/100H600 is a 9-bit, dual supply TTL to ECL translator. Devices in the Motorola 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

The H600 features both ECL and TTL logic enable controls for maximum flexibility.

The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

- 9-Bit Ideal for Byte-Parity Applications
- Flow-Through Configuration
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- ECL and TTL Enable Inputs
- Dual Supply
- 3.5 ns Max D to Q
- PNP TTL Inputs for Low Loading
- Choice of ECL Compatibility: MECL 10H (10Hxxx) or 100K (100Hxxx)



FN SUFFIX
PLASTIC PACKAGE
CASE 776

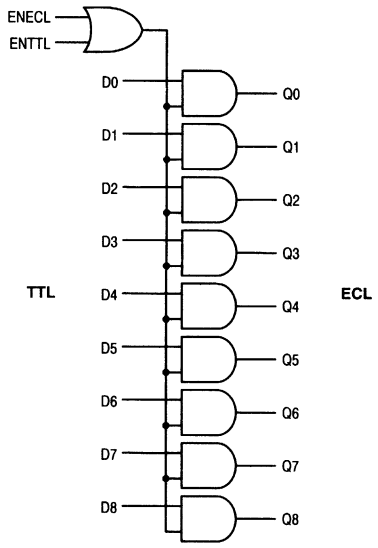
PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V_{CCE}	ECL V_{CC} (0 V)
V_{CCO}	ECL V_{CC} (0 V) — Outputs
V_{CCT}	TTL Supply (+5.0 V)
V_{EE}	ECL Supply (−5.2/−4.5 V)
D0–D8	Data Inputs (TTL)
Q0–Q8	Data Outputs (ECL)
ENECL	Enable Control (ECL)
ENTTL	Enable Control (TTL)

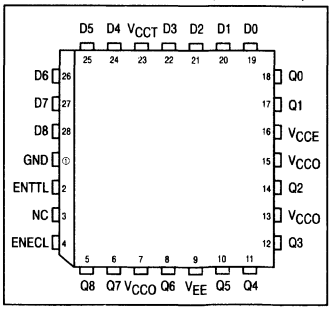
TRUTH TABLE

ENECL	ENTTL	D	Q
H	X	H	H
H	X	L	L
X	H	H	H
X	H	L	L
L	L	X	L

LOGIC SYMBOL



PINOUT: 28-LEAD PLCC (TOP VIEW)



DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
	Power Supply Current									
I_{EE}	ECL	10H		−125		−125		−125	mA	
		100H		−122		−123		−132		
I_{CCH} I_{CCL}	TTL			48 50		48 50		48 50	mA	

AC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output	D	1.4	3.0	1.5	3.2	1.7	3.5	ns	50 Ω to −2.0 V
		ENECL/ ENTTL	1.8	3.7	1.9	3.9	2.0	4.1	ns	50 Ω to −2.0 V
t_R t_F	Output Rise/Fall Time 20%−80%		0.5	1.5	0.5	1.5	0.5	1.5	ns	50 Ω to −2.0 V

10H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5%

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
I_{IH}	Input HIGH Current		225		145		145	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	−1170	−840	−1130	−810	−1070	−735	mV	
V_{IL}	Input LOW Voltage	−1950	−1480	−1950	−1480	−1950	−1450		
V_{OH}	Output HIGH Voltage	−1020	−840	−980	−810	−920	−735	mV	50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1950	−1630	−1950	−1630	−1950	−1600		

100H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −4.2 V to −5.5 V

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
I_{IH}	Input HIGH Current		225		145		145	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	−1165	−880	−1165	−880	−1165	−880	mV	
V_{IL}	Input LOW Voltage	−1810	−1475	−1810	−1475	−1810	−1475		
V_{OH}	Output HIGH Voltage	−1025	−880	−1025	−880	−1025	−880	mV	50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1810	−1620	−1810	−1620	−1810	−1620		

TTL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		2.0		2.0		V	
V_{IL}	Input LOW Voltage		0.8		0.8		0.8	V	
I_{IH}	Input HIGH Current		20		20		20	µA	V_{IN} = 2.7 V
			100		100		100		V_{IN} = 7.0 V
I_{IL}	Input LOW Current		−0.6		−0.6		−0.6	mA	V_{IN} = 0.5 V
V_{IK}	Input Clamp Voltage		−1.2		−1.2		−1.2	V	I_{IN} = −18 mA

2

MOTOROLA

MC10H601
MC100H601

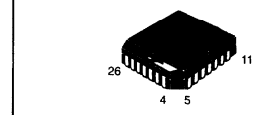
9-Bit ECL/TTL Translator

The MC10H/100H601 is a 9-bit, dual supply ECL to TTL translator. Devices in the Motorola 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

The devices feature a 48 mA TTL output stage, and AC performance is specified into both a 50 pF and 200 pF load capacitance. For the 3-state output disable, both ECL and TTL control inputs are provided, allowing maximum design flexibility.

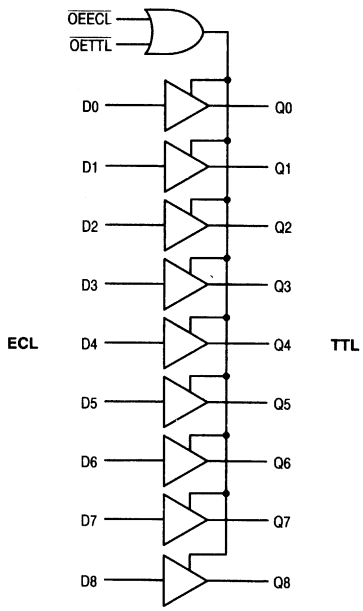
The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

- 9-Bit Ideal for Byte-Parity Applications
- 3-State TTL Outputs
- Flow-Through Configuration
- Extra TTL and ECL Power Pins to Minimize Switching Noise
- ECL and TTL 3-State Control Inputs
- Dual Supply
- 4.8 ns Max Delay into 50 pF, 9.6 ns into 200 pF (all outputs switching)
- PNP TTL Inputs for Low Loading
- Choice of ECL Compatibility: MECL 10H (10Hxxx) or 100K (100Hxxx)



FN SUFFIX
PLASTIC PACKAGE
CASE 776

LOGIC SYMBOL



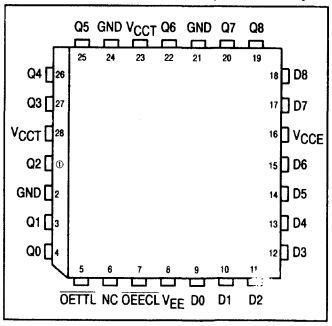
PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V_{CCE}	ECL V_{CC} (0 V)
V_{CCT}	TTL Supply (+5.0 V)
V_{EE}	ECL Supply (−5.2/−4.5 V)
D0–D8	Data Inputs (ECL)
Q0–Q8	Data Outputs (TTL)
$\overline{OEECL}$	3-State Control (ECL)
$\overline{OETTL}$	3-State Control (TTL)

TRUTH TABLE

$\overline{OEECL}$	$\overline{OETTL}$	D	Q
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

PINOUT: 28-LEAD PLCC (TOP VIEW)



DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
I_{EE}	Power Supply Current	ECL		−46		−46		−50	mA	
I_{CCH}		TTL		110		110		110	mA	
I_{CCL}				110		110		110	mA	
I_{CCZ}				105		105		105	mA	
I_{OS}	Output Short Circuit Current		−100	−225	−100	−225	−100	−225	mA	V_{OUT} = 0 V
I_{OZH}	Output Disable Current	HIGH		50		50		50	µA	V_{OUT} = 2.7 V
I_{OZL}		LOW		−50		−50		−50	µA	V_{OUT} = 0.5 V

AC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
t_{PLH}	Propagation Delay		1.7	4.8	1.7	4.8	1.7	4.8	ns	C_L = 50 pF
t_{PHL}	to Output		3.4	9.6	3.4	9.6	3.4	9.6	ns	C_L = 200 pF
t_{PLZ}	Output Disable Time	$\overline{OEECL}$	3.7	6.5	3.7	6.5	3.7	6.5	ns	C_L = 50 pF
t_{PHZ}			5.4	13	5.4	13	5.4	13	ns	C_L = 200 pF
t_{PLZ}		$\overline{OETTL}$	4.3	7.5	4.3	7.5	4.3	7.5	ns	C_L = 50 pF
t_{PHZ}			7.0	15	7.0	15	7.0	15	ns	C_L = 200 pF
t_{PZL}	Output Enable Time	$\overline{OEECL}$	3.5	6.0	3.5	6.0	3.5	6.0	ns	C_L = 50 pF
t_{PZH}			5.0	12	5.0	12	5.0	12	ns	C_L = 200 pF
t_{PZL}		$\overline{OETTL}$	4.2	7.0	4.2	7.0	4.2	7.0	ns	C_L = 50 pF
t_{PZH}			6.0	14	6.0	14	6.0	14	ns	C_L = 200 pF
t_R	Output Rise/Fall Time			1.2		1.2		1.2	ns	C_L = 50 pF
t_F	1.0 V−2.0 V			3.0		3.0		3.0	ns	C_L = 200 pF

10H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5%

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
I_{IH}	Input HIGH Current		225		145		145	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	−1170	−840	−1130	−810	−1070	−735	mV	
V_{IL}	Input LOW Voltage	−1950	−1480	−1950	−1480	−1950	−1450		

100H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −4.2 V to −5.5 V

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
I_{IH}	Input HIGH Current		225		145		145	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	−1165	−880	−1165	−880	−1165	−880	mV	
V_{IL}	Input LOW Voltage	−1810	−1475	−1810	−1475	−1810	−1475		

TTL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		2.0		2.0		V	
V_{IL}	Input LOW Voltage		0.8		0.8		0.8	V	
I_{IH}	Input HIGH Current		20		20		20	µA	V_{IN} = 2.7 V
			100		100		100		V_{IN} = 7.0 V
I_{IL}	Input LOW Current		−0.6		−0.6		−0.6	mA	V_{IN} = 0.5 V
V_{IK}	Input Clamp Voltage		−1.2		−1.2		−1.2	V	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.5		2.5		2.5		V	I_{OH} = −3.0 mA
		2.0		2.0		2.0		V	I_{OH} = −15 mA
V_{OL}	Output LOW Voltage		0.55		0.55		0.55	V	I_{OL} = 48 mA

2

MOTOROLA

MC10H602
MC100H602

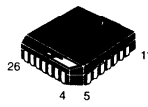
9-Bit Latch TTL/ECL Translator

The MC10H/100H602 is a 9-bit, dual supply TTL to ECL translator with latch. Devices in the Motorola 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

The H602 features D-type latches. Latching is controlled by Latch Enable (LEN), while the Master Reset input resets the latches. A post-latch logic enable is also provided (ENECL), allowing control of the output state without destroying latch data. All control inputs are ECL level.

The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

- 9-Bit Ideal for Byte-Parity Applications
- Flow-Through Configuration
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- 3.5 ns Max D to Q
- PNP TTL Inputs for Low Loading
- Choice of ECL Compatibility: MECL 10H (10Hxxx) or 100K (100Hxxx)



FN SUFFIX
PLASTIC PACKAGE
CASE 776

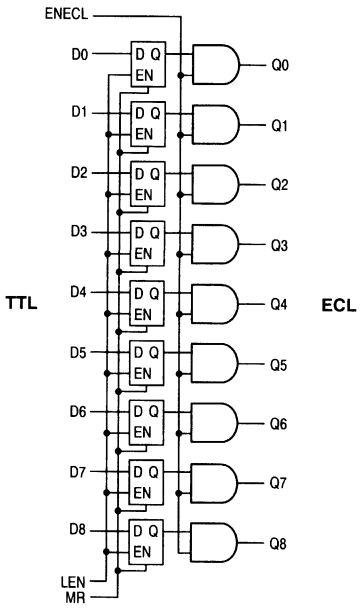
PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V_{CCE}	ECL V_{CC} (0 V)
V_{CCO}	ECL V_{CC} (0 V) — Outputs
V_{CCT}	TTL Supply (+5.0 V)
V_{EE}	ECL Supply (−5.2/−4.5 V)
D0–D8	Data Inputs (TTL)
Q0–Q8	Data Outputs (ECL)
ENECL	Enable Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

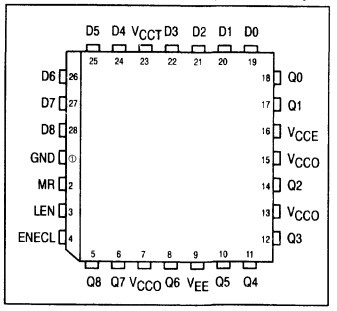
TRUTH TABLE

D	LEN	MR	ENECL	Q
L	L	L	H	L
H	L	L	H	H
X	H	L	H	Q_0
X	X	H	H	L
X	X	X	L	L

LOGIC SYMBOL



PINOUT: 28-LEAD PLCC (TOP VIEW)



DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
	Power Supply Current									
I_{EE}	ECL	10H		−125		−125		−125	mA	
		100H		−122		−123		−132		
I_{CCH}	TTL			48		48		48	mA	
I_{CCL}				50		50		50		

AC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
t_{PLH}	Propagation Delay	D	1.4	3.0	1.5	3.2	1.7	3.5	ns	
t_{PHL}	to Output	LEN	2.0	3.4	2.1	3.5	2.4	3.7		
		MR	2.0	3.4	2.1	3.5	2.5	3.9		
		ENECL	1.6	3.2	1.7	3.3	1.8	3.7		
t_s	Set-Up Time, D tc LEN		2.0		2.0		2.0		ns	
t_h	Hold Time, D to LEN		1.0		1.0		1.0		ns	
$t_{w(L)}$	LEN Pulse Width, LOW		2.0		2.0		2.0		ns	
t_R	Output Rise/Fall Time		0.5	1.5	0.5	1.5	0.5	1.5	ns	
t_F	20%−80%									

10H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5%

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
I_{IH}	Input HIGH Current		225		145		145	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	−1170	−840	−1130	−810	−1070	−735	mV	
V_{IL}	Input LOW Voltage	−1950	−1480	−1950	−1480	−1950	−1450		
V_{OH}	Output HIGH Voltage	−1020	−840	−980	−810	−920	−735	mV	50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1950	−1630	−1950	−1630	−1950	−1600		

100H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −4.2 V to −5.5 V

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
I_{IH}	Input HIGH Current		225		145		145	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	−1165	−880	−1165	−880	−1165	−880	mV	
V_{IL}	Input LOW Voltage	−1810	−1475	−1810	−1475	−1810	−1475		
V_{OH}	Output HIGH Voltage	−1025	−880	−1025	−880	−1025	−880	mV	50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1810	−1620	−1810	−1620	−1810	−1620		

TTL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		2.0		2.0		V	
V_{IL}	Input LOW Voltage		0.8		0.8		0.8	V	
I_{IH}	Input HIGH Current		20		20		20	µA	V_{IN} = 2.7 V
			100		100		100		V_{IN} = 7.0 V
I_{IL}	Input LOW Current		−0.6		−0.6		−0.6	mA	V_{IN} = 0.5 V
V_{IK}	Input Clamp Voltage		−1.2		−1.2		−1.2	V	I_{IN} = −18 mA

2

MOTOROLA

MC10H603
MC100H603

9-Bit Latch ECL/TTL Translator

The MC10H/100H603 is a 9-bit, dual supply ECL to TTL translator. Devices in the Motorola 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

The devices feature a 48 mA TTL output stage, and AC performance is specified into both a 50 pF and 200 pF load capacitance. Latching is controlled by Latch Enable (LEN), and Master Reset (MR) resets the latches. A HIGH on $\overline{OEECL}$ sends the outputs into the high impedance state. All control inputs are ECL level.

The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

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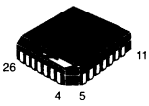
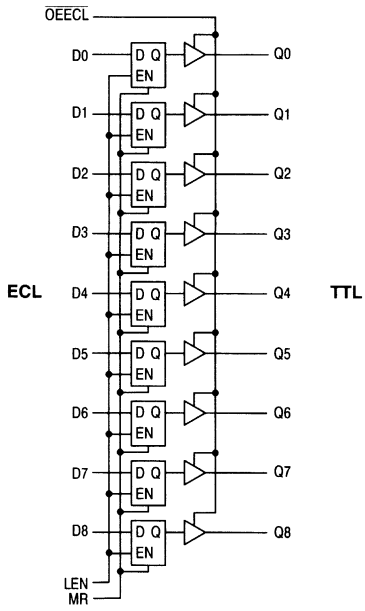
- 9-Bit Ideal for Byte-Parity Applications
- 3-State TTL Outputs
- Flow-Through Configuration
- Extra TTL and ECL Power Pins to Minimize Switching Noise
- Dual Supply
- 6.0 ns Max Delay into 50 pF, 12 ns into 200 pF (all outputs switching)
- PNP TTL Inputs for Low Loading
- Choice of ECL Compatibility: MECL 10H (10Hxxx) or 100K (100Hxxx)



FN SUFFIX
PLASTIC PACKAGE
CASE 776

LOGIC SYMBOL



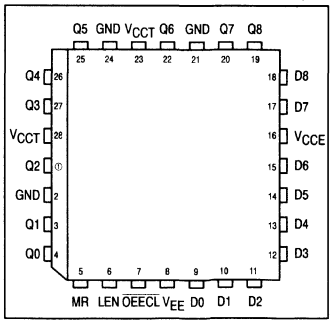
PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V_{CCE}	ECL V_{CC} (0 V)
V_{CCT}	TTL Supply (+5.0 V)
V_{EE}	ECL Supply (−5.2/−4.5 V)
D0–D8	Data Inputs (ECL)
Q0–Q8	Data Outputs (TTL)
$\overline{OEECL}$	3-State Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

TRUTH TABLE

D	LEN	MR	$\overline{OEECL}$	Q
L	L	L	L	L
H	L	L	L	H
X	H	L	L	Q_0
X	X	H	L	L
X	X	X	H	Z

PINOUT: 28-LEAD PLCC (TOP VIEW)



DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
I_{EE}	Power Supply Current	ECL	−45	−63	−45	−64	−45	−68	mA	
I_{CCH}		TTL	80	110	80	110	80	110	mA	
I_{CCL}			80	110	80	110	80	110	mA	
I_{CCZ}			80	110	80	110	80	110	mA	
I_{OS}	Output Short Circuit Current		−100	−225	−100	−225	−100	−225	mA	V_{OUT} = 0 V
I_{OZH}	Output Disable Current	HIGH		50		50		50	µA	V_{OUT} = 2.7 V
I_{OZL}		LOW		−50		−50		−50	µA	V_{OUT} = 0.5 V

AC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Parameter		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output	D	3.0 6.4	6.0 12	3.0 6.4	6.0 12	3.0 6.4	6.0 12	ns ns	C_L = 50 pF C_L = 200 pF
		LEN	3.5 7.0	6.5 13	3.5 7.0	6.5 13	3.5 7.0	6.5 13	ns ns	C_L = 50 pF C_L = 200 pF
		MR	3.0 6.0	6.0 12	3.0 6.0	6.0 12	3.0 6.0	6.0 12	ns ns	C_L = 50 pF C_L = 200 pF
t_s t_h $t_{w(L)}$	Set-Up Time, D to LEN Hold Time, D to LEN LEN Pulse Width, LOW		1.5 0.8 2.0		1.5 0.8 2.0		1.5 0.8 2.0		ns ns ns	
t_{PLZ} t_{PHZ}	Output Disable Time		2.5 4.2	6.5 13	2.5 4.2	6.5 13	2.5 4.2	6.5 13	ns ns	C_L = 50 pF C_L = 200 pF
t_{PZL} t_{PZH}	Output Enable Time		2.0 4.0	5.0 10	2.0 4.0	5.0 10	2.0 4.0	5.0 10	ns ns	C_L = 50 pF C_L = 200 pF
t_R t_F	Output Rise/Fall Time 1.0 V−2.0 V		0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	ns ns	C_L = 50 pF C_L = 200 pF

10H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5%

		0°C		25°C		75°C			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit	Condition
I_{IH}	Input HIGH Current		225		145		145	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	−1170	−840	−1130	−810	−1070	−735	mV	
V_{IL}	Input LOW Voltage	−1950	−1480	−1950	−1480	−1950	−1450		

100H ECL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −4.2 V to −5.5 V

		0°C		25°C		75°C			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit	Condition
I_{IH}	Input HIGH Current		225		145		145	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	−1165	−880	−1165	−880	−1165	−880	mV	
V_{IL}	Input LOW Voltage	−1810	−1475	−1810	−1475	−1810	−1475		

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TTL DC CHARACTERISTICS: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version); V_{EE} = −4.2 V to −5.5 V (100H version)

		0°C		25°C		75°C			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		2.0		2.0		V	
V_{IL}	Input LOW Voltage		0.8		0.8		0.8	V	
I_{IH}	Input HIGH Current		20		20		20	µA	V_{IN} = 2.7 V
			100		100		100		V_{IN} = 7.0 V
I_{IL}	Input LOW Current		−0.6		−0.6		−0.6	mA	V_{IN} = 0.5 V
V_{IK}	Input Clamp Voltage		−1.2		−1.2		−1.2	V	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.5		2.5		2.5		V	I_{OH} = −3.0 mA
		2.0		2.0		2.0		V	I_{OH} = −15 mA
V_{OL}	Output LOW Voltage		0.55		0.55		0.55	V	I_{OL} = 48 mA

MOTOROLA

MC10H604
MC100H604

REGISTERED HEX TTL TO ECL TRANSLATOR

Product Preview

Registered Hex TTL/ECL Translator

The MC10H/100H604 is a 6-bit, registered, dual supply TTL to ECL translator. The device features differential ECL outputs as well as a choice between either a differential ECL clock input or a TTL clock input. The asynchronous master reset control is an ECL level input.

With its differential ECL outputs and TTL inputs the H604 device is ideally suited for the transmit function of a HPPI bus type board-to-board interface application. The on chip registers simplify the task of synchronizing the data between the two boards.

The device is available in either ECL standard: the 10H device is compatible with MECL 10H logic levels while the 100H device is compatible with 100K logic levels.

- Differential 50Ω ECL Outputs
- Choice Between Differential ECL or TTL Clock Input
- Dual Power Supply
- Multiple Power and Ground Pins to Minimize Noise
- Specified Within-Device Skew

PIN NAMES

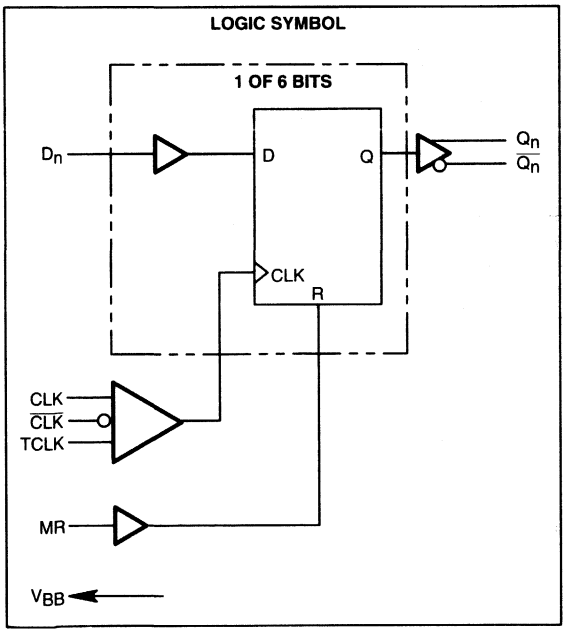
PIN	FUNCTION
D_0-D_5	TTL Data Inputs
CLK, $\overline{CLK}$	Differential ECL Clock Input
TCLK	TTL Clock Input
MR	ECL Master Reset Input
Q_0-Q_5	True ECL Outputs
$\overline{Q_0}-\overline{Q_5}$	Inverted ECL Outputs
V_{CCE}	ECL V_{CC}
V_{CCT}	TTL V_{CC}
GND	TTL Ground
V_{EE}	ECL V_{EE}

TRUTH TABLE

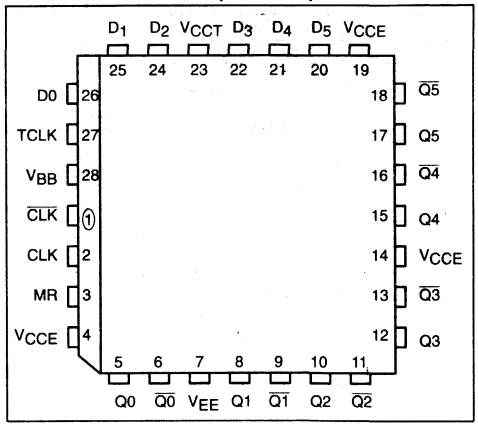
D_n	MR	TCLK/CLK	$Q_n + 1$
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

LOGIC SYMBOL



PINOUT: 28-LEAD PLCC (TOP VIEW)



DC CHARACTERISTICS: $V_{EE} = V_{EE}(Min)$ to $V_{EE}(Max)$; V_{CCE} = GND; $V_{CCT} = 5.0\ V \pm 10\%$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{EE}	ECL Power Supply Current 10H 100H			 130 130			 130 140			 130 150	mA	
I_{CCH}	TTL Power Supply Current			35			35			35	mA	
I_{CCL}				45			45			45	mA	

10H ECL DC CHARACTERISTICS: ($V_{CCT} = +5.0\ V \pm 10\%$; $V_{EE} = -5.20\ V \pm 5\%$)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			225			145			145	µA	
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA	
V_{IH}	Input HIGH Voltage	−1170		−840	−1130		−810	−1060		−720	mV	
V_{IL}	Input LOW Voltage	−1950		−1480	−1950		−1480	−1950		−1480	mV	
V_{BB}	Output Bias Voltage	−1380		−1270	−1350		−1230	−1310		−1190	mV	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	−1020 −1950		−840 −1630	−980 −1950		−810 −1630	−910 −1950		−720 −1595	mV	50 Ω to −2.0 V

100H ECL DC CHARACTERISTICS: ($V_{CCT} = +5.0\ V \pm 10\%$; $V_{EE} = -4.2\ V$ to $-5.5\ V$)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			225			145			145	µA	
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA	
V_{IH}	Input HIGH Voltage	−1165		−880	−1165		−880	−1165		−880	mV	
V_{IL}	Input LOW Voltage	−1810		−1475	−1810		−1475	−1810		−1475	mV	
V_{BB}	Output Bias Voltage	−1380		−1260	−1380		−1260	−1380		−1260	mV	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	−1025 −1810		−880 −1620	−1025 −1810		−880 −1620	−1025 −1810		−880 −1620	mV	50 Ω to −2.0 V

TTL DC CHARACTERISTICS: $V_{CCT} = 5.0\ V \pm 10\%$, $V_{EE} = -5.2\ V \pm 5\%$ (10H version); $V_{EE} = -4.2\ V$ to $-5.5\ V$ (100H version)

Symbol	Parameter	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0		 0.8	2.0		 0.8	2.0		 0.8	V V	
I_{IH}	Input HIGH Current			20 100			20 100			20 100	µA	$V_{IN} = 2.7\ V$ $V_{IN} = 7.0\ V$
I_{IL}	Input LOW Current			−0.6			−0.6			−0.6	mA	$V_{IN} = 0.5\ V$
V_{IK}	Input Clamp Voltage			−1.2			−1.2			−1.2	V	$I_{IN} = -18\ mA$

AC CHARACTERISTICS: $V_{EE} = V_{EE}(Min)$ to $V_{EE}(Max)$; V_{CCE} = GND; $V_{CCT} = 5.0\ V \pm 10\%$

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output CLK to Q TCLK to Q MR to Q	 1.5 2.0 1.5		 3.5 4.0 4.0	 1.5 2.0 1.5	 2.8 3.0 2.8	 3.5 4.0 4.0	 1.5 2.0 1.5		 3.5 4.0 4.0	ns	$C_L = 50\ pF$
t_S	Setup Time	1.5	0.5		1.5	0.5		1.5	0.5		ns	$C_L = 50\ pF$
t_H	Hold Time	1.5	0.5		1.5	0.5		1.5	0.5		ns	$C_L = 50\ pF$
t_{PW}	Minimum Pulse Width CLK, MR		1.0			1.0			1.0		ns	$C_L = 50\ pF$
V_{PP}	Minimum Input Swing					150					mV	
t_r t_f	Rise/Fall Times	0.3	1.0	2.0	0.3	1.0	2.0	0.3	1.0	2.0	ns	20% – 80%

MOTOROLA

MC10H605
MC100H605

Registered Hex ECL/TTL Translator

REGISTERED HEX ECL TO TTL TRANSLATOR

The MC10/100H605 is a 6-bit, registered, dual supply ECL to TTL translator. The device features differential ECL inputs for both data and clock. The TTL outputs feature balanced 24mA sink/source capabilities for driving transmission lines.

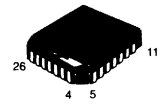
With its differential ECL inputs and TTL outputs the H605 device is ideally suited for the receive function of a HPPI bus type board-to-board interface application. The on chip registers simplify the task of synchronizing the data between the two boards.

A V_{BB} reference voltage is supplied for use with single-ended data or clock. For single-ended applications the V_{BB} output should be connected to the "bar" inputs ($\overline{Dn}$ or $\overline{CLK}$) and bypassed to ground via a 0.01 µF capacitor. To minimize the skew of the device differential clocks should be used.

The ECL level Master Reset pin is asynchronous and common to all flip-flops. A "HIGH" on the Master Reset forces the Q outputs "LOW".

The device is available in either ECL standard: the 10H device is compatible with MECL 10H logic levels while the 100H device is compatible with 100K logic levels.

- Differential ECL Data and Clock Inputs
- 48mA Sink, 15mA Source TTL Outputs
- Dual Power Supply
- Multiple Power and Ground Pins to Minimize Noise
- 700ps Within-Device Skew
- 2.0ns Part-to-Part Skew



FN SUFFIX
PLASTIC PACKAGE
CASE 776

2

PIN NAMES

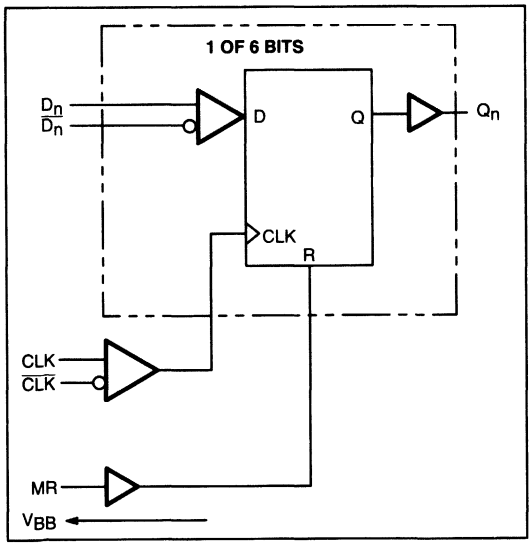
PIN	FUNCTION
D_0–D_5	True ECL Data Inputs
$\overline{D_0}$–$\overline{D_5}$	Inverted ECL Data Inputs
CLK, $\overline{CLK}$	Differential ECL Clock Input
MR	ECL Master Reset Input
Q_0–Q_5	TTL Outputs
V_{CCE}	ECL V_{CC}
V_{CCT}	TTL V_{CC}
GND	TTL Ground
V_{EE}	ECL V_{EE}

TRUTH TABLE

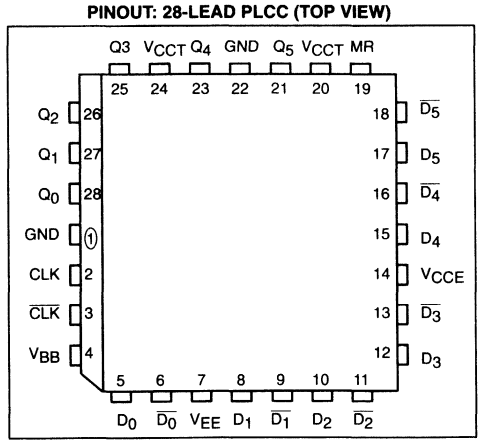
D_n	MR	TCLK/CLK	$Q_n + 1$
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

LOGIC SYMBOL



PINOUT: 28-LEAD PLCC (TOP VIEW)



10H ECL DC CHARACTERISTICS (V_{CCT} = +5.0 V ±10%; V_{EE} = −5.20 V ±5%)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{EE}	Supply Current		63	75		63	75		61	75	mA	
I_{IH}	Input High Current			225			145			145	µA	
I_{IL}	Input Low Current	0.5			0.5			0.5			µA	
V_{IH}	Input High Voltage	−1170		−840	−1130		−810	−1060		−720	mV	
V_{IL}	Input Low Voltage	−1950		−1480	−1950		−1480	−1950		−1450	mV	
V_{BB}	Output Bias Voltage	−1380		−1270	−1350		−1230	−1310		−1190	mV	
V_{Diff}	Input Differential Voltage	150			150			150			mV	
V_{max} CMRR	Input Common Mode Reject Range			0			0			0	mV	
V_{min} CMRR	Input Common Mode Reject Range	−2800 −3000 −3300			−2800 −3000 −3300			−2800 −3000 −3300			mV	V_{EE} = −4.94 V_{EE} = −5.20 V_{EE} = −5.46

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100H ECL DC CHARACTERISTICS (V_{CCT} = +5.0 V ±10%; V_{EE} = −4.2 V to −5.5 V)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{EE}	Supply Current		65	75		65	75		70	85	mA	
I_{IH}	Input High Current			225			145			145	µA	
I_{IL}	Input Low Current	0.5			0.5			0.5			µA	
V_{IH}	Input High Voltage	−1165		−880	−1165		−880	−1165		−880	mV	
V_{IL}	Input Low Voltage	−1810		−1475	−1810		−1475	−1810		−1475	mV	
V_{BB}	Output Bias Voltage	−1380		−1260	−1380		−1260	−1380		−1260	mV	
V_{Diff}	Input Differential Voltage	150			150			150			mV	
V_{max} CMRR	Input Common Mode Reject Range			0			0			0	mV	
V_{min} CMRR	Input Common Mode Reject Range	−2000 −2200 −2400 −2650 −2850			−2000 −2200 −2400 −2650 −2850			−2000 −2200 −2400 −2650 −2850			mV	V_{EE} = −4.20 V_{EE} = −4.50 V_{EE} = −4.80 V_{EE} = −5.20 V_{EE} = −5.50

* NOTE: DO NOT short the ECL inputs to the TTL V_{CC}.

TTL DC CHARACTERISTICS (V_{CCT} = +5.0 V ±10%; V_{EE} = −5.2 V ±5% (10H); V_{EE} = −4.2 V to −5.5 V (100H))

		0°C			25°C			85°C				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
I_{CCL}	Supply Current		65	75		65	75		65	75	mA	Outputs Low
I_{CCH}	Supply Current		65	75		65	75		65	75	mA	Outputs High
V_{OL}	Output Low Voltage			0.5			0.5			0.5	mV	I_{OL} = 24 mA
V_{OH}	Output High Voltage	2.5			2.5			2.5			mV	I_{OH} = 24 mA
I_{OS}	Output Short Circuit Current	100		225	100		225	100		225	mA	V_{OUT} = 0 V

AC TEST LIMITS (V_{CCT} = +5.0 V ±10%; V_{EE} = −5.2 V ±5% (10H); V_{EE} = −4.2 V to −5.5 V (100H))

		0°C			25°C			85°C				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
t_{PLH}	Propagation Delay CLK to Q (Diff) CLK to Q (SE)	 4.5 4.3	 5.3 5.3	 6.5 6.7	 4.5 4.3	 5.4 5.4	 6.5 6.7	 4.5 4.3	 5.6 5.6	 6.5 6.7	ns	Across P.S. and Temp C_L = 50 pF
t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE)	 4.0 3.8	 5.0 5.0	 6.0 6.2	 4.0 3.8	 5.1 5.1	 6.0 6.2	 4.0 3.8	 5.5 5.5	 6.0 6.2	ns	Across P.S. and Temp C_L = 50 pF
t_{PHL}	Propagation Delay MR to Q	2.5	4.9	7.0	2.5	5.2	7.0	3.0	5.8	7.5	ns	Across P.S. and Temp C_L = 50 pF
t_S	Setup Time	1.5			1.5			1.5			ns	
t_H	Hold Time	1.5			1.5			1.5			ns	
t_{PW}	Minimum Pulse Width CLK	1.0			1.0			1.0			ns	
t_{PW}	Minimum Pulse Width MR	1.0			1.0			1.0			ns	
V_{PP}	Minimum Input Swing	150			150			150			mV	Peak-to-Peak
t_r	Rise Time	0.7	1.0	1.5	0.7	1.0	1.5	0.7	1.0	1.5	ns	1 V to 2 V
t_f	Fall Time	0.5	0.7	1.2	0.5	0.7	1.2	0.5	0.7	1.2	ns	1 V to 2 V
t_{RR}	Reset/Recovery Time	2.5			2.5			2.5			ns	

MOTOROLA

MC10H606
MC100H606

Registered Hex TTL/PECL Translator

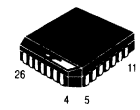
REGISTERED HEX TTL/PECL TRANSLATOR

The MC10/100H606 is a 6-bit, registered, single supply TTL to PECL translator. The device features differential PECL outputs as well as a choice between either a differential PECL clock input or a TTL clock input. The asynchronous master reset control is a PECL level input.

With its differential PECL outputs and TTL inputs the H606 device is ideally suited for the transmit function of a HPPI bus type board-to-board interface application. The on chip registers simplify the task of synchronizing the data between the two boards.

The device is available as an MC10H606 which is compatible with MECL 10H logic levels, and the MC100H606 which is compatible with 100K logic levels. Both use a V_{CC} of +5.0 volts.

- Differential 50 Ω ECL Outputs
- Choice Between Differential PECL or TTL Clock Input
- Single Power Supply
- Multiple Power and Ground Pins to Minimize Noise
- Specified Within-Device Skew



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

PIN NAMES

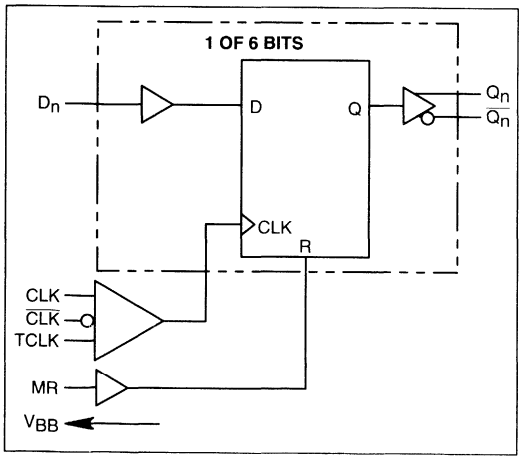
PIN	FUNCTION
D_0–D_5	TTL Data Inputs
CLK, $\overline{CLK}$	Differential PECL Clock Input
TCLK	TTL Clock Input
MR	PECL Master Reset Input
Q_0–Q_5	True PECL Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Inverted PECL Outputs
V_{CCE}	ECL V_{CC}
V_{CCT}	TTL V_{CC}
GND	TTL/PECL Ground

TRUTH TABLE

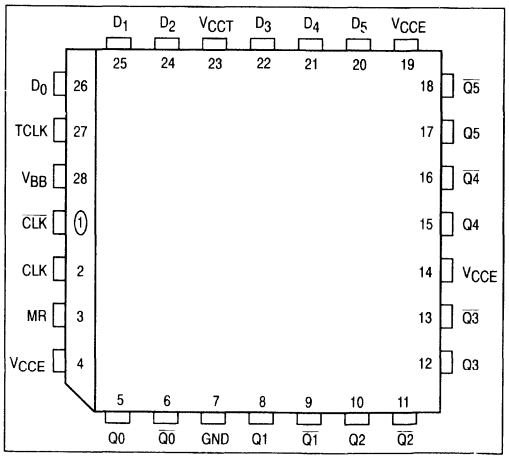
D_n	MR	TCLK/CLK	$Q_n + 1$
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

LOGIC DIAGRAM



PINOUT: 28-LEAD PLCC (TOP VIEW)



DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0 V ±5%)

		T_A = 0°C			T_A = + 25°C			T_A = + 85°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Condition
I_{CCTL}	Supply Current		18	30		18	30		18	30	mA	Outputs LOW
I_{CCTH}	Supply Current		13	25		13	25		13	25	mA	Outputs HIGH
I_{GND}	Supply Current		75	90		75	90		75	95	mA	

TTL DC CHARACTERISTICS (V_{CCT} = V_{EE} = 5.0 V ±5%)

		T_A = 0°C		T_A = 25°C		T_A = 85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		2.0		2.0		V	
V_{IL}	Input LOW Voltage		0.8		0.8		0.8	V	
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18 mA
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5 V

10H PECL DC CHARACTERISTICS (V_{CCT} = V_{EE} = 5.0 V ±5%)

		T_A = 0°C		T_A = 25°C		T_A = 85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
I_{INH}	Input HIGH Current		255		145		145	µA	
I_{INL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	3830	4160	3870	4190	3930	4280	mV	V_{CCT} = 5.0 V
V_{IL}	Input LOW Voltage	3050	3520	3050	3520	3050	3555	mV	V_{CCT} = 5.0 V
V_{OH}	Output HIGH Voltage	3980	4160	4020	4190	4080	4270	mV	V_{CCT} = 5.0 V
V_{OL}	Output LOW Voltage	3050	3370	3050	3370	3050	3400	mV	V_{CCT} = 5.0 V
V_{BB}	Output Bias Voltage	3620	3730	3650	3750	3690	3810	mV	V_{CCT} = 5.0 V

100H PECL DC CHARACTERISTICS (V_{CCT} = V_{EE} = 5.0 V ±5%)

		T_A = 0°C		T_A = 25°C		T_A = 85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
I_{INH}	Input HIGH Current		255		145		145	µA	
I_{INL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	3835	4120	3835	4120	3835	4120	mV	V_{CCT} = 5.0 V
V_{IL}	Input LOW Voltage	3190	3525	3190	3525	3190	3525	mV	V_{CCT} = 5.0 V
V_{OH}	Output HIGH Voltage	3975	4120	3975	4120	3975	4120	mV	V_{CCT} = 5.0 V
V_{OL}	Output LOW Voltage	3190	3380	3190	3380	3190	3380	mV	V_{CCT} = 5.0 V
V_{BB}	Output Bias Voltage	3620	3740	3620	3740	3620	3740	mV	V_{CCT} = 5.0 V

AC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0 V ±5%)

		T_A = 0°C			T_A = + 25°C			T_A = + 85°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Condition
t_{PD}	Propagation Delay TCLK++	1.75		3.75	1.75	3.00	3.75	1.75		3.75	ns	C_L = 50 pF
t_{PD}	Propagation Delay TCLK+–	1.75		3.75	1.75	3.00	3.75	1.75		3.75	ns	C_L = 50 pF
t_{PD}	Propagation Delay CLK++	1.50		3.50	1.50	2.50	3.50	1.50		3.50	ns	C_L = 50 pF
t_{PD}	Propagation Delay CLK+–	1.50		3.50	1.50	2.50	3.50	1.50		3.50	ns	C_L = 50 pF
t_{PD}	Propagation Delay MR+–	1.50		3.50	1.50	2.50	3.50	1.75		3.75	ns	C_L = 50 pF
t_S	Setup Time	1.5	0.5		1.5	0.5		1.5	0.5		ns	C_L = 50 pF
t_H	Hold Time	1.5	0.5		1.5	0.5		1.5	0.5		ns	C_L = 50 pF
t_{PW}	Minimum Pulse Width CLK	1.5			1.5	1.0		1.5			ns	C_L = 50 pF
t_{PW}	Minimum Pulse Width MR	1.5			1.5			1.5			ns	C_L = 50 pF
t_r	Rise Time			2.0		1.0	2.0			2.0	ns	C_L = 50 pF
t_f	Fall Time			2.0		1.0	2.0			2.0	ns	C_L = 50 pF
$t_{RES/REC}$	Reset/Recovery Time	2.5	2.0		2.5	2.0		2.5	2.0		ns	C_L = 50 pF

MOTOROLA

MC10H607
MC100H607

Advance Information

Registered Hex PECL/TTL Translator

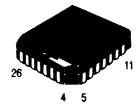
REGISTERED HEX PECL/TTL TRANSLATOR

The MC10H/100H607 is a 6-bit, registered PECL to TTL translator. The device features differential PECL inputs for both data and clock. The TTL outputs feature 48 mA sink, 24 mA source drive capability for driving high fanout loads or transmission lines. The asynchronous master reset control is an ECL level input.

With its differential PECL inputs and TTL outputs the H607 device is ideally suited for the receive function of a HPPI bus type board-to-board interface application. The on chip registers simplify the task of synchronizing the data between the two boards.

The device is available in eitner ECL standard: the 10H device is compatible with MECL 10H logic levels, with a V_{CC} of +5.0 volts, while the 100H device is compatible with 100K logic levels, with a V_{CC} of +5.0 volts.

- Differential ECL Data and Clock Inputs
- 48 mA Sink, 15 mA Source TTL Outputs
- Single Power Supply
- Multiple Power and Ground Pins to Minimize Noise
- Specified Within-Device Skew



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

TRUTH TABLE

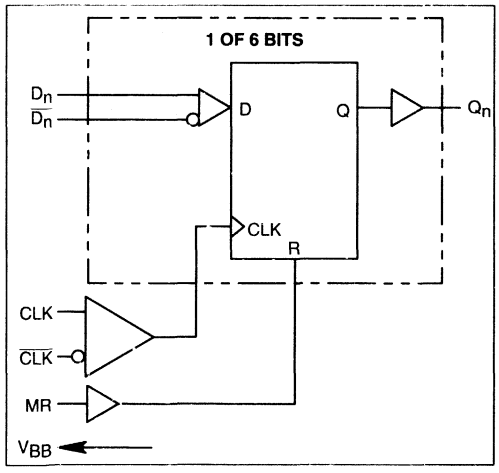
D_n	MR	CLK	$Q_n + 1$
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

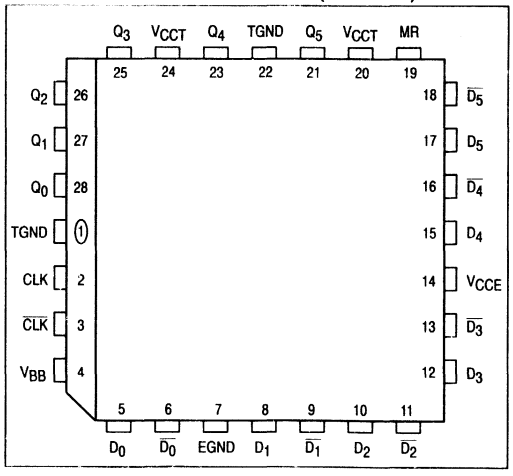
PIN NAMES

PIN	FUNCTION
D_0–D_5	True PECL Data Inputs
$\overline{D_0}$–$\overline{D_5}$	Inverted PECL Data Inputs
CLK, $\overline{CLK}$	Differential PECL Clock Input
MR	PECL Master Reset Input
Q_0–Q_5	TTL Outputs
V_{CCE}	PECL V_{CC}
V_{CCT}	TTL V_{CC}
TGND	TTL Ground
EGND	PECL Ground

LOGIC DIAGRAM



PINOUT: 28-LEAD PLCC (TOP VIEW)



This document contains information on a new product. Specifications and information herein are subject to change without notice.

DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0 V ±5%)

Symbol	Characteristic	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{EE}	ECL Power Supply Current 10H 100H		 70 65	 85 80		 70 70	 85 85		 70 75	 85 95	mA	
I_{CCL}	TTL Supply Current		100	120		100	120		100	120	mA	
I_{CCH}	TTL Supply Current		100	120		100	120		100	120	mA	

10H PECL DC CHARACTERISTICS (V_{CCT} = V_{EE} = 5.0 V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{INH}	Input HIGH Current		255		145		145	µA	
I_{INL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	3830	4160	3870	4190	3930	4280	mV	V_{CCT} = 5.0 V
V_{IL}	Input LOW Voltage	3050	3520	3050	3520	3050	3555	mV	V_{CCT} = 5.0 V
V_{BB}	Output Bias Voltage	3620	3730	3650	3750	3690	3810	mV	V_{CCT} = 5.0 V

NOTE: PECL V_{IL}, V_{IH}, V_{OL}, V_{OH}, V_{BB} are given for V_{CCT} = V_{CCE} = 5.0 V and will vary 1:1 with power supply.

100H PECL DC CHARACTERISTICS (V_{CCT} = V_{EE} = 5.0 V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input HIGH Current		255		145		145	µA	
I_{IL}	Input LOW Current		0.5		0.5		0.5	µA	
V_{IH}	Input HIGH Voltage	3835	4120	3835	4120	3835	4120	mV	V_{CCT} = 5.0 V
V_{IL}	Input LOW Voltage	3190	3525	3190	3525	3190	3525	mV	V_{CCT} = 5.0 V
V_{BB}	Output Bias Voltage	3620	3740	3620	3740	3620	3740	mV	V_{CCT} = 5.0 V

NOTE: PECL V_{IL}, V_{IH}, V_{OL}, V_{OH}, V_{BB} are given for V_{CCT} = V_{CCE} = 5.0 V and will vary 1:1 with power supply.

10H/100H TTL DC CHARACTERISTICS (V_{CCT} = V_{EE} = 5.0 V ±5%)

Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –15 mA I_{OH} = –24 mA
V_{OL}	Output LOW Voltage		0.55		0.55		0.55	V	I_{OL} = 48 mA

NOTE: DC levels such as V_{OH}, V_{OL}, etc., are standard for PECL and FAST devices, with the exceptions of: I_{OL} = 48 mA at 0.5 V_{OL}; and I_{OH} = 24 mA at 2.0 V_{OH}.

AC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0 V ±5%)

		T_A = 0°C			T_A = + 25°C			T_A = + 85°C				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
t_{PLH}[1] t_{PHL}	Propagation Delay to Output CLK to Q MR to Q		 7.3 7.3			 7.5 7.5			 8.5 8.5		ns	C_L = 50 pF
t_S	Setup Time		0.8			0.8			0.8		ns	
t_H	Hold Time		0.8			0.8			0.8		ns	
t_{PW}	Minimum Pulse Width CLK, MR		 1.0			 1.0			 1.0		ns	
V_{PP}	Minimum Input Swing	200	150		200	150		200	150		mV	
t_r	Rise Time		1.2			1.2			1.2		ns	0.8 – 2.0 V
t_f	Fall Time		1.2			1.2			1.2		ns	0.8 – 2.0 V

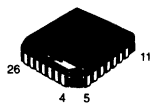
[1]Numbers are for both ++ and – – delay CLK to Q and MR to Q.

2

MOTOROLA

MC10H640
MC100H640

68030/040
PECL/TTL
CLOCK DRIVER



FN SUFFIX
PLASTIC PACKAGE
CASE 776

68030/040
PECL/TTL Clock Driver

2

The MC10H/100H640 generates the necessary clocks for the 68030, 68040 and similar microprocessors. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part-to-part skew, within-part skew and also duty cycle skew.

The user has a choice of using either TTL or PECL (referenced to +5.0 V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50 MHz and beyond, the inherent superiority of PECL (particularly differential PECL) as a means of clock signal distribution becomes increasingly evident. The 'H640 also uses differential PECL internally to achieve its superior skew characteristic.

The 'H640 includes divide-by-two and divide-by-four stages, both to achieve the necessary duty cycle skew and to generate MPU clocks as required. A typical 50 MHz processor application would use an input clock running at 100 MHz, thus obtaining output clocks at 50 MHz and 25 MHz (see Logic Symbol).

The 10H version is compatible with MECL 10H ECL logic levels, while the 100H version is compatible with 100K levels (referenced to +5.0 V).

Function

Reset (R): LOW on RESET forces all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

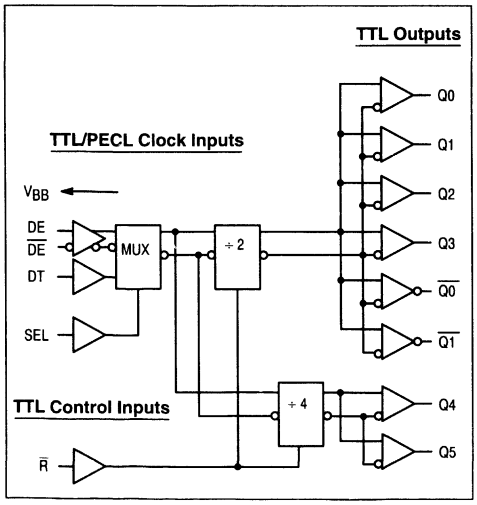
Power-Up: The device is designed to have the POS edges of the ÷2 and ÷4 outputs synchronized at power up.

Select (SEL): LOW selects the ECL input source (DE/$\overline{DE}$). HIGH selects the TTL input source (DT).

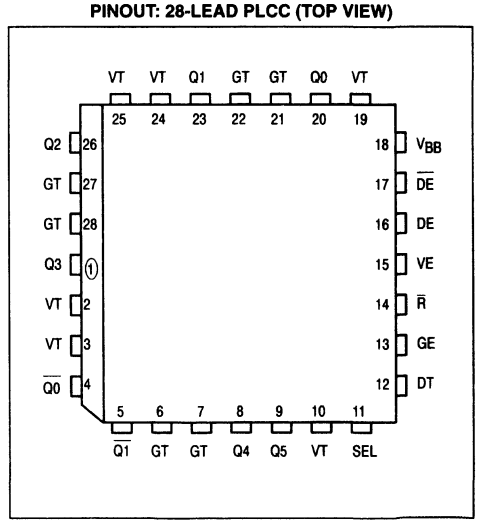
The 'H640 also contains circuitry to force a stable state of the PECL input differential pair, should both sides be left open. In this case, the DE side of the input is pulled LOW, and $\overline{DE}$ goes HIGH.

- Generates Clocks for 68030/040
- Meets 030/040 Skew Requirements
- TTL or PECL Input Clock
- Extra TTL and ECL Power/Ground Pins
- Asynchronous Reset
- Single +5.0 V Supply
- Choice of ECL Compatibility:
  MECL 10H (10Hxxx) or 100K (100Hxxx)

LOGIC SYMBOL



PINOUT: 28-LEAD PLCC (TOP VIEW)



PIN NAMES

PIN	FUNCTION
GT	TTL Ground (0 V)
VT	TTL V_{CC} (+5.0 V)
VE	PECL V_{CC} (+5.0 V)
GE	PECL Ground (0 V)
DE, $\overline{DE}$	PECL Signal Input (positive PECL)
V_{BB}	V_{BB} Reference Output
DT	TTL Signal Input
QN, $\overline{QN}$	Signal Outputs (TTL)
SEL	Input Select (TTL)
$\overline{R}$	Reset (TTL)

AC CHARACTERISTICS: VT = VE = 5.0 V ±5%

			0°C		25°C		85°C			
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH}	Propagation Delay PECL DE/$\overline{DE}$ to Output	Q0 – Q3	4.9	5.9	4.9	5.9	5.2	6.2	ns	C_L = 25 pF
t_{PLH}	Propagation Delay TTL DT to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	C_L = 25 pF
tskwd*	Within-Device Skew			0.5		0.5		0.5	ns	C_L = 25 pF
t_{PLH}	Propagation Delay PECL DE/$\overline{DE}$ to Output	$\overline{Q0}$, $\overline{Q1}$	4.9	5.9	4.9	5.9	5.2	6.2	ns	C_L = 25 pF
t_{PLH}	Propagation Delay TTL DT to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	C_L = 25 pF
t_{PLH}	Propagation Delay PECL DE/$\overline{DE}$ to Output	Q4, Q5	4.9	5.9	4.9	5.9	5.2	6.2	ns	C_L = 25 pF
t_{PLH}	Propagation Delay TTL DT to Output		5.0	6.0	5.0	6.0	5.3	6.3	ns	C_L = 25 pF
t_{PD}	Propagation Delay $\overline{R}$ to Output	All Outputs	4.3	6.3	4.3	6.3	5.0	7.0	ns	C_L = 25 pF
t_R t_F	Output Rise/Fall Time 0.8 V – 2.0 V	All Outputs	0.5	2.5 2.5	0.5	2.5 2.5	0.5	2.5 2.5	ns	C_L = 25 pF
f_{max}	Maximum Input Frequency		135		135		135		MHz	C_L = 25 pF
t_{pw}	Minimum Pulse Width		1.5		1.5		1.5		ns	
t_{rr}	Reset Recovery Time		1.25		1.25		1.25		ns	

* Within-Device Skew defined as identical transitions on similar paths through a device.

V_{CC} and C_{LOAD} Ranges to Meet Duty Cycle Requirement: 0°C ≤ T_A ≤ 85°C Output Duty cycle measured relative to 1.5 V

Symbol	Characteristic		Min	Nom	Max	Unit	Condition
	Range of V_{CC} and C_L to meet minimum pulse width (HIGH or LOW) = 11.5 ns at f_{out} ≤ 40 MHz	V_{CC} C_L	4.75 10	5.0	5.25 50	V pF	Q0–Q3 $\overline{Q0}$ – $\overline{Q1}$
	Range of V_{CC} and C_L to meet minimum pulse width (HIGH or LOW) = 9.5 ns at 40 MHz < f_{out} ≤ 50 MHz	V_{CC} C_L	4.875 15	5.0	5.125 27	V pF	Q0 – Q3

DC CHARACTERISTICS: VT = VE = 5.0 V ±5%

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{EE}	Power Supply Current	PECL		57		57		57	mA	VE Pin
I_{CCH}		TTL		30		30		30	mA	Total all VT pins
I_{CCL}				30		30		30	mA	

TTL DC CHARACTERISTICS: VT = VE = 5.0 V ±5%

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		−0.6		−0.6		−0.6	mA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = −3.0 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24 mA
V_{IK}	Input Clamp Voltage		−1.2		−1.2		−1.2	V	I_{IN} = −18 mA
I_{OS}	Output Short Circuit Current	−100	−225	−100	−225	−100	−225	mA	V_{OUT} = 0 V

10H PECL DC CHARACTERISTICS: VT = VE = 5.0 V ±5%

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	µA	
V_{IH}* V_{IL}*	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V	VE = 5.0 V
V_{BB}*	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	

*NOTE: PECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for V_{CC} = 5.0 V.

100H PECL DC CHARACTERISTICS: VT = VE = 5.0 V ±5%

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	µA	
V_{IH}* V_{IL}*	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	VE = 5.0 V
V_{BB}*	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	

*NOTE: PECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for V_{CC} = 5.0 V.

DUTY CYCLE CONTROL

To maintain a duty cycle of ±5% at 50 MHz, limit the load capacitance and/or power supply variation as shown in Figures 1 and 2. For a ±2.5% duty cycle limit, see Figures 3 and 4. Figures 5 and 6 show duty cycle variation with temperature. Figure 7 shows typical TPD versus load. Figure 8 shows reset recovery time. Figure 9 shows output states after power up.

Best duty cycle control is obtained with a single μP load and minimum line length.

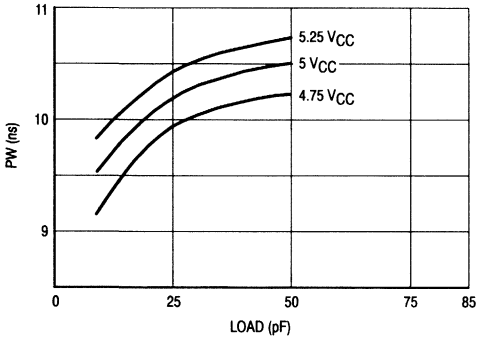


Figure 1. Positive Pulse Width at 25°C Ambient and 50 MHz Out

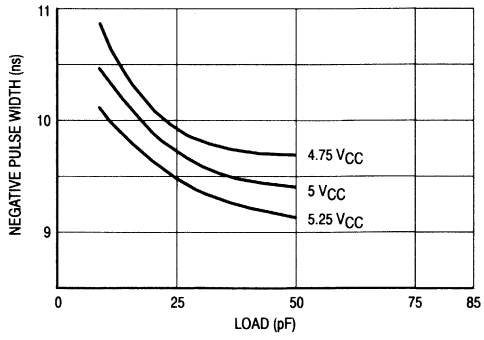


Figure 2. Negative Pulse Width @ 50 MHz Out and 25°C Ambient

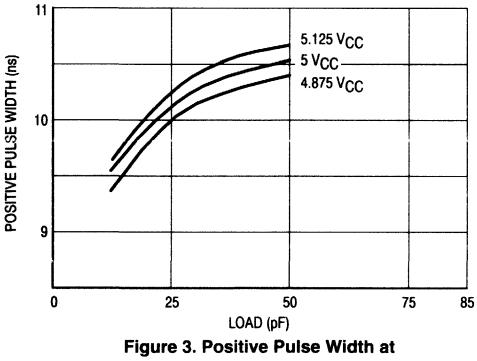


Figure 3. Positive Pulse Width at 25°C Ambient at 50 MHz Out

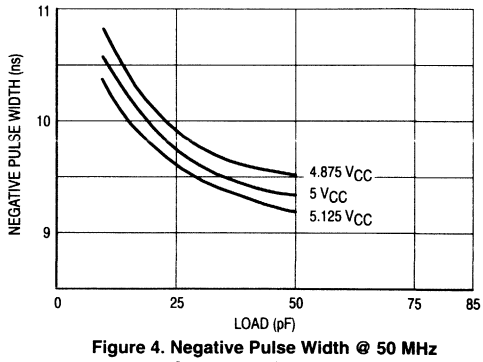


Figure 4. Negative Pulse Width @ 50 MHz Out and 25°C Ambient

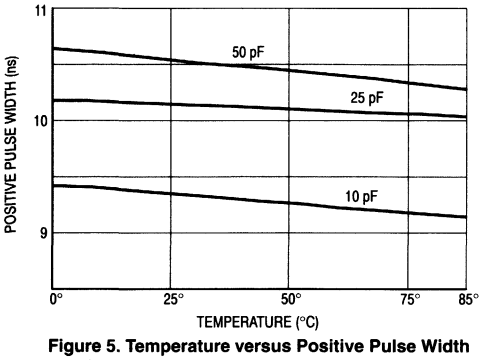


Figure 5. Temperature versus Positive Pulse Width for MC100H640 at 50 MHz and +5.0 V V_{CC}

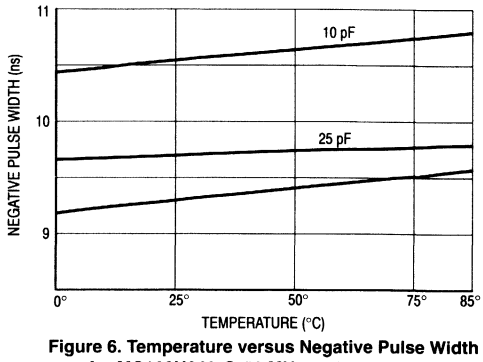


Figure 6. Temperature versus Negative Pulse Width for MC100H640 @ 50 MHz and +5.0 V V_{CC}

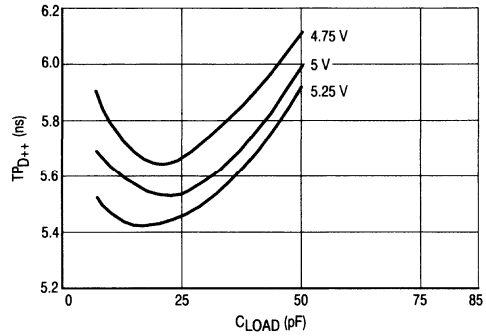


Figure 7. TP versus Load Typical at T_A = 25°C

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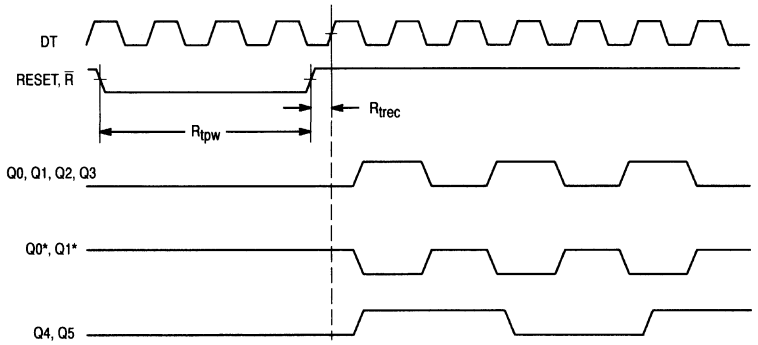
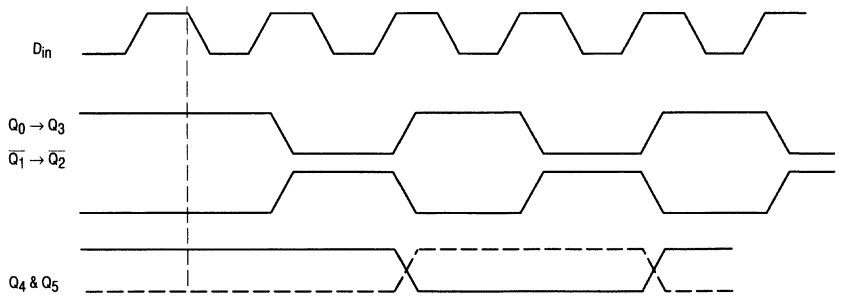


Figure 8. MC10H/100H640 Clock Phase and Reset Recovery Time After Reset Pulse



AFTER POWER UP
OUTPUTS Q_4 & Q_5 WILL SYN WITH POSITIVE EDGES OF D_{in} & $Q_0 \rightarrow Q_3$ & NEGATIVE EDGES OF $\overline{Q_0}$ & $\overline{Q_1}$

Figure 9.

MOTOROLA

MC10H641
MC100H641

Single Supply PECL/TTL 1:9 Clock Distribution Chip

SINGLE SUPPLY PECL/TTL 1:9 CLOCK DISTRIBUTION CHIP

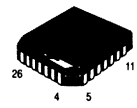
The MC10H/100H641 is a single supply, low skew translating 1:9 clock driver. Devices in the Motorola H600 translator series utilize the 28-lead PLCC for optimal power pinning, signal flow through and electrical performance.

The device features a 24 mA TTL output stage, with AC performance specified into a 50 pF load capacitance. A latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pulldown) the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW. Both the LEN and $\overline{EN}$ pins are positive PECL inputs.

The V_{BB} output is provided in case the user wants to drive the device with a single-ended input. For single-ended use the V_{BB} should be connected to the $\overline{D}$ input and bypassed with a 0.01 µF capacitor.

The 10H version of the H641 is compatible with positive MECL 10H logic levels. The 100H version is compatible with positive 100K levels.

- PECL-TTL Version of Popular ECLinPS E111
- Low Skew
- Guaranteed Skew Spec
- Latched Input
- Differential PECL Internal Design
- V_{BB} Output for Single-Ended Use
- Single +5 V Supply
- Logic Enable
- Extra Power and Ground Supplies
- Separate PECL and TTL Supply Pins
- Choice of PECL Compatibility: MECL 10H (10Hxxx) or 100K (100Hxxx)

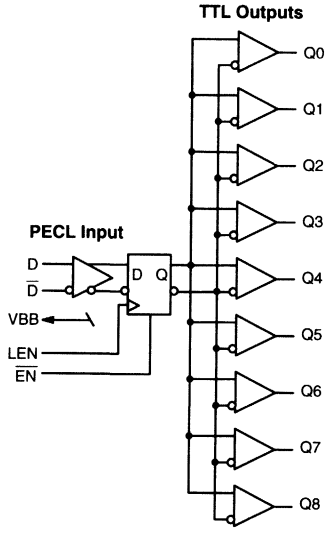


FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

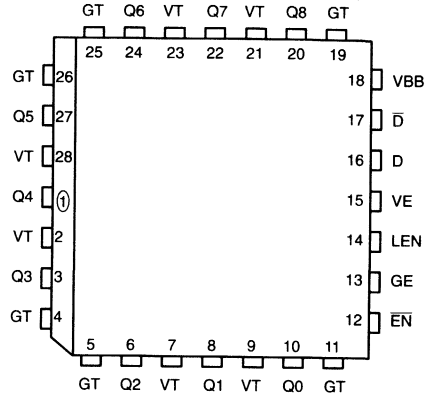
PIN NAMES

PIN	FUNCTION
GT, VT	TTL GND, TTL V_{CC}
GE, VE	PECL GND, PECL V_{CC}
D, $\overline{D}$	Signal Input (Positive PECL)
V_{BB}	V_{BB} Reference Output (Positive PECL)
Q0–Q8	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (Positive PECL)
LEN	Latch Enable Input (Positive PECL)

LOGIC DIAGRAM



Pinout: 28-Lead PLCC (Top View)



DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	T_A = 0°C			T_A = + 25°C			T_A = + 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{EE}	Power Supply Current PECL		24	30		24	30		24	30	mA	
I_{CCH}	TTL		24	30		24	30		24	30	mA	
I_{CCL}			27	35		27	35		27	35	mA	

TTL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.5		2.5		2.5		V	I_{OH} = –15 mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24 mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0 V

2

10H PECL DC CHARACTERISTICS

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input HIGH Current		225		175		175	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	3.83	4.16	3.87	4.19	3.94	4.28	V	VE = 5.0 V[1]
V_{IL}	Input LOW Voltage	3.05	3.52	3.05	3.52	3.05	3.55	V	VE = 5.0 V[1]
V_{BB}	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	VE = 5.0 V[1]

100H PECL DC CHARACTERISTICS

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input HIGH Current		225		175		175	µA	
I_{IL}	Input LOW Current	0.5		0.5		0.5		µA	
V_{IH}	Input HIGH Voltage	3.835	4.120	3.835	4.120	3.835	4.120	V	VE = 5.0 V[1]
V_{IL}	Input LOW Voltage	3.190	3.525	3.190	3.525	3.190	3.525	V	VE = 5.0 V[1]
V_{BB}	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	VE = 5.0 V[1]

1 PECL V_{IH}, V_{IL}, and V_{BB} are referenced to VE and will vary 1:1 with the power supply. The levels shown are for VE = 5.0 V.

AC CHARACTERISTICS (V_T = V_E = 5.0 V ±5%)

Symbol	Characteristic	T_J = 0°C			T_J = + 25°C			T_J = + 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay D to Q	5.00 5.36	5.50 5.86	6.00 6.36	4.86 5.27	5.36 5.77	5.86 6.27	5.08 5.43	5.58 5.93	6.08 6.43	ns	C_L = 50 pF[1]
t_{skew}	Device Skew Part-to-Part Output-to-Output			 1.0 0.5			 1.0 0.5			 1.0 0.5	ns	 C_L = 50 pF[2] C_L = 50 pF[3]
t_{PLH} t_{PHL}	Propagation Delay LEN to Q	4.9		6.9	4.9		6.9	5.0		7.0	ns	C_L = 50 pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{EN}$ to Q	5.0		7.0	4.9		6.9	5.0		7.0	ns	C_L = 50 pF
t_r t_f	Output Rise/Fall 0.8 V to 2.0 V			1.7 1.6			1.7 1.6			1.7 1.6	ns	C_L = 50 pF
f_{MAX}	Max Input Frequency	65			65			65			MHz	C_L = 50 pF[4]
t_{REC}	Recovery Time $\overline{EN}$	1.25			1.25			1.25			ns	
t_S	Setup Time	0.75	0.50		0.75	0.50		0.75	0.50		ns	
t_H	Hold Time	0.75	0.50		0.75	0.50		0.75	0.50		ns	

1 Propagation delay measurement guaranteed for junction temperatures. Measurements performed at 50 MHz input frequency.
2 Skew window guaranteed for a single temperature across a V_{CC} = V_T = V_E of 4.75 V to 5.25 V (See Application Note in this data sheet).
3 Output-to-output skew is specified for identical transitions through the device.
4 Frequency at which output levels will meet a 0.8 V to 2.0 V minimum swing.

2

Determining Skew for a Specific Application

The H641 has been designed to meet the needs of very low skew clock distribution applications. In order to optimize the device for this application special considerations are necessary in the determining of the part-to-part skew specification limits. Older standard logic devices are specified with relatively slack limits so that the device can be guaranteed over a wide range of potential environmental conditions. This range of conditions represented all of the potential applications in which the device could be used. The result was a specification limit that in the vast majority of cases was extremely conservative and thus did not allow for an optimum system design. For non-critical skew designs this practice is acceptable, however as the clock speeds of systems increase overly conservative specification limits can kill a design.

The following will discuss how users can use the information provided in this data sheet to tailor a part-to-part skew specification limit to their application. The skew determination process may appear somewhat tedious and time consuming, however if the utmost in performance is required this procedure is necessary. For applications which do not require this level of skew performance a generic part-to-part skew limit of 2.5 ns can be used. This limit is good for the entire ambient temperature range, the guaranteed V_{CC} (V_T, V_E) range and the guaranteed operating frequency range.

Temperature Dependence

A unique characteristic of the H641 data sheet is that the AC parameters are specified for a junction temperature rather than the usual ambient temperature. Because very few designs will actually utilize the entire commercial temperature range of a device a tighter propagation delay window can be established given the smaller temperature range. Because the junction temperature and not the ambient temperature is what affects the performance of the device the parameter limits are specified for junction temperature. In addition the relationship between the ambient and junction temperature will vary depending on the frequency, load and board environment of the application. Since these factors are all under the control of the user it is impossible to provide specification limits for every possible application. Therefore a baseline specification was established for specific junction temperatures and the information that follows will allow these to be tailored to specific applications.

Since the junction temperature of a device is difficult to measure directly, the first requirement is to be able to "translate" from ambient to junction temperatures. The standard method of doing this is to use the power dissipation of the device and the thermal resistance of the package. For a TTL output device the power dissipation will be a function of the load capacitance and the frequency of the output. The total power dissipation of a device can be described by the following equation:

$$P_D \text{ (watts)} = I_{CC} \text{ (no load)} * V_{CC} + V_S * V_{CC} * f * C_L * \#\text{ Outputs}$$

where:

V_S= Output Voltage Swing = 3 V
f = Output Frequency
C_L = Load Capacitance
$I_{CC} = I_{EE} + I_{CCH}$

Figure 1 plots the I_{CC} versus Frequency of the H641 with no load capacitance on the output. Using this graph and the information specific to the application a user can determine the power dissipation of the H641.

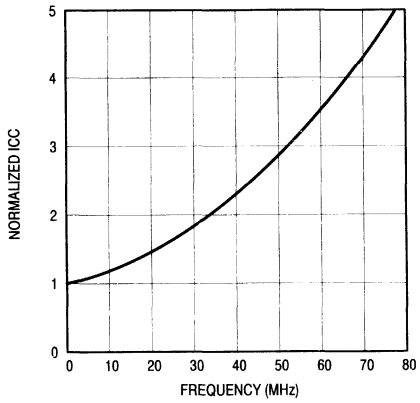


Figure 1. I_{CC} versus f (No Load)

Figure 2 illustrates the thermal resistance (in °C/W) for the 28-lead PLCC under various air flow conditions. By reading the thermal resistance from the graph and multiplying by the power dissipation calculated above the junction temperature increase above ambient of the device can be calculated.

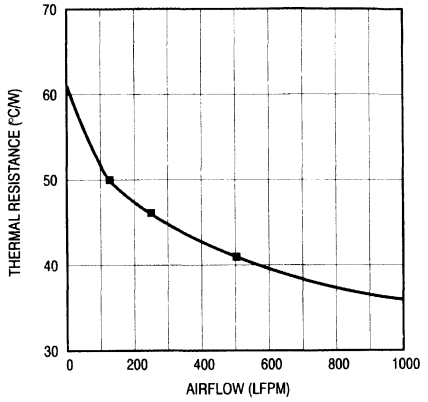


Figure 2. ∅ja versus Air Flow

Finally taking this value for junction temperature and applying it to Figure 3 allows the user to determine the propagation delay for the device in question. A more common use would be to establish an ambient temperature range for the H641's in the system and utilize the above methodology to determine the potential increased skew of the distribution network. Note that for this information if the T_{PD} versus Temperature curve were linear the calculations would not be required. If the curve were linear over all temperatures a simple temperature coefficient could be provided.

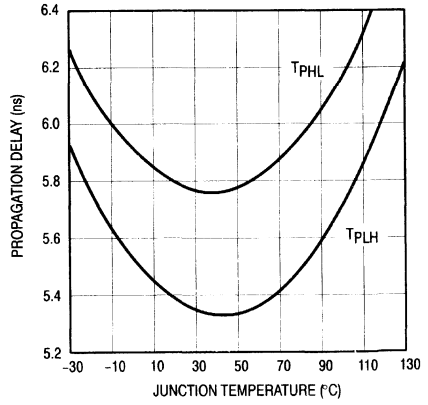


Figure 3. T_{PD} versus Junction Temperature

V_{CC} Dependence

TTL and CMOS devices show a significant propagation delay dependence with V_{CC}. Therefore the V_{CC} variation in a system will have a direct impact on the total skew of the clock distribution network. When calculating the skew between two devices on a single board it is very likely an assumption of identical V_{CC}'s can be made. In this case the number provided in the data sheet for part-to-part skew would be overly conservative. By using Figure 4 the skew given in the data sheet can be reduced to represent a smaller or zero variation in V_{CC}. The delay variation due to the specified V_{CC} variation is ≈270 ps. Therefore, the 1ns window on the data sheet can be reduced by 270 ps if the devices in question will always experience the same V_{CC}. The distribution of the propagation delay ranges given in the data sheet is actually a composite of three distributions whose means are separated by the fixed difference in propagation delay at the typical, minimum and maximum V_{CC}.

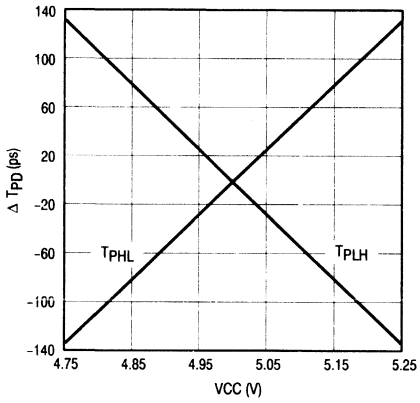


Figure 4. ΔT_{PD} versus V_{CC}

Capacitive Load Dependence

As with V_{CC} the propagation delay of a TTL output is intimately tied to variation in the load capacitance. The skew specifications given in the data sheet, of course, assume equal loading on all of the outputs. However situations could arise where this is an impossibility and it may be necessary to estimate the skew added by asymmetric loading. In addition the propagation delay numbers are provided only for 50 pF loads, thus necessitating a method of determining the propagation delay for alternative loads.

Figure 5 shows the relationship between the two propagation delays with respect to the capacitive load on the output. Utilizing this graph and the 50 pF limits the specification of the H641 can be mapped into a spec for either a different value load or asymmetric loads.

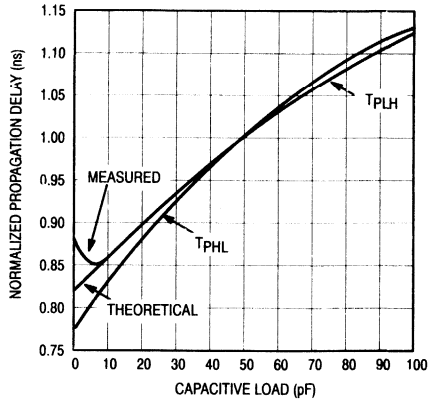


Figure 5. T_{PD} versus Load

Rise/Fall Skew Determination

The rise-to-fall skew is defined as simply the difference between the T_{PLH} and the T_{PHL} propagation delays. This skew for the H641 is dependent on the V_{CC} applied to the device. Notice from Figure 4 the opposite relationship of T_{PD} versus V_{CC} between T_{PLH} and T_{PHL}. Because of this the rise-to-fall skew will vary depending on V_{CC}. Since in all likelihood it will be impossible to establish the exact value for V_{CC}, the expected variation range for V_{CC} should be used. If this variation will be the ±5% shown in the data sheet the rise-to-fall skew could be established by simply subtracting the fastest T_{PLH} from the slowest T_{PHL}; this exercise yields 1.41 ns. If a tighter V_{CC} range can be realized Figure 4 can be used to establish the rise-to-fall skew.

Specification Limit Determination Example

The situation pictured in Figure 6 will be analyzed as an example. The central clock is distributed to two different cards; on one card a single H641 is used to distribute the clock while on the second card two H641's are required to supply the needed clocks. The data sheet as well as the graphical information of this section will be used to calculate the skew between H641a and H641b as well as the skew between all three of the devices. Only the T_{PLH} will be analyzed, the T_{PHL} numbers can be found using the same technique. The following assumptions will be used:

- All outputs will be loaded with 50 pF
- All outputs will toggle at 30 MHz
- The V_{CC} variation between the two boards is ±3%
- The temperature variation between the three devices is ±15°C around an ambient of 45°C.
- 500LFPM air flow

The first task is to calculate the junction temperature for the devices under these conditions. Using the power equation yields:

$$P_D = I_{CC}\text{ (no load)} * V_{CC} + V_{CC} * V_S * f * C_L * \#\text{ outputs}$$
$$= 1.8 * 48\text{ mA} * 5\text{ V} + 5\text{ V} * 3\text{ V} * 30\text{ MHz} * 50\text{ pF} * 9$$
$$= 432\text{ mW} + 203\text{ mW} = 635\text{ mW}$$

Using the thermal resistance graph of Figure 2 yields a thermal resistance of 41°C/W which yields a junction temperature of 71°C with a range of 56°C to 86°C. Using the T_{PD} versus Temperature curve of Figure 3 yields a propagation delay of 5.42 ns and a variation of 0.19 ns.

Since the design will not experience the full ±5% V_{CC} variation of the data sheet the 1ns window provided will be unnecessarily conservative. Using the curve of Figure 4 shows a delay variation due to a ±3% V_{CC} variation of ±0.075 ns. Therefore the 1ns window can be reduced to 1ns – (0.27 ns – 0.15 ns) = 0.88 ns. Since H641a and H641b are on the same board we will assume that they will always be at the same V_{CC}; therefore the propagation delay window will only be 1ns – 0.27 ns = 0.73 ns.

Putting all of this information together leads to a skew between all devices of

0.19 ns + 0.88 ns
(temperature + supply, and inherent device),

while the skew between devices A and B will be only

0.19 ns + 0.73 ns
(temperature + inherent device only).

In both cases, the propagation delays will be centered around 5.42ns, resulting in the following t_{PLH} windows:

T_{PLH} = 4.92 ns - 5.99 ns; 1.07 ns window (all devices)
T_{PLH} = 5.00 ns - 5.92 ns; 0.92 ns window (devices a & b)

Of course the output-to-output skew will be as shown in the data sheet since all outputs are equally loaded.

This process may seem cumbersome, however the delay windows, and thus skew, obtained are significantly better than the conservative worst case limits provided at the beginning of this note. For very high performance designs, this extra information and effort can mean the difference between going ahead with prototypes or spending valuable engineering time searching for alternative approaches.

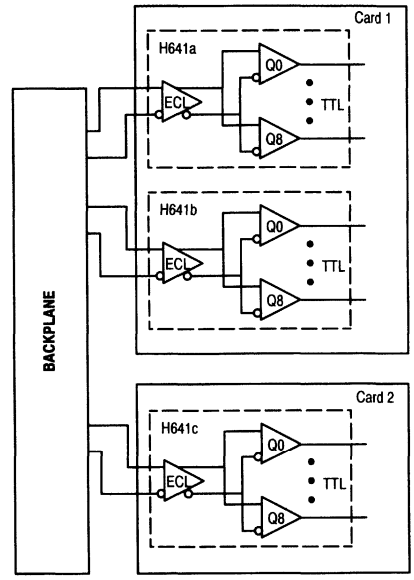


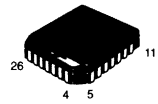
Figure 6. Example Application

MOTOROLA

MC10H642
MC100H642

Advance Information

68030/040
PECL/TTL Clock Driver



FN SUFFIX
PLASTIC PACKAGE
CASE 776

2

The MC10H/100H642 generates the necessary clocks for the 68030, 68040 and similar microprocessors. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part-to-part skew, within-part skew and also duty cycle skew.

The user has a choice of using either TTL or PECL (referenced to +5.0 V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50 MHz and beyond, the inherent superiority of PECL (particularly differential PECL) as a means of clock signal distribution becomes increasingly evident. The H642 also uses differential PECL internally to achieve its superior skew characteristic.

The H642 includes divide-by-two and divide-by-four stages, both to achieve the necessary duty cycle skew and to generate MPU clocks as required. A typical 50 MHz processor application would use an input clock running at 100 MHz, thus obtaining output clocks at 50 MHz and 25 MHz (see Logic Diagram).

The 10H version is compatible with MECL 10H ECL logic levels, while the 100H version is compatible with 100K levels (referenced to +5.0 V).

Function:

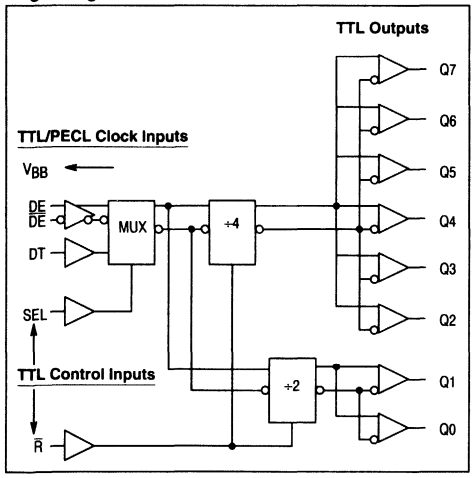
Reset(R): LOW on RESET forces all Q outputs LOW.
Select(SEL): LOW selects the ECL input source (DE/$\overline{DE}$). HIGH selects the TTL input source (DT).

The H642 also contains circuitry to force a stable input state of the PECL differential input pair, should both sides be left open. In this case, the D side of the input is pulled LOW, and $\overline{D}$ goes HIGH.

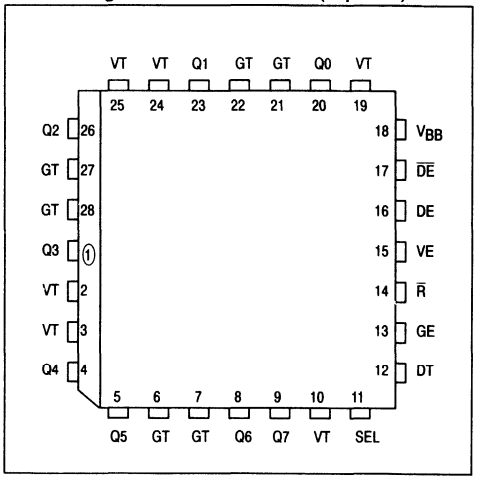
Power Up: The device is designed to have positive edges of the ÷2 and ÷4 outputs synchronized at Power Up.

- Generates Clocks for 68030/040
- Meets 030/040 Skew Requirements
- TTL or PECL Input Clock
- Extra TTL and ECL Power/Ground Pins
- Asynchronous Reset
- Single +5.0 V Supply
- Choice of PECL Compatibility: MECL 10H (10Hxxx) or 100K (100Hxxx)

Logic Diagram



Pinout Assignment — 28 Lead PLCC (Top View)



This document contains information on a new product. Specifications and information herein are subject to change without notice.

Pin	Symbol	Description	Pin	Symbol	Description
1	Q3	Signal Output (TTL)**	15	VE	PECL V_{CC} (+5.0 V)
2	VT	TTL V_{CC} (+5.0 V)	16	DE	PECL Signal Input (Non-Inverting)
3	VT	TTL V_{CC} (+5.0 V)	17	$\overline{DE}$	PECL Signal Input (Inverting)
4	Q4	Signal Output (TTL)**	18	V_{BB}	V_{BB} Reference Output
5	Q5	Signal Output (TTL)**	19	VT	TTL V_{CC} (+5.0 V)
6	GT	TTL Ground (0 V)	20	Q0	Signal Output (TTL)*
7	GT	TTL Ground (0 V)	21	GT	TTL Ground (0 V)
8	Q6	Signal Output (TTL)**	22	GT	TTL Ground (0 V)
9	Q7	Signal Output (TTL)**	23	Q1	Signal Output (TTL)*
10	VT	TTL V_{CC} (+5.0 V)	24	VT	TTL V_{CC} (+5.0 V)
11	SEL	Input Select (TTL)	25	VT	TTL V_{CC} (+5.0 V)
12	DT	TTL Signal Input	26	Q2	Signal Output (TTL)**
13	GE	PECL Ground (0 V)	27	GT	TTL Ground (0 V)
14	$\overline{R}$	Reset (TTL)	28	GT	TTL Ground (0 V)

*Divide by 2
**Divide by 4

AC CHARACTERISTICS: VT = VE = 5.0 V ±5%

Test Symbol	Characteristic		T_A = 0°C Min	T_A = 0°C Max	T_A = 25°C Min	T_A = 25°C Max	T_A = 85°C Min	T_A = 85°C Max	Unit	Condition
t_{PLH}	Propagation Delay D to Output	Q2–Q7 DE/$\overline{DE}$ DT	 5.0 5.2	 6.0 6.2	 5.0 5.1	 6.0 6.1	 5.4 5.5	 6.4 6.5	ns	C_L = 25 pF
tskpp	Part-to-Part Skew			1.0		1.0		1.0	ns	
tskwd*	Within-Device Skew			0.5		0.5		0.5	ns	
t_{PLH}	Propagation Delay D to Output	Q0, Q1 DE/$\overline{DE}$ DT	 5.0 5.1	 6.0 6.1	 5.0 5.1	 6.0 6.1	 5.4 5.5	 6.4 6.5	ns	C_L = 25 pF
tskpp	Part-to-Part Skew	All Outputs		1.0		1.0		1.0	ns	C_L = 25 pF
tskwd	Within-Device Skew			0.65		0.65		0.65	ns	C_L = 25 pF
t_{PD}	Propagation Delay R to Output	All Outputs	4.3	6.3	4.3	6.3	5.0	7.0	ns	C_L = 25 pF
t_R t_F	Output Rise/Fall Time 0.8 V to 2.0 V	All Outputs	0.5	2.5 2.5	0.5	2.5 2.5	0.5	2.5 2.5	ns	C_L = 25 pF
f_{MAX}**	Maximum Input Frequency		135		135		135		MHz	C_L = 25 pF
RPW	Reset Pulse Width		1.5		1.5		1.5		ns	
RRT	Reset Recovery Time		1.25		1.25		1.25		ns	

* Within-Device Skew defined as identical transactions on similar paths through a device.
** NOTE: MAX Frequency is 135 MHz.

10H PECL CHARACTERISTICS: VT = VE = 5.0 V ±5%

Test Symbol	Characteristic	T_A = 0°C Min	T_A = 0°C Max	T_A = 25°C Min	T_A = 25°C Max	T_A = 85°C Min	T_A = 85°C Max	Unit	Condition
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	μA	
	* NOTE								
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V	V_{EE} = 5.0 V
	* NOTE								
V_{BB}	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	

*NOTE: PECL LEVELS are referenced to V_{CC} and will vary 1:1 with the power supply. The VALUES shown are for V_{CC} = 5.0 V.

100H PECL CHARACTERISTICS: VT = VE = 5.0 V ±5%

Test Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	0.5	225	0.5	175	0.5	175	µA	
	* NOTE								
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	3.835 3.190	4.120 3.525	3.835 3.190	4.120 3.525	3.835 3.190	4.120 3.525	V	V_{EE} = 5.0 V
	* NOTE								
V_{BB}	Output Reference Voltage	3.620	3.740	3.620	3.740	3.620	3.740	V	

*NOTE: PECL LEVELS are referenced to V_{CC} and will vary 1:1 with the power supply. The VALUES shown are for V_{CC} = 5.0 V.

10H/100H DC CHARACTERISTICS: VT = VE = 5.0 V ±5%

Test Symbol	Characteristic		T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
I_{EE}	Power Supply Current	PECL		57		57		57	mA	VE Pin
I_{CCH}		TTL		30		30		30	mA	Total All VT Pins
I_{CCL}				30		30		30	mA	

10H/100H TTL DC CHARACTERISTICS: VT = VE = 5.0 V ±5%

Test Symbol	Characteristic	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	0.8	2.0	0.8	2.0	0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		−0.6		−0.6		−0.6	mA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = −3.0 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24 mA
V_{IK}	Input Clamp Voltage		−1.2		−1.2		−1.2	V	I_{IN} = −18 mA
I_{OS}	Output Short Circuit Current	−100	−225	−100	−225	−100	−225	mA	V_{OUT} = 0 V

Duty Cycle Control

To maintain a duty cycle of ±5% at 50 MHz, limit the load capacitance and/or power supply variation as shown in Figures 1 and 2. For a ±2.5% duty cycle limit, see Figures 3 and 4. Figures 5 and 6 show duty cycle variation with temperature. Figure 7 shows typical TPD versus load. Figure 8 shows reset recovery time. Figure 9 shows output states after power up.

Best duty cycle control is obtained with a single μP load and minimum line length.

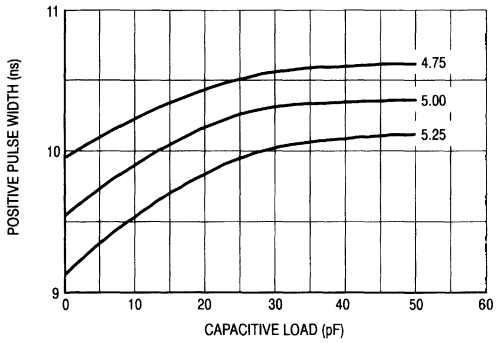


Figure 1. MC10H642 Positive PW versus Load @ ±5% V_{CC}, T_A = 25°C

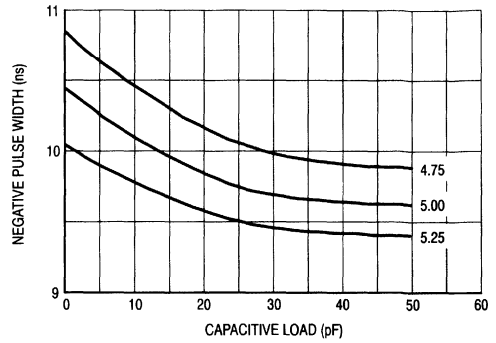


Figure 2. MC10H642 Negative PW versus Load @ ±5% V_{CC}, T_A = 25°C

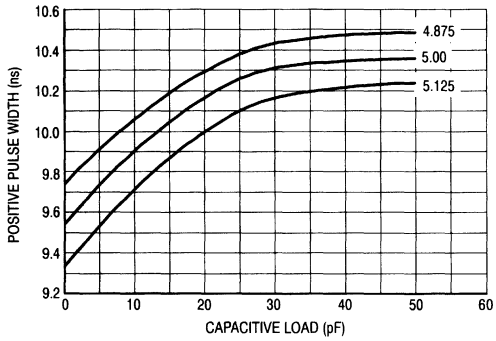


Figure 3. MC10H642 Positive PW versus Load @ ±2.5% V_{CC}, T_A = 25°C

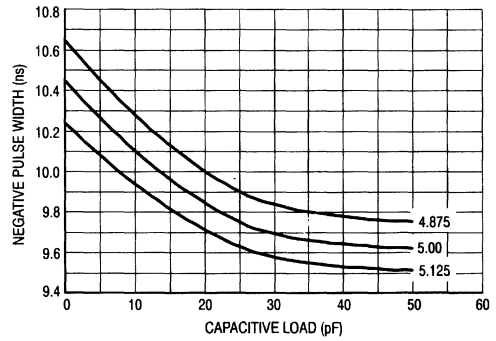


Figure 4. MC10H642 Negative PW versus Load @ ±2.5% V_{CC}, T_A = 25°C

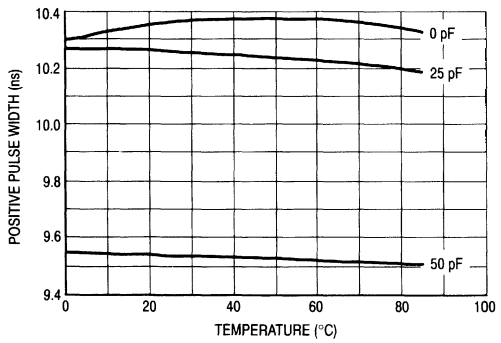


Figure 5. MC10H642 Positive PW versus Temperature, V_{CC} = 5.0 V

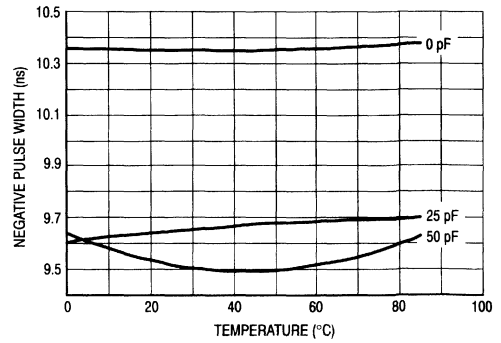


Figure 6. MC10H642 Negative PW versus Temperature, V_{CC} = 5.0 V

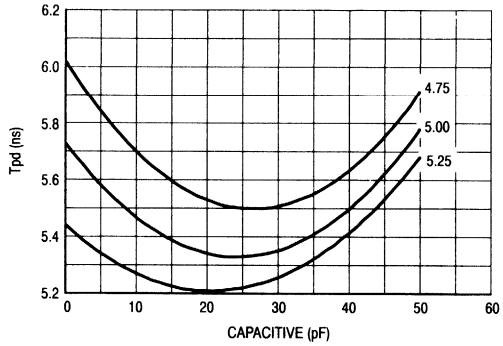


Figure 7. MC10H642 + Tpd versus Load, V_{CC} ±5%, T_A = 25°C (Overshoot at 50 MHz with no load makes graph non linear)

2

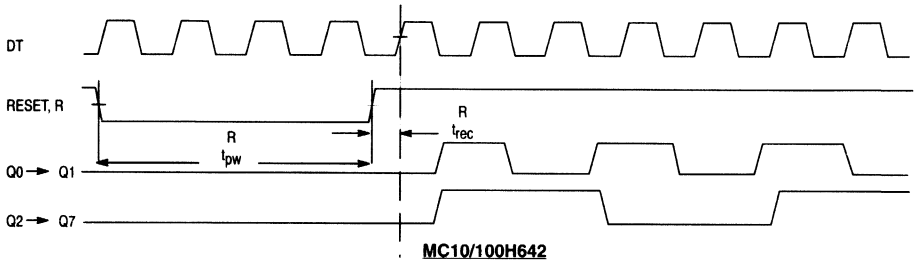


Figure 8. Clock Phase and Reset Recovery Time After Reset Pulse

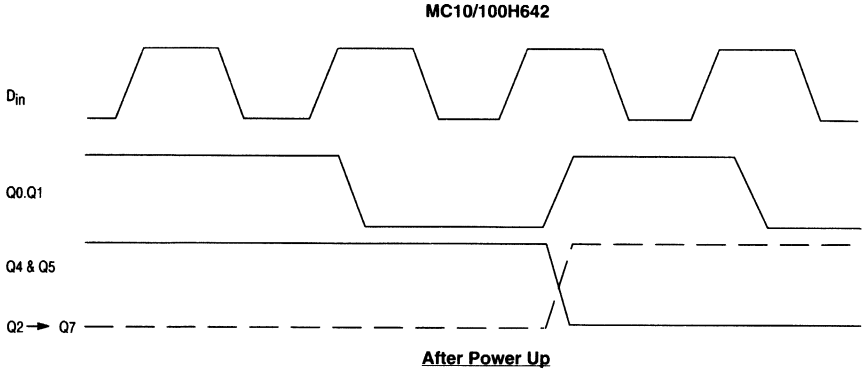
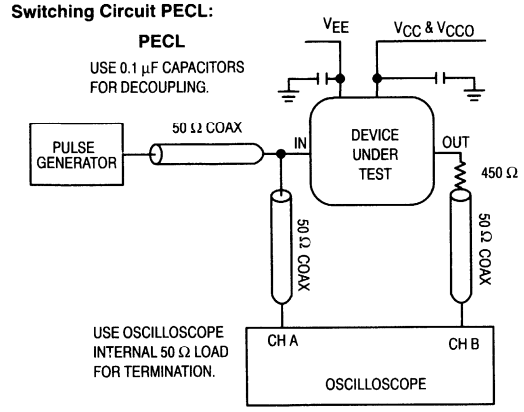


Figure 9. Outputs Q2 → Q7 will Synchronize with Pos Edges of D_{in} & Q0 → Q1

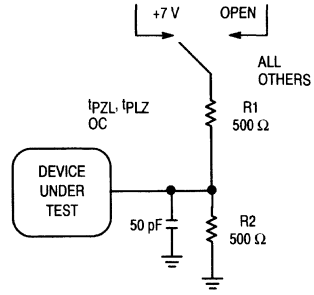
SWITCHING CIRCUIT AND WAVEFORMS

Switching Circuit PECL:

PECL

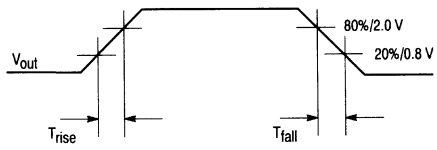


TTL



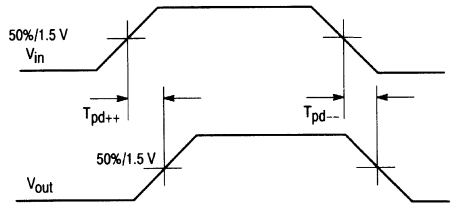
WAVEFORMS: Rise and Fall Times

PECL/TTL



Propagation Delay — Single Ended

PECL/TTL



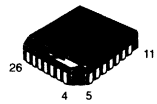
2

MOTOROLA

MC10H643
MC100H643

Dual Supply ECL/TTL 1:8 Clock Driver

DUAL SUPPLY ECL/TTL 1:8 CLOCK DRIVER



FN SUFFIX
PLASTIC PACKAGE
CASE 776

2

The MC10H/100H643 is a dual supply, low skew translating 1:8 clock driver. Devices in the Motorola H600 translator series utilize the 28-lead PLCC for optimal power pinning, signal flow through and electrical performance. The dual-supply H643 is similar to the H641, which is a single-supply 1:9 version of the same function.

The device features a 48 mA TTL output stage, with AC performance specified into a 50 pF load capacitance. A Latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pulldowns) the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW.

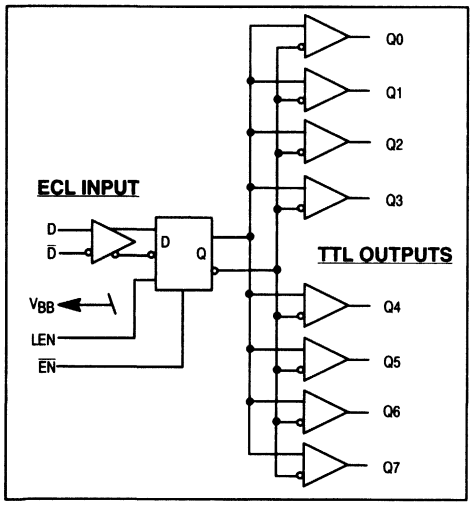
The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

- ECL – TTL version of popular ECLinPS E111
- Low Skew Within Device 0.5 ns
- Guaranteed Skew Spec Part-to-Part 1.0 ns
- Latch
- Differential Internal Design
- V_{BB} Output
- Dual Supply
- Reset/Enable
- Multiple TTL and ECL Power/Ground Pins
- Choice of ECL Compatibility:
  MECL 10H (10Hxxx) or 100K (100Hxxx)

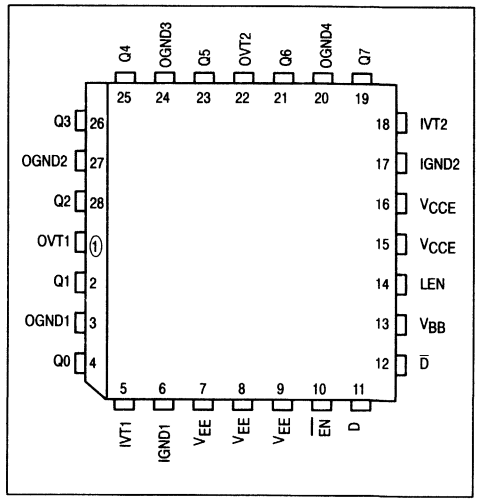
PIN NAMES

PIN	FUNCTION
OGND	TTL Output Ground (0 V)
OVT	TTL Output V_{CC} (+5.0 V)
IGND	Internal TTL GND (0 V)
IVT	Internal TTL V_{CC} (+5.0 V)
V_{EE}	ECL V_{EE} (–5.2/–4.5 V)
V_{CCE}	ECL Ground (0 V)
D, $\overline{D}$	Signal Input (ECL)
V_{BB}	V_{BB} Reference Output
Q0–Q7	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (ECL)
LEN	Latch Enable Input (ECL)

LOGIC SYMBOL



PINOUT: 28-LEAD PLCC (TOP VIEW)



DC CHARACTERISTICS: IVT = OVT = 5.0 V ±5%; V_{EE} = −5.2 V ±5% (10H Version); V_{EE} = −4.5 V ±0.3 V (100H Version)

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{EE}	Power Supply Current	ECL	—	42	—	42	—	42	mA	V_{EE} Pins
I_{CCL}		TTL	—	106	—	106	—	106	mA	Total all OVT and IVT pins
I_{CCH}			—	95	—	95	—	95	mA	

AC CHARACTERISTICS: IVT = OVT = 5.0 V ±5%; V_{EE} = −5.2 V ±10% (10H), −4.5 V ±0.3 V (100H); V_{CCE} = GND

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
t_{PLH}	Propagation Delay to Output								
	D	4.0	5.0	4.1	5.1	4.4	5.4	ns	C_L = 50 pF
	LEN	3.5	5.5	3.5	5.5	3.9	5.9		
	$\overline{EN}$	3.5	5.5	3.5	5.5	3.9	5.9		
t_{SKPP}	Part-to-Part Skew		1.0		1.0		1.0	ns	
t_{SKEW}	Within-Device Skew	—	0.5	—	0.5	—	0.5	ns	Note 1
t_w	Pulse Width Out HIGH or LOW @ f_{out} = 50 MHz	9.0	11.0	9.0	11.0	9.0	11.0	ns	C_L = 50 pF Note 2
t_s	Setup Time D	0.75	—	0.75	—	0.75	—	ns	
t_h	Hold Time D	0.75	—	0.75	—	0.75	—	ns	
t_{RR}	Recovery Time								
	LEN	1.25	—	1.25	—	1.25	—	ns	
	$\overline{EN}$	1.25	—	1.25	—	1.25	—		
t_{pw}	Minimum Pulse Width								
	LEN	1.5	—	1.5	—	1.5	—	ns	
	$\overline{EN}$	1.5	—	1.5	—	1.5	—		
t_r t_f	Rise / Fall Times 0.8 V – 2.0 V	0.5	1.2	0.5	1.2	0.5	1.2	ns	C_L = 50 pF

1. Within-Device skew defined as identical transitions on similar paths through a device.
2. Pulse width is defined relative to 1.5 V measurement points on the output waveform.

TRUTH TABLE

D	LEN	$\overline{EN}$	Q
L	L	L	L
H	L	L	H
X	H	L	Q_0
X	X	H	L

TTL CHARACTERISTICS: IVT = OVT = 5.0 V ±5%; V_{EE} = −5.2 V ±5% (10H Version); V_{EE} = −4.5 V ±0.3 V (100H Version)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = −3.0 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OH} = 48 mA
IOS	Output Short Circuit Current	−100	−225	−100	−225	−100	−225	mA	V_{OUT} = 0 V

10H ECL CHARACTERISTICS: IVT = OVT = 5.0 V ±5%; V_{EE} = −5.2 V ±5% (10H Version); V_{EE} = −4.5 V ±0.3 V (100H Version)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	−1170 −1950	−840 −1480	−1130 −1950	−810 −1480	−1060 −1950	−720 −1445	mV	
V_{BB}	Output Reference Voltage	−1380	−1270	−1350	−1250	−1310	−1190	mV	

100H ECL CHARACTERISTICS: IVT = OVT = 5.0 V ±5%; V_{EE} = −5.2 V ±5% (10H Version); V_{EE} = −4.5 V ±0.3 V (100H Version)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	−1165 −1810	−880 −1475	−1165 −1810	−880 −1475	−1165 −1810	−880 −1475	mV	
V_{BB}	Output Reference Voltage	−1380	−1260	−1380	−1260	−1380	−1260	mV	

MOTOROLA

MC10H644
MC100H644

68030/040 PECL/TTL Clock Driver

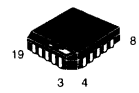
68030/040
PECL/TTL
CLOCK DRIVER

The MC10H/100H644 generates the necessary clocks for the 68030, 68040 and similar microprocessors. The device is functionally equivalent to the H640, but with fewer outputs in a smaller outline 20-lead PLCC package. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part-to-part skew, within-part skew and also duty cycle skew.

The user has a choice of using either TTL or PECL (PECL referenced to +5.0 V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50 MHz and beyond, the inherent superiority of PECL (particularly differential PECL) as a means of clock signal distribution becomes increasingly evident. The H644 also uses differential PECL internally to achieve its superior skew characteristic.

The H644 includes divide-by-two and divide-by-four stages, both to achieve the necessary duty cycle and skew to generate MPU clocks as required. A typical 50 MHz processor application would use an input clock running at 100 MHz, thus obtaining output clocks at 50 MHz and 25 MHz (see Logic Symbol).

The 10H version is compatible with MECL 10H ECL logic levels, while the 100H version is compatible with 100K levels (referenced to +5.0 V).



FN SUFFIX
PLASTIC PACKAGE
CASE 775

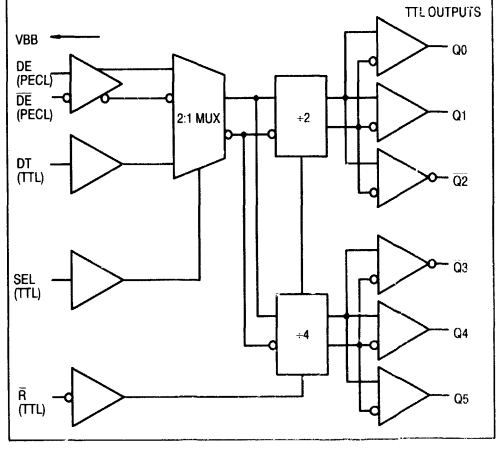
Function

Reset (R): LOW on RESET forces all Q outputs LOW and all $\overline{Q}$ outputs HIGH.
Synchronized Outputs: The device is designed to have the POS edges of the ÷2 and ÷4 outputs synchronized.
Select (SEL): LOW selects the PECL input source (DE/$\overline{DE}$). HIGH selects the TTL input source (DT).

The H644 also contains circuitry to force a stable state of the PECL input differential pair, should both sides be left open. In this case, the DE side of the input is pulled LOW, and $\overline{DE}$ goes HIGH.

- Generates Clocks for 68030/040
- Meets 68030/040 Skew Requirements
- TTL or PECL Input Clock
- Extra TTL and PECL Power/Ground Pins
- Within Device Skew on Similar Paths is 0.5 ns
- Asynchronous Reset
- Single +5.0 V Supply
- Choice of PECL Compatibility: MECL 10H (10Hxxx) or 100K (100Hxxx)

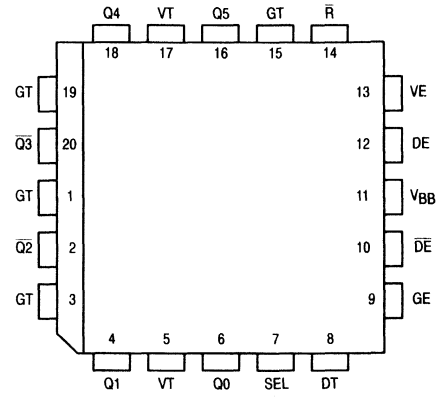
LOGIC SYMBOL



PIN NAMES

PIN	FUNCTION
GT	TTL Ground (0 V)
VT	TTL V_{CC} (+5.0 V)
VE	PECL V_{CC} (+5.0 V)
GE	PECL Ground (0 V)
DE, $\overline{DE}$	PECL Signal Input (positive ECL)
V_{BB}	V_{BB} Reference Output
DT	TTL Signal Input
Qn, $\overline{Qn}$	Signal Outputs (TTL)
SEL	Input Select (TTL)
$\overline{R}$	Reset (TTL)

PINOUT: 20–LEAD PLCC (TOP VIEW)



AC CHARACTERISTICS: VT = VE = 5.0 V ±5%

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
t_{PLH}	Propagation Delay PECL D to Output	All Outputs	5.8	6.8	5.7	6.7	6.1	7.1	ns	C_L = 50 pF
t_{PLH}	Propagation Delay TTL D to Output		5.7	6.7	5.7	6.7	6.0	7.0	ns	C_L = 50 pF
t_{PLH}/ t_{PHL}	Propagation Delay PECL/TTL D to Output		4.2	7.2	4.26	7.26	4.73	7.73	ns	C_L = 50 pF
t_{skwd}*	Within-Device Skew	Q0, 1, 4, 5	—	0.5	—	0.5	—	0.5	ns	C_L = 50 pF
t_{skwd}*	Within-Device Skew	$\overline{Q2}$, $\overline{Q3}$	—	0.5	—	0.5	—	0.5	ns	C_L = 50 pF
t_{skwd}*	Within-Device Skew	All Outputs	—	1.5	—	1.5	—	1.5	ns	C_L = 50 pF
$t_{skp\text{-}p}$*	Part-to-Part Skew	Q0, 1, 4, 5	—	1.0	—	1.0	—	1.0	ns	C_L = 50 pF
t_{PD}	Propagation Delay R to Output	All Outputs	4.3	7.3	4.3	7.3	4.5	7.5	ns	C_L = 50 pF
t_R t_F	Output Rise/Fall Time 0.8 V–2.0 V	All Outputs	0.5	1.6	0.5	1.6	0.5	1.6	ns	C_L = 50 pF
f_{max}	Maximum Input Frequency		135	—	135	—	135	—	MHz	C_L = 50 pF
TW	Minimum Pulse Width Reset		1.5	—	1.5	—	1.5	—	ns	
t_{rr}	Reset Recovery Time		1.25	—	1.25	—	1.25	—	ns	
T_{PW}	Pulse Width Out High or Low @ f_{in} = 100 MHz and C_L = 50 pF	Q0, 1	9.5	10.5	9.5	10.5	9.5	10.5	ns	C_L = 50 pF Relative 1.5 V
TS	Setup Time SEL to DE, DT		2.0	—	2.0	—	2.0	—	ns	
TH	Hold Time SEL to DE, DT		2.0	—	2.0	—	2.0	—	ns	

* Skews are specified for Identical Edges

DC CHARACTERISTICS: VT = VE = 5.0 V ±5%

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{EE}	Power Supply Current	ECL		65		65		65	mA	VE Pin
I_{CC}		TTL		85		85		85	mA	Total all V_T pins

TTL DC CHARACTERISTICS: VT = VE = 5.0 V ±5%

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	µA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		−0.6		−0.6		−0.6	mA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = −3.0 mA I_{OH} = −24 mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24 mA
V_{IK}	Input Clamp Voltage		−1.2		−1.2		−1.2	V	I_{IN} = −18 mA
I_{OS}	Output Short Circuit Current	−100	−225	−100	−225	−100	−225	mA	V_{OUT} = 0 V

10H PECL DC CHARACTERISTICS: VT = VE = 5.0 V ±5%

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	µA	
V_{IH}* V_{IL}*	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.55	V	VE = 5.0 V
V_{BB}*	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	VE = 5.0 V

100H PECL DC CHARACTERISTICS: VT = VE = 5.0 V ±5%

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	µA	
V_{IH}* V_{IL}*	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	VE = 5.0 V
V_{BB}*	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	VE = 5.0 V

* NOTE: ECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for V_{CC} = 5.0 V.

MOTOROLA

MC10H645

Advance Information

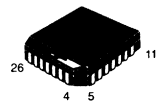
1:9 TTL Clock Driver

1:9 TTL CLOCK DRIVER

The MC10H645 is a single supply, low skew, TTL I/O 1:9 Clock Driver. Devices in the Motorola H600 clock driver family utilize the 28-lead PLCC for optimal power and signal pin placement.

The device features a 24 mA TTL output stage with AC performance specified into a 50 pF load capacitance. A 2:1 input mux is provided on chip to allow for distributing both system and diagnostic clock signals or designing clock redundancy into a system. With the SEL input held LOW the DO input will be selected, while the D1 input is selected when the SEL input is forced HIGH.

- Low Skew Typically 0.65 ns Within Device
- Guaranteed Skew Spec 1.25 ns Part-to-Part
- Input Clock Muxing
- Differential ECL Internal Design
- Single Supply
- Extra TTL and ECL Power/Ground Pins



FN SUFFIX
PLASTIC PACKAGE
CASE 776

2

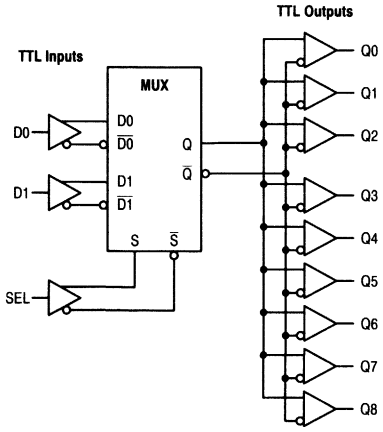
PIN NAMES

PIN	FUNCTION
GT	TTL Ground (0 V)
VT	TTL V_{CC} (+5.0 V)
VE	ECL V_{CC} (+5.0 V)
GE	ECL Ground (0 V)
Dn	TTL Signal Input
Q0 - Q8	TTL Signal Outputs
SEL	TTL Mux Select

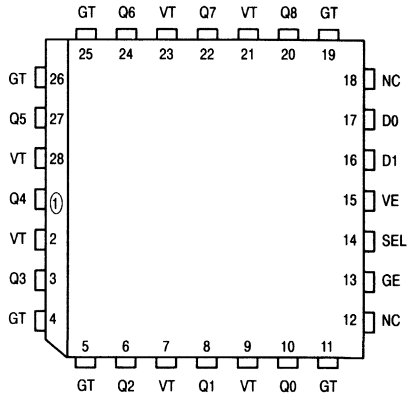
TRUTH TABLE

D0	D1	SEL	Q
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

LOGIC SYMBOL



PINOUT: 28-LEAD PLCC (TOP VIEW)



This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN DESCRIPTIONS

Pin	Symbol	Description	Pin	Symbol	Description
1	Q4	Signal Output (TTL)	15	VE	ECL V_{CC} (+5.0 V)
2	VT	TTL V_{CC} (+5.0 V)	16	D1	Signal Input (TTL)
3	Q3	Signal Output (TTL)	17	D0	Signal Input (TTL)
4	GT	TTL Ground (0 V)	18	NC	No Connection
5	GT	TTL Ground (0 V)	19	GT	TTL Ground (0 V)
6	Q2	Signal Output (TTL)	20	Q8	Signal Output (TTL)
7	VT	TTL V_{CC} (+5.0 V)	21	VT	TTL V_{CC} (+5.0 V)
8	Q1	Signal Output (TTL)	22	Q7	Signal Output (TTL)
9	VT	TTL V_{CC} (+5.0 V)	23	VT	TTL V_{CC} (+5.0 V)
10	Q0	Signal Output (TTL)	24	Q6	Signal Output (TTL)
11	GT	TTL Ground (0 V)	25	GT	TTL Ground (0 V)
12	NC	No Connection	26	GT	TTL Ground (0 V)
13	GE	ECL Ground	27	Q5	Signal Output (TTL)
14	SEL	Select Input (TTL)	28	VT	TTL V_{CC} (+5.0 V)

2

ABSOLUTE RATINGS (Do not exceed)

Rating	Symbol	Value	Unit
Power Supply Voltage	VE (ECL)	−0.5 to +7.0	V
Power Supply Voltage	VT (TTL)	−0.5 to +7.0	V
Input Voltage	VI (TTL)	−0.5 to +7.0	V
Disabled 3-State Output	V_{out}	0.0 to V_T	V
Storage Temperature	T_{stg}	−65 to 150	°C
Operating Temperature	T_{amb}	0.0 to +85	°C

DC CHARACTERISTICS VT = VE = 5.0 V ±5%

			0°C		25°C		85°C			
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	Unit	Condition
I_{EE}	Power Supply Current	ECL		30		30		30	mA	VE Pin
I_{CCH}		TTL		30		30		30	mA	Total all VT pins
I_{CCL}				35		35		35	mA	
V_{OH}	Output HIGH Voltage		2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = −3.0 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.5		0.5		0.5	V	I_{OL} = 24 mA
I_{OS}	Output Short Circuit Current		−100	−225	−100	−225	−100	−225	mA	V_{OUT} = 0 V

AC CHARACTERISTICS VT = VE = 5.0 V ±5%

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
t_{PLH}	Propagation Delay D_0 to Output Only	Q0 – Q8	5.2	6.2	5.2	6.2	5.6	6.6	ns	C_L = 50 pF
t_{skpp}	Part-to-Part Skew D_0 to Output Only			1.0		1.0		1.0	ns	
t_{skwd}*	Within-Device Skew D_0 to Output Only			0.65		0.65		0.65	ns	
t_{PLH}	Propagation Delay SEL to Q	Q0 – Q8	5.2	7.3	5.2	7.2	5.7	7.7	ns	C_L = 50 pF
t_r t_f	Output Rise/Fall Time 0.8 V to 2.0 V	Q0 – Q8	0.5 0.5	1.7 1.6	0.5 0.5	1.7 1.6	0.5 0.5	1.7 1.6	ns	C_L = 50 pF
t_S	Setup Time SEL to D		1.0		1.0		1.0		ns	

* Within-Device Skew defined as identical transitions on similar paths through a device.

DUTY CYCLE SPECIFICATIONS 0°C ≤ TA ≤ 85°C; Duty Cycle Measured Relative to 1.5 V

Symbol	Characteristic		Min	Nom	Max	Unit	Condition
PW	Range of V_{CC} and C_L to Meet Min Pulse Width (HIGH or LOW) at f_{out} ≤ 50 MHz	V_{CC} C_L PW	4.875 10.0 9.0	5.0	5.125 50.0 11.0	V pF ns	All Outputs

MOTOROLA

MC10H646
MC100H646

Product Preview

PECL/TTL-TTL 1:8 Clock Distribution Chip

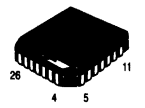
PECL/TTL-TTL
1:8 CLOCK
DISTRIBUTION CHIP

The MC10H/100H646 is a single supply, low skew translating 1:8 clock driver. Devices in the Motorola 'H600 translator series utilize the 28-lead PLCC for optimal power pinning, signal flow through and electrical performance. The single supply H646 is similar to the H643, which is a dual supply 1:8 version of the same function.

The device features a 24 mA TTL output stage, with AC performance specified into a 50 pF load capacitance.

The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

- PECL/TTL-TTL Version of Popular ECLinPS E111
- Low Skew
- Guaranteed Skew Spec
- Tri-State Enable
- Differential Internal Design
- V_{BB} Output
- Single Supply
- Extra TTL and ECL Power/Ground Pins
- Choice of ECL Compatibility: MECL 10H (10Hxxx) or 100K (100Hxxx)
- Matched High and Low Output Impedance

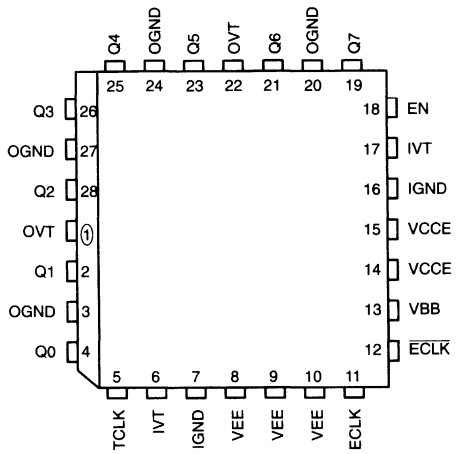


FN SUFFIX
PLASTIC PACKAGE
CASE 776

PIN NAMES

PIN	FUNCTION
OGND	TTL Output Ground (0 V)
OVT	TTL Output V_{CC} (+5.0 V)
IGND	Internal TTL GND (0 V)
IVT	Internal TTL V_{CC} (+5.0 V)
V_{EE}	ECL V_{EE} (0 V)
V_{CCE}	ECL Ground (5.0 V)
ECLK, $\overline{ECLK}$	Differential Signal Input (PECL)
V_{BB}	V_{BB} Reference Output
Q0–Q7	Signal Outputs (TTL)
EN	Tri-State Enable Input (TTL)
LEN	Signal Input (TTL)

Pinout: 28-Lead PLCC (Top View)



DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0 V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.6	– –	2.6	– –	2.6	– –	V	I_{OH} = 24 mA
V_{OL}	Output LOW Voltage	–	0.5	–	0.5	–	0.5	V	I_{OI} = 24 mA
IOS	Output Short Circuit Current	–	–	–	–	–	–	mA	See Note 1

1 The outputs must not be shorted to ground, as this will result in permanent damage to the device. The high drive outputs of this device do not include a limiting IOS resistor.

10H PECL DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0 V ±5%)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			225			175			175	µA	
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA	
V_{IH}	Input HIGH Voltage	3.83		4.16	3.87		4.19	3.94		4.28	V	IVT = IVO = VCCE = 5.0V (1)
V_{IL}	Input LOW Voltage	3.05		3.52	3.05		3.52	3.05		3.555	V	IVT = IVO = VCCE = 5.0V (1)
V_{BB}	Output Reference Voltage	3.62		3.73	3.65		3.75	3.69		3.81	V	IVT = IVO = VCCE = 5.0V (1)

100H PECL DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0 V ±5%)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			225			175			175	µA	
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA	
V_{IH}	Input HIGH Voltage	3.835		4.12	3.835		4.12	3.835		3.835	V	IVT = IVO = VCCE = 5.0V (1)
V_{IL}	Input LOW Voltage	3.19		3.525	3.19		3.525	3.19		3.525	V	IVT = IVO = VCCE = 5.0V (1)
V_{BB}	Output Reference Voltage	3.62		3.74	3.62		3.74	3.62		3.74	V	IVT = IVO = VCCE = 5.0V (1)

1 PECL V_{IH}, V_{IL} and V_{BB} are referenced to VCCE and will vary 1:1 with the power supply. The levels shown are for IVT = IVO = VCCE = 5.0 V

DC CHARACTERISTICS (IVT = OVT = VCCE = 5.0 V ±5%)

Symbol	Characteristic	0°C		25°C			85°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
I_{CCL}	Power Supply Current	–		–	166		–		mA	Total all OVT, IVT,
I_{CCH}		–		–	154		–		mA	and VCCE pins

AC CHARACTERISTICS (IVT = OVT = VCCE = 5.0 V ±5%)

Symbol	Characteristic		0°C		25°C			85°C		Unit	Condition
			Min	Max	Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	Q0-Q7				6.5				ns	C_L = 50 pF
t_{skpp}	Part-to-Part Skew			1.0			1.0		1.0	ns	
t_{skwd}	Within-Device Skew		–	0.5		–	0.5		0.5	ns	
t_w	Pulse Width Out HIGH or LOW @ f_{OUT} = 50 MHz	Q0-Q7	9.0		9.0			9.0		ns	C_L = 50 pF

2

AC CHARACTERISTICS (continued) (IVT = OVT = VCCE = 5.0 V ±5%)

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit	Condition
t_R t_F	Output Rise/Fall Time 0.8 V to 2.4 V 0.8 V to 2.0 V	All Outputs		1.6 1.2	0.7 0.3		1.6 1.2		1.6 1.2	ns	C_L = 50 pF

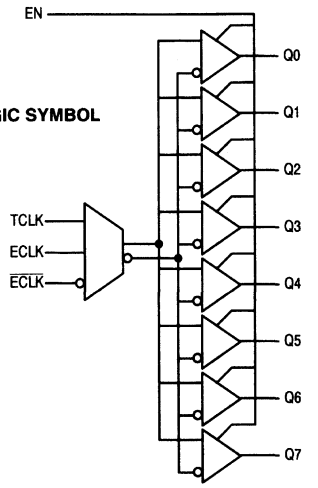
Note to Product Preview Edition: The pre-silicon simulation value for typical propagation delay to all outputs is 6.5ns. Final value will be established as the measured statistical mean after characterization of a sufficient number of lots, and thus may not exactly equal the target. The skew specification is an absolute value that measures the worst case T_{pd} difference between any two of the specified outputs.

TRUTH TABLE

TCLK	ECLK	$\overline{ECLK}$	EN	Q
GND	L	H	H	L
GND	H	L	H	H
H	GND	GND	H	H
L	GND	GND	H	L
X	X	X	L	Z

X = Immaterial; L = Low Voltage Level; H = High Voltage Level; Z = Tristate

LOGIC SYMBOL



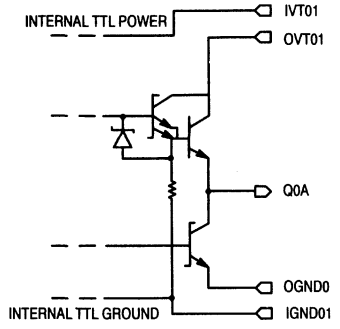


Figure 1. Output Structure

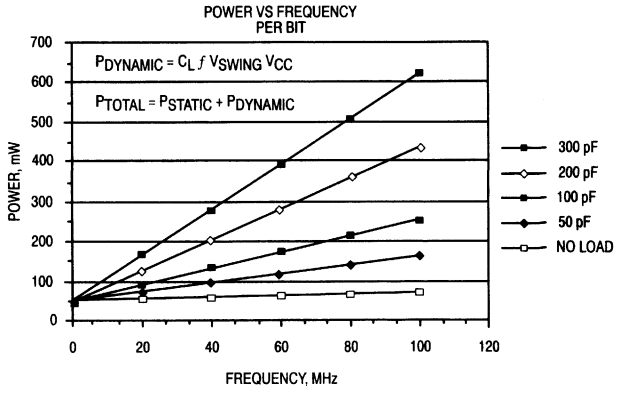


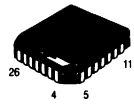
Figure 2. Power versus Frequency (Typical)

MOTOROLA

MC10H660
MC100H660

4-Bit ECL-TTL Load Reducing DRAM Driver

4-BIT ECL-TTL LOAD REDUCING DRAM DRIVER



FN SUFFIX
PLASTIC PACKAGE
CASE 776

2

The MC10H/100H660 is a 4-bit ECL input, translating DRAM address driver, ideally suited for driving TTL compatible DRAM inputs from an ECL system. It is designed for use in high capacity, highly interleaved DRAM memory boards, that directly interface to a high speed, pipelined ECL bus interface, where new operations may be initiated to the board at up to a 50 MHz rate.

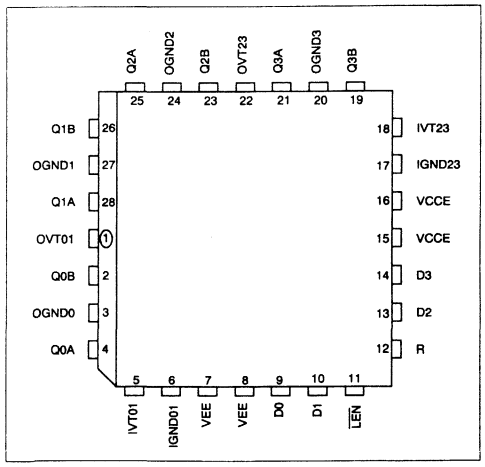
The latch provides the capability for the memory controller to propagate new addresses to different banks without having to wait for the address timing constraints to be satisfied from a previous memory operation. The dual output fanout reduces input loading from the controller by a factor of two, thus significantly improving board etch propagation delays from the controller, without the need for additional ECL buffering.

The H660 features special TTL outputs which do not have an IOS limiting resistor, therefore allowing rapid charging of the load capacitance. Output voltage levels are designed specifically for driving DRAM inputs. The output stages feature separate power and ground pins to isolate output switching noise from internal circuitry, and also to improve simultaneous switching performance.

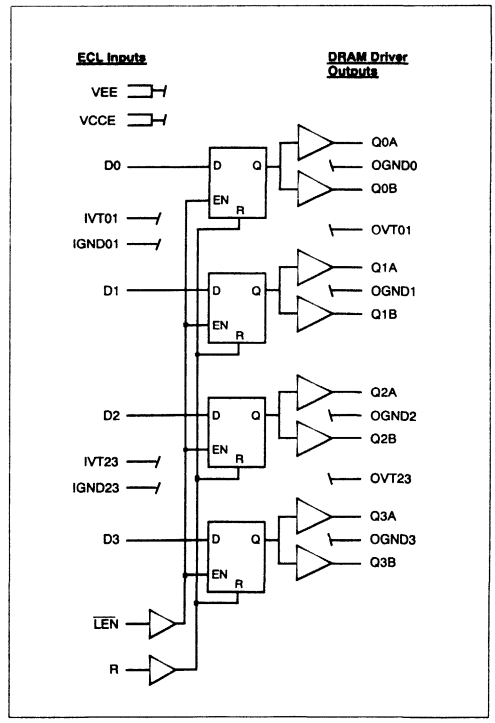
The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

- High Capacitive Drive Outputs to Drive DRAM Address Inputs
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- 10.7 ns Max. D to Q into 300 pF
- Choice of ECL Compatibility: MECL 10H (10Hxxx) or 100K (100Hxxx)

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

PIN	FUNCTION
OGND[0:3]	Output Ground (0V)
OVT01, OVT23	Output VCCT (+5.0 V)
IGND01, IGND23	Internal TTL Ground (0V)
IVT01, IVT23	Internal TTL VCCT (+5.0 V)
VEE	ECL Neg. Supply (–5.2 / –4.5 V)
VCCE	ECL Ground (0V)
D[0:3]	Data Inputs (ECL)
Q[0:3]A, Q[0:3]B	Data Outputs (TTL levels)
$\overline{LEN}$	Latch Enable (ECL)
R	Reset (ECL)

TRUTH TABLE

D	$\overline{LEN}$	R	Q
L	H	L	L
H	H	L	H
X	L	L	Q_0
X	X	H	L

2

DC Characteristics: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version)
V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Characteristic		0°C min	0°C max	25°C min	25°C max	85°C min	85°C max	Unit	Condition
I_{EE}	Power Supply Current	ECL		41.8		44.0		46.2	mA	
I_{CCH}		TTL		77.0		77.1		79.2	mA	
I_{CCL}				94.6		95.7		96.8	mA	

TTL DC Characteristics: V_{CCT} = 5.0 V ± 10%; V_{EE} = –5.2 V ± 5% (10H version)
V_{EE} = –4.2 V to –5.5 V (100H version)

Symbol	Characteristic	0°C min	0°C max	25°C min	25°C max	85°C min	85°C max	Unit	Condition
V_{OH}	Output HIGH Voltage	2.6		2.6		2.6		V	I_{OH} = –24 mA
V_{OL}	Output LOW Voltage		0.50		0.50		0.50	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current*		*		*		*	V	See Note 1

[1]The outputs must not be shorted to ground, as this will result in permanent damage to the device. The high drive outputs of this device do not include a limiting IOS resistor.

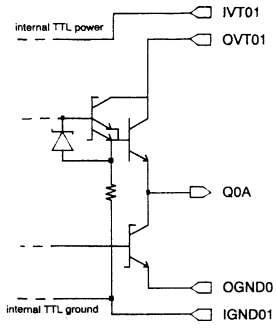
Minimum recommended load capacitance is 100 pF. Precise output performance and waveforms will depend on the exact nature of the actual load. The lumped load is of course an approximation to a real memory system load.

AC Characteristics: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5% (10H version)
V_{EE} = −4.2 V to −5.5 V (100H version)

Symbol	Characteristic		0°C min	0°C max	25°C min	25°C max	85°C min	85°C max	Unit	Condition
t_s	Set-up Time, D to $\overline{LEN}$		0.5		0.5		0.5		ns	
t_n	Hold Time, D to $\overline{LEN}$		1.5		1.5		1.5		ns	
t_w(H)	LEN Pulse Width, HIGH		2.0		2.0		2.0		ns	
t_R t_F	Output Rise/Fall Time 0.8 V – 2.0 V		0.5	2.0	0.5	2.0	0.5	2.0	ns	C_L = 200 pF
t_{PLH} t_{PHL}	Propagation Delay to Output	D	3.0 4.0 4.5	6.0 8.0 9.5	3.0 4.0 4.5	6.0 8.0 9.5	3.0 4.0 4.5	6.0 8.0 9.5	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF
	50% point of ECL input to 1.5 V point of TTL output	$\overline{LEN}$	4.3 4.9 5.4	6.9 8.9 10.4	4.3 4.9 5.4	6.9 8.9 10.4	4.3 4.9 5.4	6.9 8.9 10.4	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF
t_{PHL}	Propagation Delay to Output	R	4.1 4.5 5.0	9.1 8.5 10.0	4.1 4.5 5.0	9.1 8.5 10.0	4.1 4.5 5.0	9.1 8.5 10.0	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF
t_{PLH}	Propagation Delay to Output	D	3.9 4.8 5.8	5.9 7.2 8.8	3.9 4.8 5.8	5.9 7.2 8.8	4.0 5.0 5.9	6.1 7.4 8.9	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF
	50% point of ECL input to 2.4 V point of TTL output	$\overline{LEN}$	4.7 5.5 6.3	7.1 8.3 9.5	4.7 5.5 6.3	7.1 8.3 9.5	4.8 5.6 6.4	7.2 8.4 9.6	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF
t_{PHL}	Propagation Delay to Output	D	4.5 6.0 7.0	6.7 9.0 10.6	4.5 6.0 7.0	6.7 9.0 10.6	4.4 6.0 6.9	6.6 9.0 10.3	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF
	50% point of ECL input to 0.8 V point of TTL output	$\overline{LEN}$	4.0 4.9 6.0	6.0 7.3 9.0	4.0 4.9 6.0	6.0 7.3 9.0	4.0 4.9 5.9	6.0 7.3 8.9	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF
		R	4.3 6.1 7.2	6.5 9.1 10.8	4.3 6.1 7.2	6.5 9.1 10.8	4.3 6.1 7.2	6.5 9.1 10.8	ns	C_L = 100 pF C_L = 200 pF C_L = 300 pF

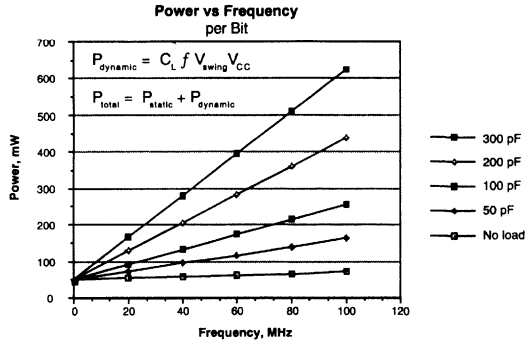
OUTPUT STRUCTURE

– Output Q0A Shown



POWER vs FREQUENCY

– typical



2

10H ECL DC Characteristics: V_{CCT} = 5.0 V ± 10%; V_{EE} = −5.2 V ± 5%

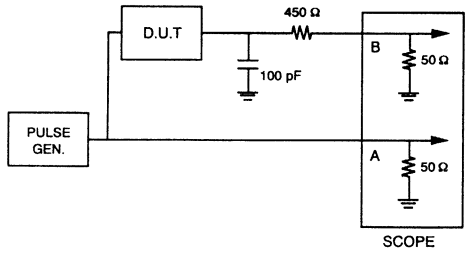
Symbol	Characteristic	0°C min	0°C max	25°C min	25°C max	85°C min	85°C max	Unit	Condition
I_{IH}	Input HIGH Current		225		145		145	µA	
I_{IL}	Input LOW Current	1.5		1.0		1.0		µA	
V_{IH}	Input HIGH Voltage	-1170	-840	-1130	-810	-1060	-720	mV	
V_{IL}	Input LOW Voltage	-1950	-1480	-1950	-1480	-1950	-1445	mV	

100H ECL DC Characteristics: V_{CCT} = 5.0 V ± 10%; V_{EE} = −4.2 V to −5.5 V

Symbol	Characteristic	0°C min	0°C max	25°C min	25°C max	85°C min	85°C max	Unit	Condition
I_{IH}	Input HIGH Current		225		145		145	µA	
I_{IL}	Input LOW Current	1.5		1.0		1.0		µA	
V_{IH}	Input HIGH Voltage	-1165	-880	-1165	-880	-1165	-880	mV	
V_{IL}	Input LOW Voltage	-1810	-1475	-1810	-1475	-1810	-1475	mV	

AC TEST SET-UP

C_L = 100 pF



The MC10/100 H660 ECL-TTL DRAM Address Driver

The MC 10/100H660 was designed for use in high capacity, highly interleaved DRAM memory boards, that directly interface to a high speed, pipelined ECL bus interface, where new operations may be initiated to the board at a 50 MHz rate (e.g. bipolar RISC systems).

The following briefly discusses the major design features of the part over existing semiconductor devices traditionally used in interfacing DRAMs in high performance system environments.

1. ECL Translator

High performance memory systems of the past that were interfaced to ECL buses had to rely on separate ECL translators and DRAM drivers to interface to large DRAM arrays, which is acceptable if the module is not highly interleaved and the bus cycle time is comparable to the DRAM access time. This becomes inadequate as the cycle time of the interface becomes significantly faster than the address timing requirements of the RAM, and as the degree of internal board interleaving increases. These higher performance demands require that the internal address and control signals propagated to the DRAM drivers be implemented in ECL, thus requiring the integration of the driver and translator functions.

Integration of the translator/drive function also reduces access latency, as well as keeping DRAM timing parameters from being violated, due to the excessive delays encountered with separate parts.

2. MOS Drive Capability

Outputs are specifically designed for driving large numbers of DRAMs (~ 300 pF), which reduce the number of parts and power requirements needed per board. Output voltage levels are designed specifically for driving DRAM inputs. No ECL translator parts on the market today provide the designer with this drive capability as well as the flexibility to vary the number of DRAMs that are driven by the part.

3. Transparent Latch

The latch is added to provide the capability for a memory controller to propagate new addresses to different banks without having to wait for the address timing constraints to be satisfied from a previous memory operation. For system implementations where this is acceptable, the user has the capability to keep the latch open, thus having the part act as an address translator/buffer, with minimal performance impact due to the additional propagation delay incurred from the internal latch. The latch is controlled with an already existing DRAM timing signal.

4. 1:2 Output Fanout

This function is useful in that it reduces input loading from the controller by a factor of two, thus significantly improving board etch propagation delays from the controller to the large number of translators, without the addition of ECL glue logic parts to reduce the loading. In large memory boards, so many translators are needed that this type of organization is not a handicap.

5. Low Skew, Low Propagation Delay

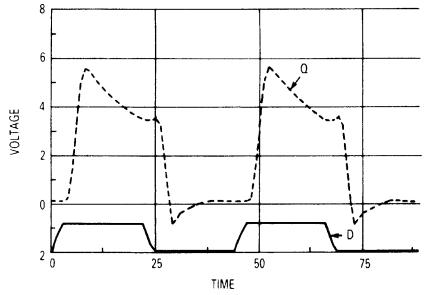
Low skew of the part as well as fast propagation delay enable faster overall DRAM operation to be attained than is possible with existing parts.

6. Power and Package Pin Layout

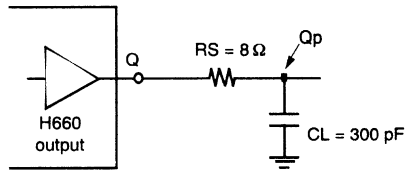
The H660 is specifically designed with additional power and ground pins to greatly improve simultaneous switching performance over existing driver parts.

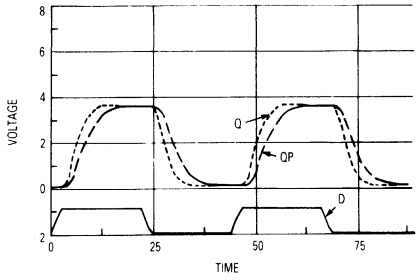
OUTPUT WAVEFORMS
simulated

Example 1. An output load consisting of just CL = 50 pF results in overshoot at the output Q:



Example 2. In a memory system application, use of an external source resistor is suggested. Simulations run with RS = 8Ω and CL = 300 pF leads to clean waveforms both at the output, Q, and at point Qp:



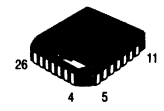


MOTOROLA

MC10H680
MC100H680

4-Bit Differential ECL Bus/TTL Bus Transceiver

4-BIT DIFFERENTIAL ECL BUS/TTL BUS TRANSCEIVER



FN SUFFIX
PLASTIC PACKAGE
CASE 776

2

The MC10H/100H680 is a dual supply 4-bit differential ECL bus to TTL bus transceiver. It is designed to allow the system designer to no longer be limited in bus speed associated with standard TTL busses. Using a differential ECL Bus will increase the frequency of operation and increase noise immunity.

Both the TTL and the ECL ports are capable of driving a bus. The ECL outputs have the ability to drive 25 Ω, allowing both ends of the bus line to be terminated in the characteristic impedance of 50 Ω. The TTL outputs are specified to source 15 mA and sink 48 mA, allowing the ability to drive highly capacitive loads.

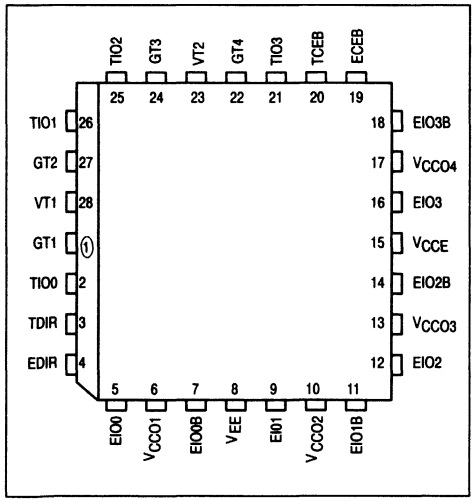
The ECL output levels are V_{OH} approximately equal to −1.0 V and V_{OL} cutoff equal to −2.0 V (VTT). When the ECL ports are disabled both EIOx and EIOxB go to the V_{OL} cutoff level. The ECL input receivers have special circuitry which detects this disabled condition, prevents oscillation, and forces the TTL output to the low state. The noise margin in this disabled state is greater than 600 mV. Multiple ECL V_{CCO} pins are utilized to minimize switching noise.

The TTL ports have standard levels. The TTL input receivers have PNP input devices to significantly reduce loading. Multiple TTL power and ground pins are utilized to minimize switching noise.

The control pins (EDIR and ECEB) of the 10H version is compatible with MECL 10H ECL logic levels. The control pins of the 100H version are compatible with 100K levels.

- Differential ECL Bus (25 Ω) I/O Ports
- High Drive TTL Bus I/O Ports
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- Direction and Chip Enable Control Pins
- Choice of ECL Compatibility: MECL 10H (10Hxxx) or 100K (100Hxxx)

PIN ASSIGNMENT



PIN NAMES

PIN	FUNCTION
GND[1:4]	TTL Ground
V_{CCO}[1:4]	ECL V_{CC} (0 V) — Outputs
V_{CCE}	ECL V_{CC} (0 V)
V_{CCT}[1:2]	TTL Supply (+5.0 V)
V_{EE}	ECL Supply (−5.2/−4.5 V)
EIO[0:3]	ECL I/O Non-Inverting Ports
EIO[0:3]B	ECL I/O Inverting Ports
TIO[0:3]	TTL I/O Ports
TDIR	TTL Direction Control
EDIR	ECL Direction Control
TCEB	TTL Chip Enable Bar Control
ECEB	ECL Chip Enable Bar Control

TRUTH TABLE

TDIR — Direction Control TTL Levels
EDIR — Direction Control ECL Levels
TCEB — Chip Enable Bar Control TTL Levels
ECEB — Chip Enable Bar Control ECL Levels
TIN — TTL Input
TOUT — TTL Output
EIN — ECL Input
EINB — ECL Input Bar
EOUT — ECL Output
EOUTB — ECL Output Bar

H — HIGH
L — LOW
LC — ECL Low Cutoff (VTT = −2.0 V)
X — Don't Care
Z — High Impedance

ECEB	TCEB	EDIR	TDIR	EIN	EINB	EOUT	EOUTB	TIN	TOUT	COMMENTS
H	X	X	X	X	X	LC	LC	X	Z	ECL and TTL Outputs Disabled
X	H	X	X	X	X	LC	LC	X	Z	ECL and TTL Outputs Disabled
L	L	H	X	H	LC			NA	H	ECL to TTL Direction
L	L	H	X	LC	H			NA	L	ECL to TTL Direction
L	L	H	X	LC	LC			NA	L	ECL to TTL Direction (L-L Cond.)
L	L	X	H	H	LC			NA	H	ECL to TTL Direction
L	L	X	H	LC	H			NA	L	ECL to TTL Direction
L	L	X	H	LC	LC			NA	L	ECL to TTL Direction (L-L Cond.)
L	L	L	L	NA	NA	H	LC	H		TTL to ECL Direction
L	L	L	L	NA	NA	LC	H	L		TTL to ECL Direction

Pin	Symbol	Description	Pin	Symbol	Description
1	GND1	TTL Gnd	15	V_{CCE}	ECL V_{CC}
2	TIO0	TTL I/O Bit 0	16	EIO3	ECL I/O Bit 3
3	TDIR	TTL Controlled Direction	17	V_{CCO4}	ECL V_{CC} (0 V) — Outputs
4	EDIR	ECL Controlled Direction	18	EIO3B	ECL I/O Bit 3 Bar
5	EIO0	ECL I/O Bit 0	19	ECEB	ECL Control Chip Enable Bar
6	V_{CCO1}	ECL V_{CC} (0 V) — Outputs	20	TCEB	TTL Control Chip Enable Bar
7	EIO0B	ECL I/O Bit 0 Bar	21	TIO3	TTL I/O Bit 3
8	V_{EE}	ECL V_{EE}	22	GND4	TTL GND
9	EIO1	ECL I/O Bit 1	23	V_{CCT2}	TTL V_{CC}
10	V_{CCO2}	ECL V_{CC} (0 V) — Outputs	24	GND3	TTL GND
11	EIO1B	ECL I/O Bit 1 Bar	25	TIO2	TTL I/O Bit 2
12	EIO2	ECL I/O Bit 2	26	TIO1	TTL I/O Bit 1
13	V_{CCO3}	ECL V_{CC} (0 V) — Outputs	27	GND2	TTL GND
14	EIO2B	ECL I/O Bit 2 Bar	28	V_{CCT1}	TTL V_{CC}

ABSOLUTE RATINGS (Do not exceed):

Power Supply Voltage	V_{EE} (ECL)	−8.0 to 0	Vdc
Power Supply Voltage	V_{CCT} (TTL)	−0.5 to +7.0	Vdc
Input Voltage	V_I (ECL) V_I (TTL)	0.0 to V_{EE} −0.5 to +7.0	Vdc
Disabled 3-State Output	V_{out} (TTL)	0.0 to V_{CCT}	Vdc
Output Source Current Continuous	I_{out} (ECL)	100	mAdc
Output Source Current Surge	I_{out} (ECL)	200	mAdc
Storage Temperature	T_{stg}	−65 to 150	°C
Operating Temperature	T_{amb}	0.0 to +75	°C

ECL DC CHARACTERISTICS: V_{CCT} = +5.0 V ±10%, V_{EE} = −5.2 ±5% (10H Version); V_{EE} = −4.2 V to −5.5 V (100H Version)

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	Supply Current/ECL		−110		−110		−110	mA	
I_{INH}	Input HIGH Current		225		145		145	µA	
I_{INL}	Input LOW Current	0.5		0.5		0.3		µA	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	−1100 −2.1	−840 −2.03	−1100 −2.1	−810 −2.03	−1100 −2.1	−735 −2.03	mV V	25 Ω to −2.1 V

CONTROL INPUTS ONLY
10H ECL DC CHARACTERISTICS: V_{CCT} = +5.0 ±10%, V_{EE} = −5.2 ±5%

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	−1170 −1950	−840 −1480	−1130 −1950	−810 −1480	−1070 −1950	−735 −1450	mV	

CONTROL INPUTS ONLY
100H ECL DC CHARACTERISTICS: V_{CCT} = +5.0 ±10%, V_{EE} = −4.2 V to −5.5 V

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	−1165 −1810	−880 −1475	−1165 −1810	−880 −1475	−1165 −1810	−880 −1475	mV	

TTL DC CHARACTERISTICS: V_{CCT} = +5.0 V ±10%, V_{EE} = −5.2 ±5% (10H Version); V_{EE} = −4.2 V to −5.5 V (100H Version)

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Standard Input Standard Input	2.0	 0.8	2.0	 0.8	2.0	 0.8	Vdc	
V_{IK}	Input Clamp		−1.2		−1.2		−1.2	Vdc	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = −3.0 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage		0.55		0.55		0.55	V	I_{OL} = 48 mA
I_{IH}*	TTL (Input HIGH) TTL (Input HIGH)		20 100		20 100		20 100	µA	V_{in} = 2.7 V V_{in} = 7.0 V
I_{IL}*	TTL (Input LOW)		−0.6		−0.6		−0.6	mA	V_{in} = 0.5 V
I_{CCL}	Supply Current		75		75		75	mA	
I_{CCH}	Supply Current		70		70		70	mA	
I_{CCZ}	Supply Current		70		70		70	mA	
I_{OS}	Output Short Circuit Current	−100	−225	−100	−225	−100	−225	mA	V_{OUT} = 0 V

* NOTE: TTL Control Inputs only

TTL I/O DC CHARACTERISTICS ONLY

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
$I_{IH/IOZH}$ $I_{IL/IOZL}$	Output Disable Current		70 200		70 200		70 200	µA	V_{OUT} = 2.7 V V_{OUT} = 0.5 V

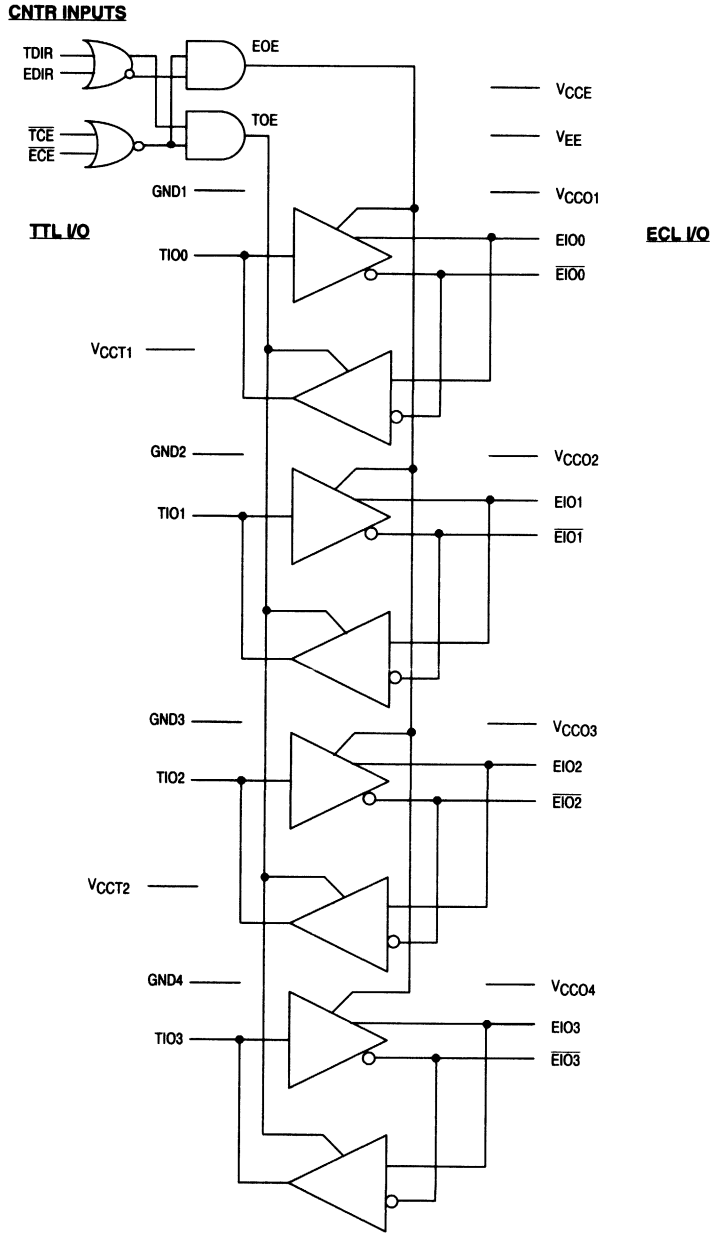
ECL TO TTL DIRECTION / AC TEST

Test Symbol	Parameter	Waveforms	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	2, 4	2.7	4.8	2.7	4.8	2.7	4.8	ns	C_L = 50 pF
t_{PZH} t_{PZL}	ECEB to Output Enable Time	2, 5, 6	4.5 4.0	6.5 6.0	4.5 4.0	6.5 6.0	4.7 4.4	6.7 6.4	ns	C_L = 50 pF
t_{PHZ} t_{PLZ}	ECEB to Output Disable Time	2, 5, 6	4.6 4.5	8.6 6.5	4.6 4.5	8.6 6.5	4.8 5.3	8.8 7.3	ns	C_L = 50 pF
t_{PZH} t_{PZL}	TCEB to Output Enable Time	2, 5, 6	5.7 5.4	7.7 6.9	5.7 5.4	7.7 6.9	5.9 5.9	7.9 7.4	ns	C_L = 50 pF
t_{PHZ} t_{PLZ}	TCEB to Output Disable Time	2, 5, 6	4.0 4.0	8.5 5.8	4.1 4.2	8.4 6.0	4.2 4.7	8.3 6.5	ns	C_L = 50 pF
t_r/t_f	1.0 to 2.0 Vdc	3	0.4	1.5	0.4	1.5	0.4	1.5	ns	C_L = 50 pF

TTL TO ECL DIRECTION / AC TEST

Test Symbol	Parameter	Waveforms	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	1, 4	1.8	4.6	1.8	4.6	2.0	4.9	ns	25 Ω to −2.0 V
t_{PLH} t_{PHL}	ECEB to Output	1, 4	2.9	5.1	3.0	5.2	3.4	5.7	ns	25 Ω to −2.0 V
t_{PLH} t_{PHL}	TCEB to Output	1, 4	3.4	6.3	3.5	6.6	3.8	7.4	ns	25 Ω to −2.0 V
t_r/t_f	Output Rise/Fall Time 20%−80%	1, 3	1.0	3.4	1.0	3.4	1.0	3.4	ns	25 Ω to −2.0 V

BLOCK DIAGRAM



SWITCHING CIRCUIT AND WAVEFORMS

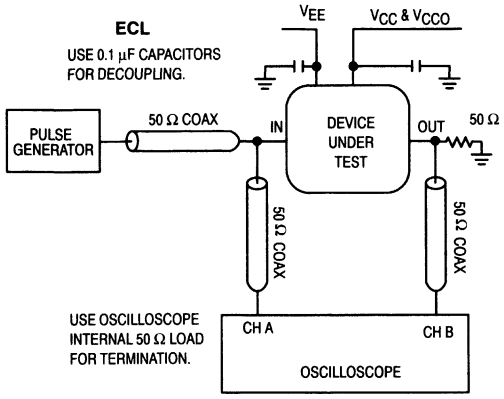


Figure 1. Switching Circuit ECL

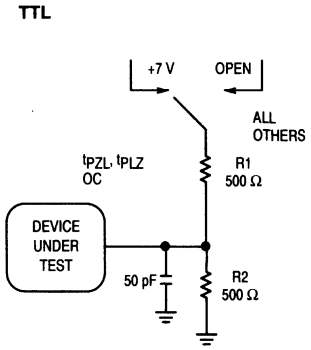


Figure 2.

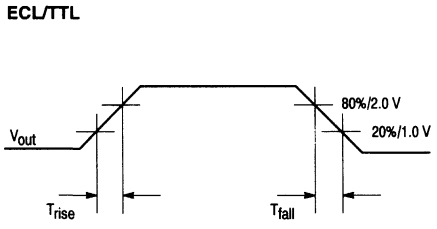


Figure 3. WAVEFORMS: Rise and Fall Times

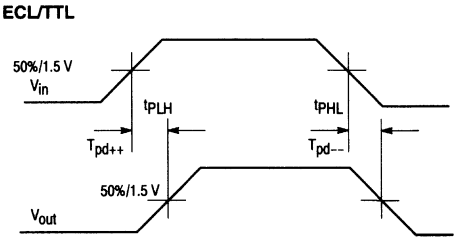


Figure 4. Propagation Delay — Single Ended

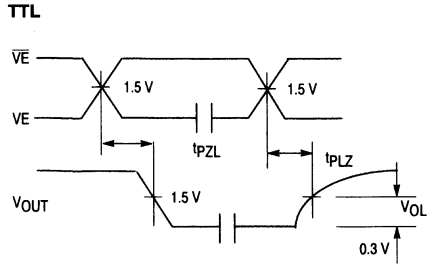


Figure 5. 3-State Output Low Enable and Disable Times

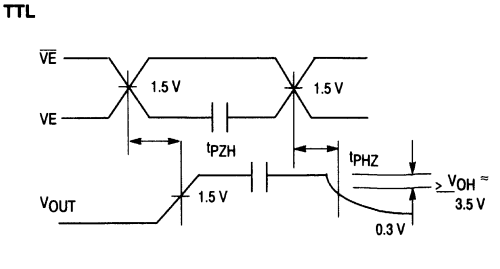
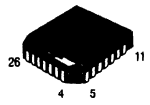


Figure 6. 3-State Output High Enable and Disable Times

MOTOROLA

MC10H681
MC100H681

HEX ECL/TTL TRANSCEIVER WITH LATCHES



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CASE 776

2

Hex ECL/TTL Transceiver with Latches

The MC10/100H681 is a dual supply Hex ECL/TTL transceiver with latches in both directions. ECL controlled Direction and Chip Enable Bar pins. There are two Latch Enable pins, one for each direction.

The ECL outputs are single ended and drive 50 Ω. The TTL outputs are specified to source 12 mA and sink 48 mA, allowing the ability to drive highly capacitive loads. The high driving ability of the TTL outputs make the device ideal for bussing applications.

- Separate Latch Enable Controls for each Direction
- ECL Single Ended 50 Ω I/O Port
- High Drive TTL I/O Ports
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- Direction and Chip Enable Control Pins
- Choice of ECL Compatibility: MECL 10H (10Hxxx) or 100K (100Hxxx)

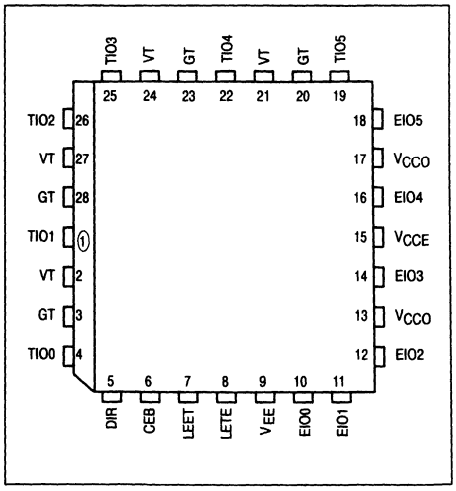
The ECL output levels are standard V_{OH} and V_{OL} cutoff equal to –2.0 V (V_{TT}). When the ECL ports are disabled the outputs go to the V_{OL} cutoff level. Multiple ECL V_{CCO} pins are utilized to minimize switching noise.

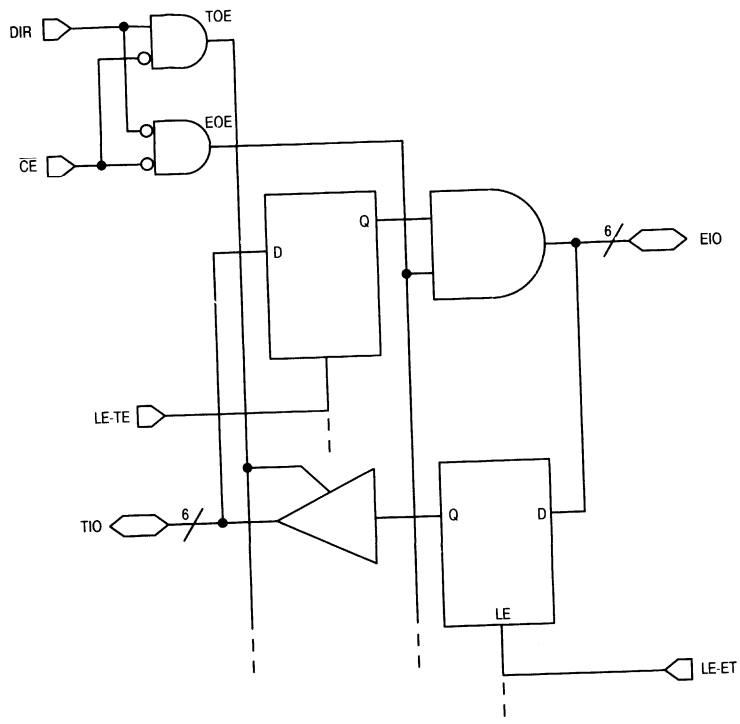
The TTL ports have standard levels. The TTL input receivers have PNP input devices to significantly reduce loading. Multiple TTL power and ground pins are utilized to minimize switching noise.

The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

Pin	Symbol	Description
1	TI01	TTL I/O BIT 1
2	VT	TTL V_{CC} (5.0 V)
3	GT	TTL GND (0 V)
4	TI00	TTL I/O Bit 0
5	DIR	Direction Control (ECL)
6	CEB	Chip Enable Bar Control (ECL)
7	LEET	Latch Enable ECL-TTL Control (ECL)
8	LETE	Latch Enable TTL-ECL Control (ECL)
9	V_{EE}	ECL Supply (–5.2/–4.5 V)
10	EI00	ECL I/O BIT 0
11	EI01	ECL I/O BIT 1
12	EI02	ECL I/O BIT 2
13	V_{CCO}	ECL V_{CC} (0 V) — Outputs
14	EIO3	TTL I/O BIT 3
15	V_{CCE}	ECL V_{CC} (0 V)
16	EIO4	ECL I/O BIT 4
17	V_{CCO}	ECL V_{CC} (0 V) — Outputs
18	EIO5	ECL I/O BIT 5
19	TI05	TTL I/O BIT 5
20	GT	TTL GND (0 V)
21	VT	TTL V_{CC} (5.0 V)
22	TI04	TTL I/O BIT 4
23	GT	TTL GND (0 V)
24	VT	TTL V_{CC} (5.0 V)
25	TIO3	TTL I/O BIT 3
26	TIO2	TTL I/O BIT 2
27	VT	TTL V_{CC} (5.0 V)
28	GT	TTL V_{CC} (0 V)

PIN ASSIGNMENT





TRUTH TABLE

CEB	DIR	LEET	LETE	EOUT	TOUT
H	X	X	X	Z	Z
L	H	L	L	Z	EIN
L	H	H	L	Z	Qo
L	L	L	L	TIN	Z
L	L	L	H	Qo	Z

- Hex
- Bi-Directional
- ECL/TTL Translation
- Dual Supply
- ECL Outputs, 50 Ohm S.E., V_{OH}/Cutoff
- TTL Outputs, 48 mA Sink, 12 mA Source
- Multi Power and Ground Pins
- Separate LE Controls

ECL DC CHARACTERISTICS: V_{CCT} = +5.0 V ±10%, V_{EE} = −5.2 ±5% (10H Version); V_{EE} = −4.2 V to −5.5 V (100H Version)

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	Supply Current/ECL	—	−113	—	−113	—	−113	mA	
I_{INH}	Input HIGH Current	—	225	—	145	—	145	µA	
I_{INL}	Input LOW Current	0.5	—	0.5	—	0.3	—	µA	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	−1100 −2.1	−840 −2.03	−1100 −2.1	−810 −2.03	−1100 −2.1	−735 −2.03	mV V	50 Ω to −2.1 V

10H ECL DC CHARACTERISTICS: V_{CCT} = +5.0 ±10%, V_{EE} = −5.2 ±5%

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	−1170 −1950	−840 −1480	−1130 −1950	−810 −1480	−1070 −1950	−735 −1450	mV	

100H ECL DC CHARACTERISTICS: V_{CCT} = +5.0 ±10%, V_{EE} = −4.2 V to −5.5 V

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	−1165 −1810	−880 −1475	−1165 −1810	−880 −1475	−1165 −1810	−880 −1475	mV	

ABSOLUTE RATINGS (Do not exceed):

Power Supply Voltage	V_{EE} (ECL)	−8.0 to 0	Vdc
Power Supply Voltage	V_{CCT} (TTL)	−0.5 to +7.0	Vdc
Input Voltage	V_I (ECL) V_I (TTL)	0.0 to V_{EE} −0.5 to +7.0	Vdc
Disabled 3-State Output	V_{out} (TTL)	0.0 to V_{CCT}	Vdc
Output Source Current Continuous	I_{out} (ECL)	100	mAdc
Output Source Current Surge	I_{out} (ECL)	200	mAdc
Storage Temperature	T_{stg}	−65 to 150	°C
Operating Temperature	T_{amb}	0.0 to +75	°C

TTL DC CHARACTERISTICS: V_{CCT} = +5.0 V ±10%, V_{EE} = −5.2 ±5% (10H Version); V_{EE} = −4.2 V to −5.5 V (100H Version)

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Standard Input Standard Input	2.0 —	— 0.8	2.0 —	— 0.8	2.0 —	— 0.8	Vdc	
V_{IK}	Input Clamp	—	−1.2	—	−1.2	—	−1.2	Vdc	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = −3.0 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage	—	0.55	—	0.55	—	0.55	V	I_{OL} = 48 mA
I_{IH}/I_{OZH} I_{IL}/I_{OZL}	Output Disable Current	— —	70 200	— —	70 200	— —	70 200	µA	V_{OUT} = 2.7 V V_{OUT} = 0.5 V
I_{CCL}	Supply Current	—	63	—	63	—	63	mA	
I_{CCH}	Supply Current	—	63	—	63	—	63	mA	
I_{CCZ}	Supply Current	—	63	—	63	—	63	mA	
I_{OS}	Output Short Circuit Current	−100	−225	−100	−225	−100	−225	mA	V_{OUT} = 0 V

2

ECL TO TTL DIRECTION AC CHARACTERISTICS

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	4.0	7.8	4.0	7.8	4.2	8.0	ns	C_L = 50 pF
t_{PLH} t_{PHL}	LEET to Output	6.4 5.8	9.1 7.6	6.4 5.8	9.1 7.6	6.6 6.1	9.3 8.0	ns	C_L = 50 pF
t_{PZH} t_{PZL}	CEB to Output Enable Time	5.5 5.6	8.3 8.5	5.5 5.6	8.3 8.5	4.7 5.7	8.5 8.6	ns	C_L = 50 pF
t_{PHZ} t_{PLZ}	CEB to Output Disable Time	3.9 3.7	7.6 5.5	3.9 3.7	7.6 5.5	4.1 4.3	7.7 6.0	ns	C_L = 50 pF
t_r/t_f	1.0 Vdc to 2.0 Vdc	0.4	2.2	0.4	2.2	0.4	2.2	ns	C_L = 50 pF

TTL TO ECL DIRECTION AC CHARACTERISTICS

Test Symbol	Parameter	T_A = 0°C		T_A = 25°C		T_A = 75°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	2.1	4.0	2.1	4.0	2.5	4.5	ns	50 Ω to −2.0 V
t_{PLH} t_{PHL}	CEB to Output	2.3 3.0	4.0 4.6	2.5 3.0	4.0 4.6	2.9 3.3	4.3 5.0	ns	50 Ω to −2.0 V
t_{PHL} t_{PLH}	LETE to Output	2.7	4.2	2.7	4.2	3.0	4.6	ns	50 Ω to −2.0 V
t_r/t_f	Output Rise/Fall Time 20%−80%	0.4	2.2	0.4	2.2	0.4	2.2	ns	50 Ω to −2.0 V

TEST CIRCUITS AND WAVEFORMS

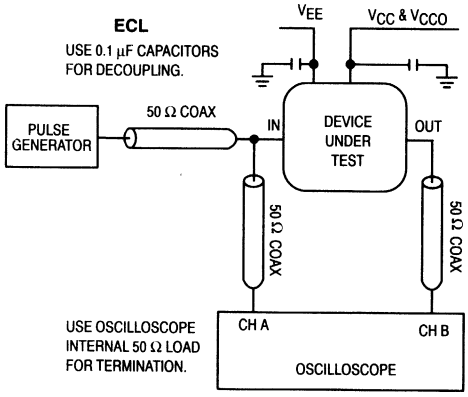


Figure 1. Test Circuit ECL

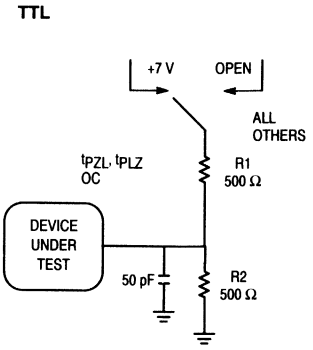


Figure 2. Test Circuit TTL

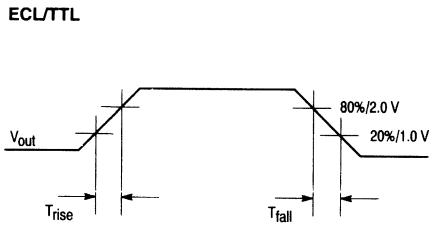


Figure 3. Rise and Fall Times

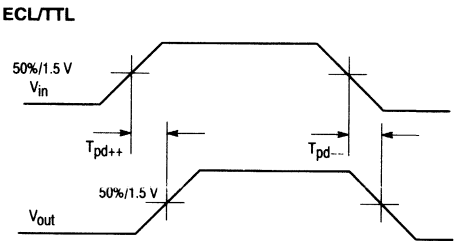


Figure 4. Propagation Delay — Single Ended

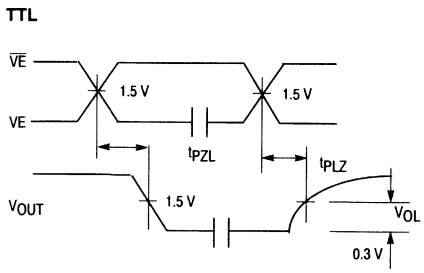


Figure 5. 3-State Output Low Enable and Disable Times

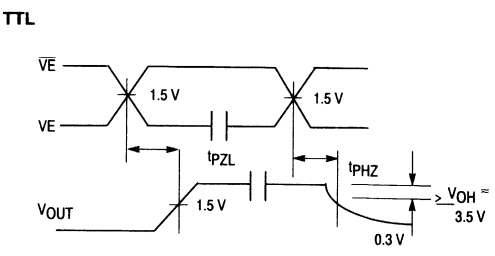
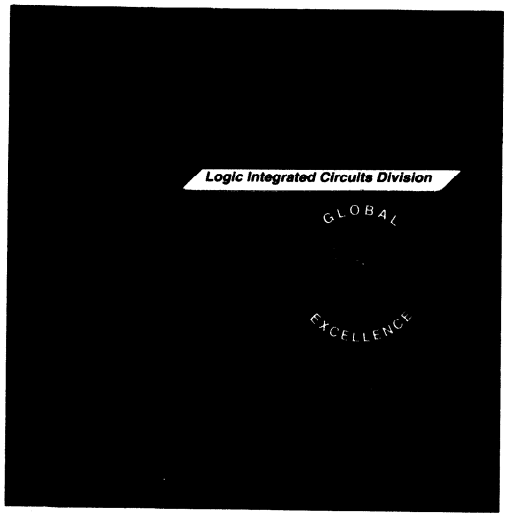


Figure 6. 3-State Output High Enable and Disable Times



MECL 10K

Selector Guide | **Data Sheets** | **3**

MECL 10K
INTEGRATED CIRCUITS

MC10,100/10,200 Series
–30 to 85°C

Function Selection — (–30° to +85°C)

Function	Device	Case
NOR Gates		
Quad 2-Input Gate/Strobe	MC10100	620, 648, 775
Quad 2-Input Gate	MC10102	620, 648, 775
Triple 4-3-3 Input Gate	MC10106	620, 648, 775
Dual 3-Input 3-Output Gate	MC10111	620, 648, 775
Dual 3-Input 3-Output Gate	MC10211	620, 648, 775
OR Gates		
Quad 2-Input Gate	MC10103	620, 648, 775
Dual 3-Input 3-Output Gate	MC10110	620, 648, 775
Dual 3-Input 3-Output Gate	MC10210	620, 648, 775
AND Gates		
Quad 2-Input Gate	MC10104	620, 648, 775
Hex Gate	MC10197	620, 648, 775
Complex Gates		
Quad OR/NOR Gate	MC10101	620, 648, 775
Triple 2-3-2 Input OR/NOR Gate	MC10105	620, 648, 775
Dual 4-5 Input OR/NOR Gate	MC10109	620, 648, 775
Dual 3-Input 3-Output OR/NOR Gate	MC10212	620, 648, 775
Triple 2-Input Exclusive OR/NOR Gate	MC10107	620, 648, 775
Quad 2-Input Exclusive OR/NOR Gate	MC10113	620, 648, 775
Dual 2-Wide 2-3 Input OR-AND/OR-AND INVERT	MC10117	620, 648, 775
Dual 2-Wide 3-Input OR-AND	MC10118	620, 648, 775
4-Wide 4-3-3-3 Input OR-AND	MC10119	620, 648, 775
4-Wide 3-Input OR-AND/OR-AND INVERT	MC10121	620, 648, 775
Buffers/Inverters		
Hex Buffer/Enable	MC10188	620, 648, 775
Hex Inverter/Enable	MC10189	620, 648, 775
Hex Inverter/Buffer	MC10195	620, 648, 775
Line Drivers/Line Receivers		
Triple Line Receiver	MC10114	620, 648, 775
Quad Line Receiver	MC10115	620, 648, 775
Triple Line Receiver	MC10116	620, 648, 775
Quad Bus Receiver	MC10129	620
Quad Bus Driver	MC10192	620, 648, 775
Triple Line Receiver	MC10216	620, 648, 775
Triple 4-3-3 Input Bus Driver	MC10123	620, 648, 775
Dual Bus Driver	MC10128	620
Translators		
Quad TTL-MECL	MC10124	620, 648, 775
Quad MECL-TTL	MC10125	620, 648, 775
Quad MST to MECL	MC10190	620, 648, 775

Function	Device	Case
Flip-Flop/Latches		
Dual D Master Slave Flip-Flop	MC10131	620, 648, 775
Dual J-K Master Slave Flip-Flop	MC10135	620, 648, 775
Hex D Master Slave Flip-Flop	MC10176	620, 648, 775
Hex D Common Reset Flip-Flop	MC10186	620, 648, 775
Dual D Master Slave Flip-Flop	MC10231	620, 648, 775
Quad Latch	MC10133	620, 648, 775
Quint Latch	MC10175	620, 648, 775
Quad/Common Clock Latch	MC10168	620, 648, 775
Quad/Negative Clock Latch	MC10153	620, 648, 775
Dual Latch	MC10130	620, 648, 775
Encoders		
8-Input Encoder	MC10165	620, 648, 775
Decoders		
Binary to 1-8 (Low)	MC10161	620, 648, 775
Binary to 1-8 (High)	MC10162	620, 648, 775
Dual Binary to 1-4 (Low)	MC10171	620, 648, 775
Dual Binary to 1-4 (High)	MC10172	620, 648, 775
Parity Generator/Checkers		
12-Bit Parity Generator-Checker	MC10160	620, 648, 775
9 + 2 Bit Parity	MC10170	620, 648, 775
Counters		
Hexadecimal	MC10136	620, 648, 775
Decade	MC10137	620, 648
Biquinary	MC10138	620, 648, 775
Binary Down Counter	MC10154	620, 648
Binary	MC10178	620, 648, 775
Arithmetic Functions		
5-Bit Magnitude Comparator	MC10166	620, 648, 775
4-Bit Arithmetic Function Gen.	MC10181	623, 649
Shift Register		
4-Bit Universal	MC10141	620, 648, 775
Multivibrators		
Monostable Multivibrators	MC10198	620, 648, 775
Multiplexer		
Quad 2-Input/Noninverting	MC10158	620, 648, 775
Dual Multiplexer/Latch	MC10132	620, 648
Dual Multiplexer/Latch	MC10134	620, 648, 775
Quad 2-Input/Inverting	MC10159	620, 648, 775
8-Line	MC10164	620, 648, 775
Quad 2-Input/Latch	MC10173	620, 648, 775
Dual 4-1	MC10174	620, 648, 775

MOTOROLA

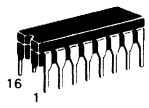
MC10100

QUAD 2-INPUT NOR GATE WITH STROBE

The MC10100 is a quad NOR gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates.

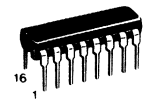
P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

QUAD 2-INPUT NOR GATE WITH STROBE



L SUFFIX
CERAMIC PACKAGE
CASE 620

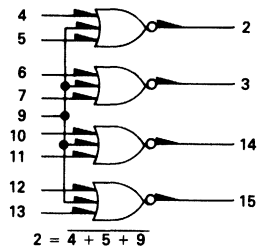
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

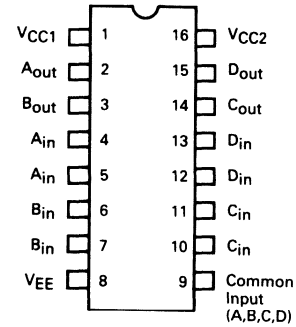
3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10100 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	—	29	—	21	26	—	29	mAdc	—	—	—	—	8	1,16
Input Current	I_{inH}	4*	—	390	—	—	245	—	245	μAdc	4*	—	—	—	8	1,16
		9	—	750	—	—	470	—	470	μAdc	9	—	—	—	8	1,16
	I_{inL}	4*	0.5	—	0.5	—	—	0.3	—	μAdc	—	4*	—	—	8	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	—	−0.810	−0.890	−0.700	Vdc	—	—	—	—	8	1,16
		14	−1.060	−0.890	−0.960	—	−0.810	−0.890	−0.700	Vdc	—	—	—	—	8	1,16
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	—	−1.650	−1.825	−1.615	Vdc	4,5,9	—	—	—	8	1,16
		14	−1.890	−1.675	−1.850	—	−1.650	−1.825	−1.615	Vdc	9,10,11	—	—	—	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	—	−0.980	—	—	−0.910	—	Vdc	—	—	—	—	9	8	1,16
		3	−1.080	—	−0.980	—	—	−0.910	—	↓	—	—	—	—	9	↓	↓
		14	−1.080	—	−0.980	—	—	−0.910	—		—	—	—	—	9		
		15	−1.080	—	−0.980	—	—	−0.910	—		—	—	—	—	9		
Logic "0" Threshold Voltage	V_{OLA}	2	—	−1.655	—	—	−1.630	—	−1.595	Vdc	—	—	9	—	8	1,16
		3	—	−1.655	—	—	−1.630	—	−1.595	↓	—	—	9	—	↓	↓
		14	—	−1.655	—	—	−1.630	—	−1.595		—	—	9	—		
		15	—	−1.655	—	—	−1.630	—	−1.595		—	—	9	—		
Switching Times (50-ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t_{4+2-}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	—	—	4	2	8	1,16
	t_{4-2+}	2	1.0	3.1	1.0	↓	2.9	1.0	3.3	↓	—	—	4	↓	↓	↓
	t_{9+2-}	2	1.0	3.1	1.0		2.9	1.0	3.3		6,10,12	—	9			
Rise Time (20% to 80%)	t_{2+}	2	1.1	3.6	1.1		3.3	1.1	3.7		—	—	4			
Fall Time (20% to 80%)	t_{2-}	2	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	—	—	4	↓	↓	↓

*Individually test each input applying V_{IH} or V_{IL} to input under test.

MOTOROLA

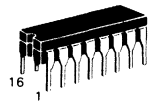
MC10101

QUAD OR/NOR GATE

The MC10101 is a quad 2-input OR/NOR gate with one input from each gate common to pin 12.

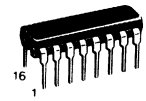
P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

QUAD OR/NOR GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

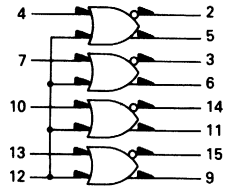
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

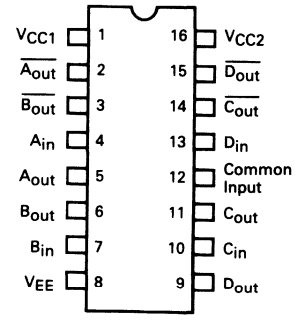
3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10101 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	425	–	–	265	–	265	μAdc	4	–	–	–	8	1,16
		12	–	850	–	–	535	–	535	μAdc	12	–	–	–	8	1,16
	I_{inL}	4	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
		12	0.5	–	0.5	–	–	0.3	–	μAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	5	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	12	–	–	–	8	1,16
		5	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	↓	4	–	–	–	↓	↓
		2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	↓	–	–	–	–	↓	↓
		2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	↓	–	–	–	–	↓	↓
Logic "0" Output Voltage	V_{OL}	5	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	–	–	–	8	1,16
		5	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	↓	–	–	–	–	↓	↓
		2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	↓	12	–	–	–	↓	↓
		2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	↓	4	–	–	–	↓	↓
Logic "1" Threshold Voltage	V_{OHA}	5	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	12	–	8	1,16
		5	−1.080	–	−0.980	–	–	−0.910	–	↓	–	–	4	–	↓	↓
		2	−1.080	–	−0.980	–	–	−0.910	–	↓	–	–	–	12	↓	↓
		2	−1.080	–	−0.980	–	–	−0.910	–	↓	–	–	–	4	↓	↓
Logic "0" Threshold Voltage	V_{OLA}	5	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	12	8	1,16
		5	–	−1.655	–	–	−1.630	–	−1.595	↓	–	–	–	4	↓	↓
		2	–	−1.655	–	–	−1.630	–	−1.595	↓	–	–	12	–	↓	↓
		2	–	−1.655	–	–	−1.630	–	−1.595	↓	–	–	4	–	↓	↓
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2-}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	2	8	1,16
	t_{4-2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
	t_{4+5+}	5	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	5	↓	↓
	t_{4-5-}	5	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	5	↓	↓
Rise Time (20 to 80%)	t_{2+}	2	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	–	–	↓	2	↓	↓
	t_{5+}	5	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	5	↓	↓
Fall Time (20 to 80%)	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
	t_{5-}	5	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	5	↓	↓

MOTOROLA

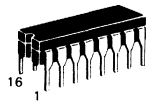
MC10102

QUAD 2-INPUT NOR GATE

The MC10102 is a quad 2-input NOR gate. The MC10102 provides one gate with OR/NOR outputs.

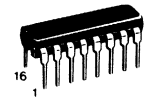
P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

QUAD 2-INPUT NOR GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

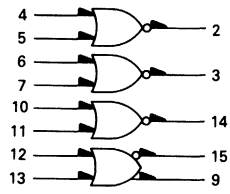
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

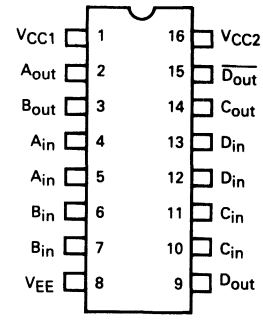
3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10102 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	12	–	425	–	–	265	–	265	μAdc	12	–	–	–	8	1,16
	I_{inL}	12	0.5	–	0.5	–	–	0.3	–	μAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	9	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	–	–	–	8	1,16
		9	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	↓	13	–	–	–	↓	↓
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	↓	–	–	–	–	↓	↓
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	↓	–	–	–	–	↓	↓
Logic "0" Output Voltage	V_{OL}	9	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		9	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	↓	–	–	–	–	↓	↓
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	↓	12	–	–	–	↓	↓
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	↓	13	–	–	–	↓	↓
Logic "1" Threshold Voltage	V_{OHA}	9	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	12	–	8	1,16
		9	-1.080	–	-0.980	–	–	-0.910	–	↓	–	–	13	–	↓	↓
		15	-1.080	–	-0.980	–	–	-0.910	–	↓	–	–	–	12	↓	↓
		15	-1.080	–	-0.980	–	–	-0.910	–	↓	–	–	–	13	↓	↓
Logic "0" Threshold Voltage	V_{OLA}	9	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	12	8	1,16
		9	–	-1.655	–	–	-1.630	–	-1.595	↓	–	–	–	13	↓	↓
		15	–	-1.655	–	–	-1.630	–	-1.595	↓	–	–	12	–	↓	↓
		15	–	-1.655	–	–	-1.630	–	-1.595	↓	–	–	13	–	↓	↓
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{12+15-}	15	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	12	15	8	1,16
	t_{12-15+}	15	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	15	↓	↓
	t_{12+9+}	9	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	9	↓	↓
	t_{12-9-}	9	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	9	↓	↓
Rise Time	t_{15+}	15	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	–	–	↓	15	↓	↓
(20 to 80%)	t_{9+}	9	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	9	↓	↓
Fall Time	t_{15-}	15	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	15	↓	↓
(20 to 80%)	t_{9-}	9	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	9	↓	↓

MOTOROLA

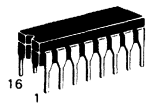
MC10103

QUAD 2-INPUT OR GATE

The MC10103 is a quad 2-input OR gate. The MC10103 provides one gate with OR/NOR outputs.

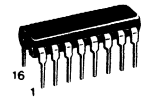
P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

QUAD 2-INPUT OR GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

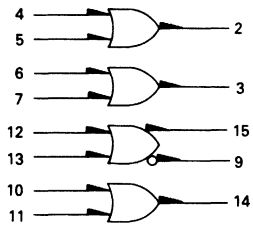
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

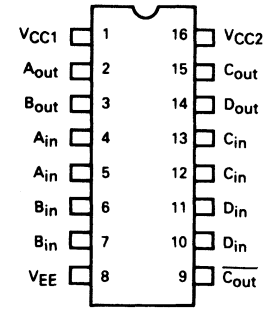
3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10103 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	21	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4*	–	390	–	–	245	–	245	μAdc	4*	–	–	–	8	1,16
	I_{inL}	4*	0.5	–	0.5	–	–	0.3	–	μAdc	–	4*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,5	–	–	–	8	1,16
		9	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	—	–	–	–	8	1,16
		9	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	12,13	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	4,5	—	8	1,16
		9	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	12,13	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	—	4,5	8	1,16
		9	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	12,13	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	2	8	1,16
	t_{12+9-}	9	1.0	3.1	1.0		2.9	1.0	3.3		–	–	12	9		
Rise Time (20% to 80%)	t_{2+}	2	1.1	3.6	1.1		3.3	1.1	3.7		–	–	4	2		
Fall Time (20% to 80%)	t_{2-}	2	1.1	3.6	1.1		3.3	1.1	3.7		–	–	4	2		

*Individually test each input applying V_{IH} or V_{IL} to input under test.

MOTOROLA

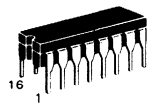
MC10104

QUAD 2-INPUT AND GATE

The MC10104 is a quad 2-input AND gate. One of the gates has both AND/NAND outputs available.

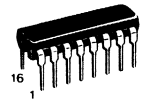
P_D = 35 mW typ/gate (No Load)
t_{pd} = 2.7 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

QUAD 2-INPUT AND GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

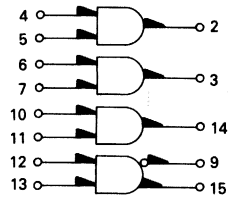
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

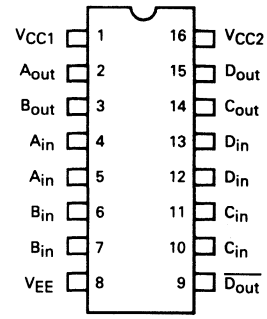
3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Test	MC10104 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BLEOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	39	–	–	35	–	39	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}*	12	–	425	–	–	265	–	265	µAdc	12,13	–	–	–	8	1,16
		13	–	350	–	–	220	–	220	µAdc	13	–	–	–	8	1,16
	I_{inL}	12	0.5	–	0.5	–	–	0.3	–	µAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12,13	–	–	–	8	1,16
		9	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		9	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	12,13	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	9	-1.090	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	12	8	1,16
		9	-1.090	–	-0.980	–	–	-0.910	–		–	–	–	13		
		15	-1.090	–	-0.980	–	–	-0.910	–		12	–	13			
		15	-1.090	–	-0.980	–	–	-0.910	–		13	–	12			
Lgoic "0" Threshold Voltage	V_{OLA}	9	–	-1.655	–	–	-1.630	–	-1.595	Vdc	12	–	13		8	1,16
		9	–	-1.655	–	–	-1.630	–	-1.595		13	–	12			
		15	–	-1.655	–	–	-1.630	–	-1.595		–	–	–	12		
		15	–	-1.655	–	–	-1.630	–	-1.595		–	–	–	13		
Switching Times* (50-ohm load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{12+15+}	15	1.0	4.3	1.0	2.2	4.0	1.0	4.2	ns	13	–	12	15	8	1,16
	t_{12-15-}	15									–			15		
	t_{12+9-}	9									–			9		
	t_{12-9+}	9									–			9		
	t_{13+15+}	15				2.7					12	–	13	15		
	t_{13+9-}	9				2.7					12	–	13	9		
Rise Time (20 to 80%)	t_{15+}	15	1.5	3.7	1.5	2.0	3.5	1.5	3.6		–	–	–	15		
	t_{9+}	9									–	–	–	9		
Fall Time (20 to 80%)	t_{15-}	15									–	–	–	15		
	t_{9-}	9									–	–	–	9		

*Inputs 4, 7, 10, and 13 will behave similarly for ac and I_{inH} values.

Inputs 5, 6, 11, and 12 will behave similarly for ac and I_{inH} values.

MOTOROLA

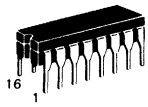
MC10105

TRIPLE 2-3-2-INPUT OR/NOR GATE

The MC10105 is a triple 2-3-2 input OR/NOR gate.

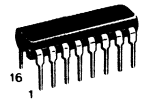
P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

TRIPLE 2-3-2-INPUT OR/NOR GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

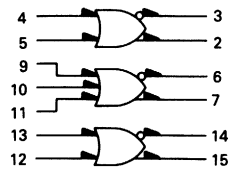
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

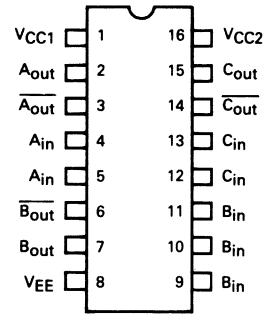
3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10105 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	23	–	17	21	–	23	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4		425	–	–	265	–	265	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	4	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3		-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2		-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	4	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	3	8	1,16
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓
	t_{4+2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
Rise Time (20 to 80%)	t_{3+}	3	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	–	↓	↓	3	↓	↓
	t_{2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
Fall Time (20 to 80%)	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓
	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓

MOTOROLA

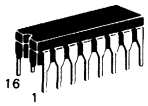
MC10106

TRIPLE 4-3-3-INPUT NOR GATE

The MC10106 is a triple 4-3-3 input NOR gate.

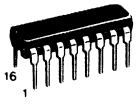
P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

TRIPLE 4-3-3-INPUT NOR GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

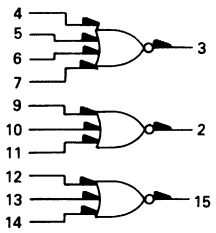
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

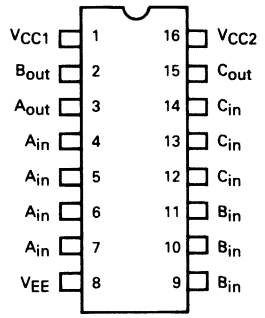
3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10106 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	23	–	17	21	–	23	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in}H$	4	–	425	–	–	265	–	265	μAdc	4	–	–	–	8	1,16
	$I_{in}L$	4	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.080		-0.980			-0.910			–	–	–	9	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2		-1.655			-1.630		-1.595		–	–	9	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	3	8	1,16
	t_{4-3+}		1.0	3.1	1.0		2.9	1.0	3.3		–	–				
Rise Time (20 to 80%)	t_{3+}		1.1	3.6	1.1		3.3	1.1	3.7		–	–				
Fall Time (20 to 80%)	t_{3-}		1.1	3.6	1.1		3.3	1.1	3.7		–	–				

MOTOROLA

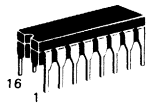
MC10107

TRIPLE 2-INPUT EXCLUSIVE "OR"/EXCLUSIVE "NOR"

The MC10107 is a triple-2 input exclusive OR/NOR gate.

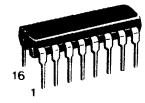
P_D = 40 mW typ/gate (No Load)
t_{pd} = 2.8 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

TRIPLE 2-INPUT EXCLUSIVE "OR"/EXCLUSIVE "NOR"



L SUFFIX
CERAMIC PACKAGE
CASE 620

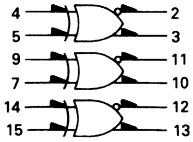
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

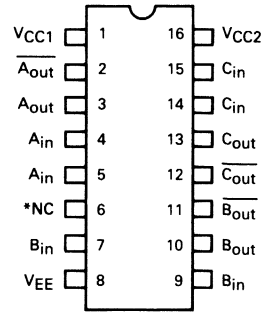
LOGIC DIAGRAM



$3 = (4 \cdot \bar{5}) + (\bar{4} \cdot 5)$
$2 = (\bar{4} \cdot \bar{5}) + (4 \cdot 5)$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



*NC = No Connection

Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10107 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	31	–	28	–	31	mAdc	5,7,15	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4,9,14	–	425	–	265	–	265	µAdc	*	–	–	–	8	1,16
		5,7,15	–	350	–	220	–	220	µAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	0.5	–	0.5	–	0.3	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	4,5	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		–	–	–	–		
		3	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		4	–	–	–		
		3	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		5	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		5	–	–	–		
		3	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		4,5	–	–	–		
		3	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		–	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	-0.910	–	Vdc	5	–	4	–	8	1,16
		2	-1.080	–	-0.980	–	-0.910	–		–	–	–	4		
		3	-1.080	–	-0.980	–	-0.910	–		–	–	4	–		
		3	-1.080	–	-0.980	–	-0.910	–		–	–	5	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2	–	-1.655	–	-1.630	–	-1.595		–	–	5	–		
		3	–	-1.655	–	-1.630	–	-1.595		5	–	4	–		
		3	–	-1.655	–	-1.630	–	-1.595		–	–	–	4		
Switching Times (50 Ω Load)					Min	Typ Max			Unit	+1.1 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t++	Inputs	1.1	3.8	1.1	2.0 3.7	1.1	4.0	ns	5,7,15	–	Input	Corresponding	8	1,16
	t+-	4, 9 or 14									–	4, 9, or	Ex-OR/Ex-NOR		
	t-+	to either									–	14	Outputs		
	t--	Output									–				
	t++	Inputs				2.8				4,9,14	–	Input	Corresponding		
	t+-	5,7, or 15									–	5, 7, or	Ex-OR/Ex-NOR		
	t-+	to either									–	15	Outputs		
	t--	Output									–				
Rise Time (20 to 80%)	t+	**	1.1	3.5		2.5 3.5		3.8		4,9,14	–	Any Input	Corresponding Ex-OR/Ex NOR Outputs		
Fall Time (20 to 80%)	t-	**	1.1	3.5		2.5 3.5		3.8		4,9,14	–	Any Input			

*Individually test each input applying V_{IH} or V_{IL} to input under test.
**Any Output

MOTOROLA

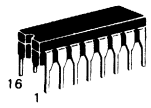
MC10109

DUAL 4-5-INPUT "OR/NOR" GATE

The MC10109 is a dual 4-5 input OR/NOR gate.

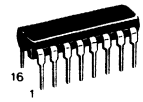
P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

DUAL 4-5-INPUT "OR/NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

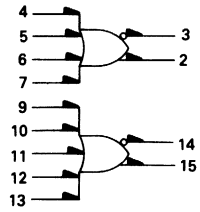
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

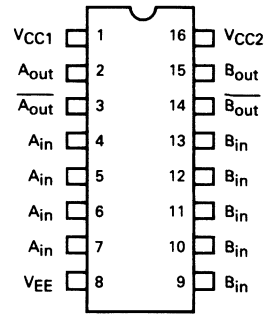
3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10109 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	15	–	11	14	–	15	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	425	–	–	265	–	265	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	0.5	–	0.5	–	–	0.3		μAdc	–	4	–	–	8	1,16
High Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Low Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	4	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	4	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.0	3.7	1.0	2.0	2.9	1.0	3.7	ns	–	–	4	2	8	1,16
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
	t_{4+3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓
Rise Time (20 to 80%)	t_{2+}	2	1.1	4.0	1.1	↓	3.3	1.1	4.0	↓	–	–	↓	2	↓	↓
	t_{3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓
Fall Time (20 to 80%)	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓

MOTOROLA

MC10110

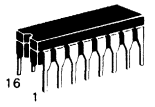
DUAL 3-INPUT 3-OUTPUT "OR" GATE

The MC10110 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR" ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the MC10110 particularly useful in clock distribution applications where minimum clock skew is desired. Three V_{CC} pins are provided and each one should be used.

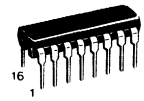
P_D = 80 mW typ/gate (No Load)
t_{pd} = 2.4 ns typ (All Outputs Loaded)
t_r, t_f = 2.2 ns typ (20%–80%)

DUAL 3-INPUT 3-OUTPUT "OR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

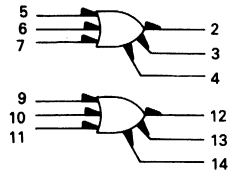
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

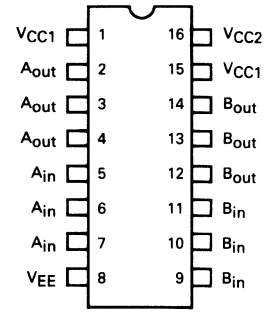
3

LOGIC DIAGRAM



V_{CC1} = Pin 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10110 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	42	–	30	38	–	42	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	680	–	–	425	–	425	μAdc	*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	6	–	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	7	–	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	6	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	7	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2+}	2	1.4	3.5	1.4	2.4	3.5	1.5	3.8	ns	–	–	5	2	8	1,15,16
	t_{5-2-}	2									–	–		2		
	t_{5+3+}	3									–	–		3		
	t_{5-3-}	3									–	–		3		
	t_{5+4+}	4									–	–		4		
	t_{5-4-}	4									–	–		4		
Rise Time (20 to 80%)	t_{2+}	2	1.0		1.1	2.2		1.2			–	–		2		
	t_{3+}	3									–	–		3		
	t_{4+}	4									–	–		4		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		
	t_{4-}	4									–	–		4		

*Individually test each input using the pin connections shown.

MOTOROLA

MC10111

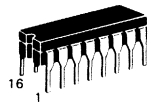
DUAL 3-INPUT 3-OUTPUT "NOR" GATE

The MC10111 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the MC10111 particularly useful in clock distribution applications where minimum clock skew is desired. Three V_{CC} pins are provided and each one should be used.

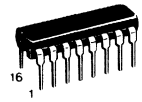
P_D = 80 mW typ/gate (No Load)
t_{pd} = 2.4 ns typ (All Outputs Loaded)
t_r, t_f = 2.2 ns typ (20%–80%)

DUAL 3-INPUT 3-OUTPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

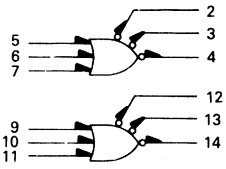
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

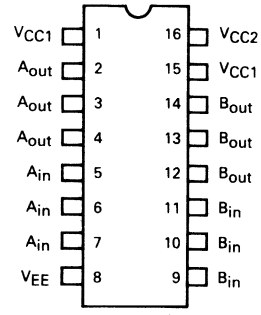
3

LOGIC DIAGRAM



V_{CC1} = Pin 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10111 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	42	–	–	38	–	42	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	680	–	–	425	–	425	μAdc	*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	6	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	5	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	6	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	7	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	6	–	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	7	–	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2-}	2	1.4	3.5	1.4	2.4	3.5	1.5	3.8	ns	–	–	5	2	8	1,15,16
	t_{5-2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
	t_{5+3-}	3									–	–		3		
	t_{5-3+}	3									–	–		3		
	t_{5+4-}	4									–	–		4		
	t_{5-4+}	4									–	–		4		
Rise Time (20 to 80%)	t_{2+}	2	1.0		1.1	2.2	3.5	1.2	3.8		–	–		2		
	t_{3+}	3	↓		↓	↓	↓	↓	↓		–	–		3		
	t_{4+}	4									–	–		4		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		
	t_{4-}	4	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	4	↓	↓

*Individually test each input using the pin connections shown.

MOTOROLA

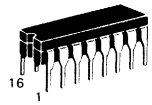
MC10113

QUAD EXCLUSIVE OR GATE

The MC10113 is a quad Exclusive OR gate, with an enable common to all four gates. The outputs may be wire-ORed together to perform a 4-bit comparison function (A = B). The enable is active low.

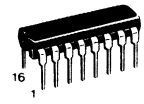
P_D = 175 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
t_r, t_f = 2.0 ns typ (20% to 80%)

QUAD EXCLUSIVE OR GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

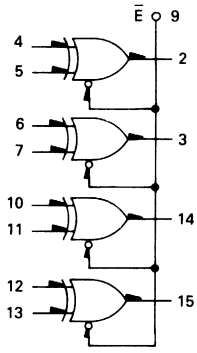
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM



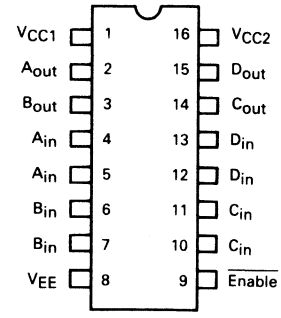
TRUTH TABLE

IN		E	OUTPUT
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
ϕ	ϕ	H	L

ϕ = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10113 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	46	–	42	–	46	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4,7,10,13	–	425	–	265	–	265	μAdc	*	–	–	–	8	1,16
		5,6,11,12	–	350	–	220	–	220	μAdc	*	–	–	–	8	1,16
		9	–	870	–	545	–	545	μAdc	9	–	–	–	8	1,16
	$I_{in\ L}$	*	0.5	–	0.5	–	0.3	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		7	–	–	–		
		14	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		11	–	–	–		
		15	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700		13	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	–	4	–	–	8	1,16
		3	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		–	7	–	–		
		14	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		–	11	–	–		
		15	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615		–	13	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	-0.910	–	Vdc	–	–	4	–	8	1,16
		3	-1.080	–	-0.980	–	-0.910	–		–	–	6	–		
		14	-1.080	–	-0.980	–	-0.910	–		–	–	10	–		
		15	-1.080	–	-0.980	–	-0.910	–		–	–	12	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		3	–	-1.655	–	-1.630	–	-1.595		–	–	–	7		
		14	–	-1.655	–	-1.630	–	-1.595		–	–	–	11		
		15	–	-1.655	–	-1.630	–	-1.595		–	–	–	13		
Switching Times (50 Ω Load)					Min	Typ	Max		Unit	+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.1	4.7	1.3	2.6	4.5	1.3	5.0	ns	–	–	4	2	8	1,16
	t_{4-2-}	2	1.1	4.7	1.3	2.6	4.5	1.3	5.0		–	–	4			
	t_{9+2-}	2	1.3	5.2	1.5	3.4	5.0	1.5	5.5		4	–	9			
	t_{9-2+}	2	1.3	5.2	1.5	3.4	5.0	1.5	5.5		4	–	9			
Rise Time (20 to 80%)	t_{2+}	2	1.1	4.2	1.1	2.5	3.9	1.1	4.4		–	–	4			
Fall Time (20 to 80%)	t_{2-}	2	1.1	4.2	1.1	2.5	3.9	1.1	4.4		–	–	4			

*Individually test each input applying V_{IH} or V_{IL} to input under test.

MOTOROLA

MC10114

TRIPLE LINE RECEIVER

The MC10114 is a triple line receiver designed for use in sensing differential signals over long lines. An active current source and translated emitter follower inputs provide the line receiver with a common mode noise rejection limit of one volt in either the positive or the negative direction. This allows a large amount of common mode noise immunity for extra long lines.

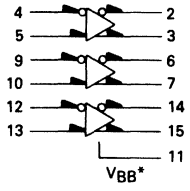
Another feature of the MC10114 is that the OR outputs go to a logic low level whenever the inputs are left floating. The outputs are each capable of driving 50 ohm transmission lines.

This device is useful in high speed central processors, minicomputers, peripheral controllers, digital communication systems, testing and instrumentation systems. The MC10114 can also be used for MOS to MECL interfacing and it is ideal as a sense amplifier for MOS RAM's.

A V_{BB} reference is provided which is useful in making the MC10114 a Schmitt trigger, allowing single-ended driving of the inputs, or other applications where a stable reference voltage is necessary. See MECL Design Handbook (HB205) pages 226 and 228.

P_D = 145 mW typ/pkg
t_{pd} = 2.4 ns typ (Single Ended Input)
t_{pd} = 2.0 ns typ (Differential Input)
t_r, t_f = 2.1 ns typ (20% to 80%)

LOGIC DIAGRAM

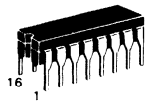


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

*V_{BB} to be used to supply bias to the MC10114 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

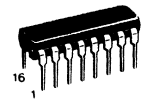
When the input pin with the bubble goes positive, its respective output pin with bubble goes positive.

TRIPLE LINE RECEIVER



L SUFFIX
CERAMIC PACKAGE
CASE 620

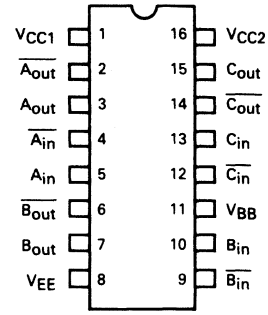
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts)									
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}
−30°C	-0.890	-1.890	-1.205	-1.500	From	+0.110	-0.890	-1.890	-2.890	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	Pin	+0.190	-0.850	-1.810	-2.850	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	11	+0.300	-0.825	-1.700	-2.825	-5.2

Characteristic	Symbol	Pin Under Test	MC10114 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	39	–	28	35	–	39	mAdc	–	4,9,12	–	–	5,10,13	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	70	–	–	45	–	45	μAdc	4	9,12	–	–	5,10,13	–	–	–	–	8	1,16
	I_{CBO}	4	–	1.5	–	–	1.0	–	1.0	μAdc	–	9,12	–	–	5,10,13	–	–	–	–	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	9,12	–	–	5,10,13	–	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9,12	4	–	–	5,10,13	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9,12	4	–	–	5,10,13	–	–	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	9,12	–	–	5,10,13	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9,12	4	–	5,10,13	–	–	–	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9,12	–	–	4	5,10,13	–	–	–	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9,12	–	–	4	5,10,13	–	–	–	–	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9,12	4	–	5,10,13	–	–	–	–	8	1,16
Reference Voltage	V_{BB}	11	-1.420	-1.280	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	–	–	–	5,10,13	–	–	–	–	8	1,16
Common Mode Rejection Test	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	–	4	5	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	–	–	–	5	4	8	1,16
	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	–	–	–	5	4	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	–	4	5	–	–	8	1,16
Switching Times (50-ohm Load)			Min	Max	Min	Typ	Max	Min	Max				Pulse In	Pulse Out						-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.0	4.4	1.0	2.4	4.0	0.9	4.3	ns	–	–	4	2	5,10,13	–	–	–	–	8	1,16
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	–	–	–	–	↓	↓
	t_{4+3-}	3									–	–		3		–	–	–	–		
	t_{4-3+}	3									–	–		3		–	–	–	–		
Rise Time (20% to 80%)	t_{2+}	2	1.5	3.8	1.5	2.1	3.5	1.5	3.7		–	–		2		–	–	–	–		
	t_{3+}	3	↓	↓	↓	↓	↓	↓	↓		–	–		3		–	–	–	–		
Fall Time (20% to 80%)	t_{2-}	2									–	–		2		–	–	–	–		
	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	–	–	–	–	↓	↓

*V_{IHH} — Input logic "1" level shifted positive one volt for common mode rejection tests
V_{ILH} — Input logic "0" level shifted positive one volt for common mode rejection tests
V_{IHL} — Input logic "1" level shifted negative one volt for common mode rejection tests
V_{ILL} — Input logic "0" level shifted negative one volt for common mode rejection tests

MOTOROLA

MC10115

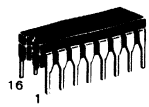
QUAD LINE RECEIVER

The MC10115 is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10115 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 9) to prevent upsetting the current source bias network.

P_D = 110 mW typ/pkg (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

QUAD LINE RECEIVER



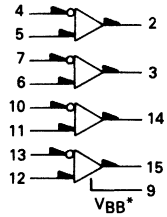
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM

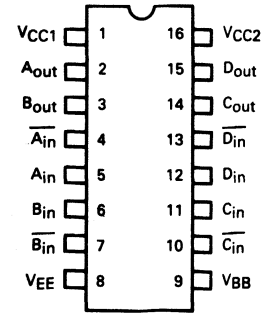


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

*V_{BB} to be used to supply bias to the MC10115 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

When the input pin with the bubble goes positive, the output goes negative.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES					
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}
−30°C	-0.890	-1.890	-1.205	-1.500	From Pin 9	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475		-5.2
+85°C	-0.700	-1.825	-1.035	-1.440		-5.2

Characteristic	Symbol	Pin Under Test	MC10115 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	26	–	29	mAdc	–	4,7,10,13	–	–	5,6,11,12	8	1,16
Input Current	$I_{in\ H}$	4	–	150	–	95	–	95	μAdc	4	7,10,13	–	–	5,6,11,12	8	1,16
	I_{CBO}	4	–	1.5	–	1.0	–	1.0	μAdc	–	7,10,13	–	–	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	7,10,13	4	–	–	5,6,11,12	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	-0.910	–	Vdc	–	7,10,13	–	4	5,6,11,12	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	-1.630	–	-1.595	Vdc	–	7,10,13	4	–	5,6,11,12	8	1,16
Reference Voltage	V_{BB}	9	1.420	1.280	-1.350	-1.230	1.295	-1.150	Vdc	–	–	–	–	5,6,11,12	8	1,16
Switching Times (50 Ω Load)										Pulse In		Pulse Out				-3.2 V	+2.0 V
Propagation Delay	t_{4-2+}	2	1.0	3.1	1.0	2.9	1.0	3.3	ns	4		2		5,6,11,12	8	1,16
	t_{4+2-}	2	1.0	3.1	1.0	2.9	1.0	3.3		↓		↓		↓	↓	↓
Rise Time (20% to 80%)	t_{2+}	2	1.1	3.6	1.1	3.3	1.1	3.7								
Fall Time (20% to 80%)	t_{2-}	2	1.1	3.6	1.1	3.3	1.1	3.7	↓							

MOTOROLA

MC10116

TRIPLE LINE RECEIVER

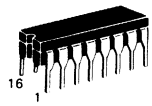
The MC10116 is a triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10116 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

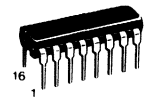
P_D = 85 mW typ/pkg (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

TRIPLE LINE RECEIVER



L SUFFIX
CERAMIC PACKAGE
CASE 620

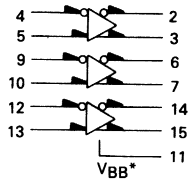
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM

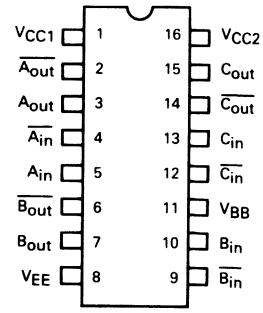


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

*V_{BB} to be used to supply bias to the MC10116 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source <1.0 mA.

When the input pin with the bubble goes positive, the output pin with the bubble goes positive.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	From	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	Pin	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	11	-5.2

Characteristic	Symbol	Pin Under Test	MC10116 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	23	–	17	21	–	23	mAdc	–	4,9,12	–	–	5,10,13	8	1,16
Input Current	I_{inH}	4	–	150	–	–	95	–	95	µAdc	4	9,12	–	–	5,10,13	8	1,16
	I_{CBO}	4	–	1.5	–	–	1.0	–	1.0	µAdc	–	9,12	–	–	5,10,13	8,4	1,16
High Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	9,12	–	–	5,10,13	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9,12	4	–	–	5,10,13	8	1,16
Low Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9,12	4	–	–	5,10,13	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	9,12	–	–	5,10,13	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9,12	4	–	5,10,13	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9,12	–	–	4	5,10,13	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9,12	–	4	5,10,13	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9,12	–	4	–	5,10,13	8	1,16
Reference Voltage	V_{BB}	11	-1.420	-1.280	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	–	–	–	5,10,13	8	1,16
Switching Times (50 Ω Load)			Min	Max	Min	Typ	Max	Min	Max				Pulse In	Pulse Out		-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	4	2	5,10,13	8	1,16
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓	↓
	t_{4+3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓	↓
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓	↓
Rise Time (20% to 80%)	t_{2+}	2	1.1	3.6	1.1	↓	3.3	1.1	3.7	↓	–	–	↓	2	↓	↓	↓
	t_{3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓	↓
Fall Time (20% to 80%)	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓	↓
	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	3	↓	↓	↓

MOTOROLA

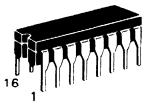
MC10117

DUAL 2-WIDE 2-3-INPUT "OR-AND/OR-AND-INVERT" GATE

The MC10117 is a general purpose logic element designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates.

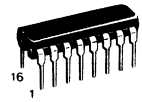
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
t_r, t_f = 2.2 ns typ (20%–80%)

DUAL 2-WIDE 2-3-INPUT "OR-AND/OR-AND-INVERT" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

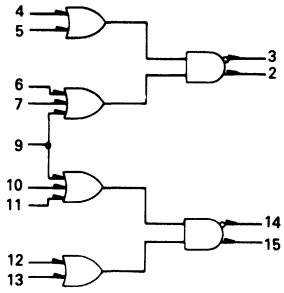
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

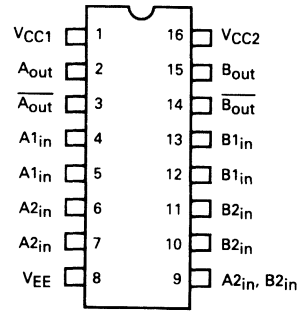
3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10117 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$*	6	–	425	–	–	265	–	265	μAdc	4	–	–	–	8	1,16
		9	–	560	–	–	350	–	350	μAdc	9	–	–	–	8	1,16
		4	–	390	–	–	245	–	245	μAdc	–	4	–	–	8	1,16
	$I_{in\ L}$	4	0.5	–	0.5	–	–	0.3	–	μAdc	–	9	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-.890	-0.960	–	-.810	-0.890	-.700	Vdc	4,9	–	–	–	8	1,16
		3	-1.060	-0.780	-0.960	–	-0.700	-0.890	-0.590	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9	–	4	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	4	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	–	4	–	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	9	–	4	2	8	1,16
	t_{4-2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	2	↓	↓
	t_{4+3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓
Rise Time (20 to 80%)	t_{2+}	2	0.9	4.1	1.1	2.2	4.0	1.1	4.6	↓	↓	–	↓	2	↓	↓
	t_{3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓
Fall Time (20 to 80%)	t_{2-}	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	2	↓	↓
	t_{3-}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓

* Inputs 4, 5, 12 and 13 Have Same $I_{in\ H}$ Limit
Inputs 6, 7, 10 and 11 Have Same $I_{in\ H}$ Limit

MOTOROLA

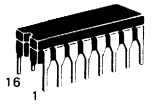
MC10118

DUAL 2-WIDE 3-INPUT "OR-AND" GATE

The MC10118 is a basic logic building block providing the OR/AND function, useful in data control and digital multiplexing applications.

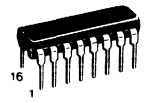
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

DUAL 2-WIDE 3-INPUT "OR-AND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

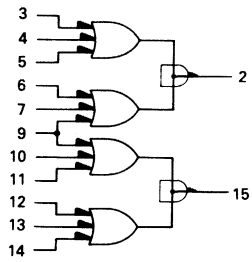
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

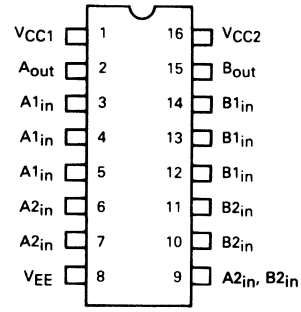
3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10118 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$*	6	–	425	–	–	265	–	265	μAdc	6	–	–	–	8	1,16
		12	–	390	–	–	245	–	245	↓	7	–	–	–	↓	↓
		9	–	560	–	–	350	–	350	↓	9	–	–	–	↓	↓
	$I_{in\ L}$	6	0.5	–	0.5	–	–	0.3	–	μAdc	–	6	–	–	8	1,16
		7	↓	–	↓	–	–	↓	–	↓	–	7	–	–	↓	↓
		9	↓	–	↓	–	–	↓	–	↓	–	9	–	–	↓	↓
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9	–	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	3	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{6+2+}	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	3	–	6	2	8	1,16
	t_{6-2-}	↓	1.4	3.9	1.4	2.3	3.4	1.4	3.8	↓	↓	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_+	↓	0.8	4.1	1.5	2.5	4.0	1.5	4.6	↓	↓	–	↓	↓	↓	↓
Fall Time (20 to 80%)	t_-	↓	0.8	4.1	1.5	2.5	4.0	1.5	4.6	↓	↓	–	↓	↓	↓	↓

* Inputs 3, 4, 5, 12, 13 and 14 Have Same $I_{in\ H}$ Limit
Inputs 6, 7, 10 and 11 have same $I_{in\ H}$ Limit

MOTOROLA

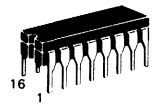
MC10119

4-WIDE 4-3-3-3-INPUT "OR-AND" GATE

The MC10119 is a 4-Wide 4-3-3-3-Input OR/AND gate with one input from two gates common to pin 10.

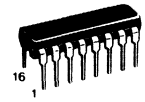
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

4-WIDE 4-3-3-3-INPUT "OR-AND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

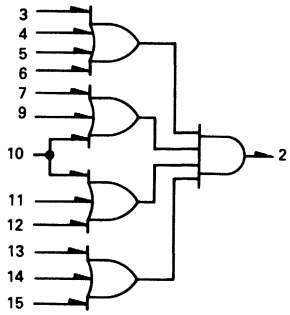
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

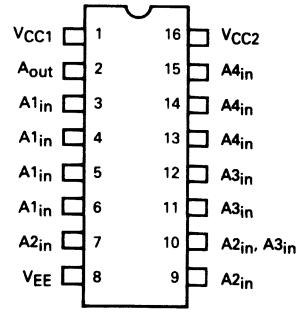
3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10119 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$*	3	–	390	–	–	245	–	245	μAdc	7	–	–	–	8	1,16
		10	–	495	–	–	310	–	310	↓	10	–	–	–	↓	↓
	$I_{in\ L}$	7	0.5	–	0.5	–	–	0.3	–	μAdc	–	7	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,10,15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	10,15	–	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	3	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	1.4	3.9	1.4	2.3	3.4	1.4	3.8	ns	10,13	–	3	2	8	1,16
	t_{3-2-}	↓	1.4	3.9	1.4	2.3	3.4	1.4	3.8	↓	↓	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_+		0.8	4.1	1.5	2.5	4.0	1.5	4.6			–				
Fall Time (20 to 80%)	t_-		0.8	4.1	1.5	2.5	4.0	1.5	4.6			–				

*Inputs 3,4,5,6,7,9,11,12,13,14,15 Have Same $I_{in\ H}$ Limit

MOTOROLA

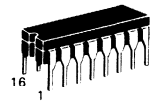
MC10121

4-WIDE "OR-AND/OR-AND-INVERT" GATE

The MC10121 is a basic logic building block providing the simultaneous OR-AND/OR-AND-INVERT function, useful in data control and digital multiplexing applications.

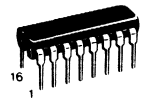
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

4-WIDE "OR-AND/OR-AND-INVERT" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

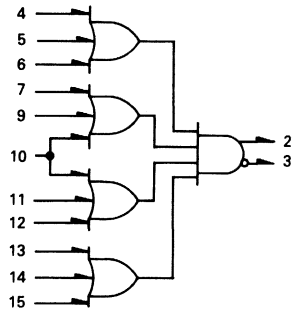
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

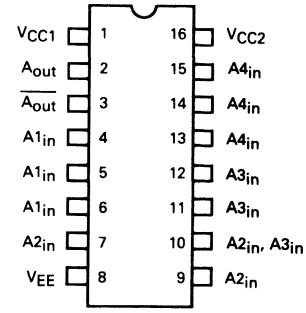
3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10121 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	29	–	20	26	–	29	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	7	–	390	–	–	245	–	245	μAdc	7	–	–	–	8	1,16
		9	–	390	–	–	245	–	245	↓	9	–	–	–	↓	↓
		10	–	495	–	–	310	–	310		10	–	–	–		
	$I_{in\ L}$	7	0.5	–	0.5	–	–	0.3	–	μAdc	–	7	–	–	8	1,16
		9	↓	–	↓	–	–	↓	–	↓	–	9	–	–	↓	↓
		10		–		–	–		–		–	10	–	–		
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,10,13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,10,13	–	–	–	8	1,16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	10,13	–	4	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	–	8	1,16
		2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	10,13	–	–	4	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.4	3.6	1.4	2.3	3.4	1.4	3.5	ns	10,13	–	4	3	8	1,16
	t_{4-3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	3	↓	↓
	t_{4+2+}	2										–		2		
	t_{4-2-}	2										–		2		
Rise Time (20 to 80%)	t_{3+}	3	0.9	4.1	1.1	2.5	4.0	1.1	4.6			–		3		
	t_{2+}	2	↓	↓	↓	↓	↓	↓	↓			–		2		
Fall Time (20 to 80%)	t_{3-}	3										–		3		
	t_{2-}	2										–		2		

*This is advance information and specifications are subject to change without notice.

MOTOROLA

MC10123

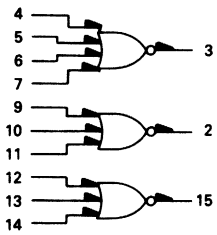
TRIPLE 4-3-3 INPUT BUS DRIVER

The MC10123 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with V_{OL} = −2.1 Vdc so that the bus may be terminated to −2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10123 are "turned-off." This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to −2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10123, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 1.

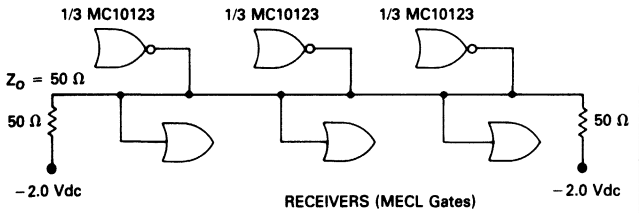
P_D = 310 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

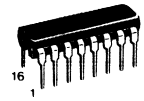
FIGURE 1 — 50-OHM BUS DRIVER (TYPICAL APPLICATION)



TRIPLE 4-3-3 INPUT BUS DRIVER

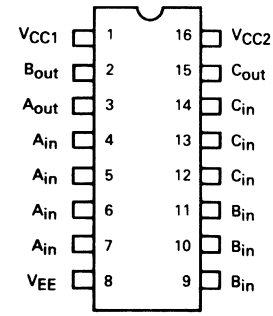
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

3

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 25-ohm resistor to −2.1 volts. Test procedures are shown for only one input an one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10123 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	82	–	71	75	–	82	mAdc	4,5,6,7,9,10 11,12,13,14	–	–	–	8	1,16
Input Current	I_{inH}	4	–	350	–	–	220	–	220	μAdc	4	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	μAdc	–	4			8	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	−2.1	-2.030	−2.1	–	-2.030	−2.1	-2.030	Vdc	4,5,6,7,9,12	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	4,5,6,7	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-2.010	–	–	-2.010	–	-2.010	Vdc	9,12	–	4,5,6,7	–	8	1,16
Switching Times (25-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	1.2	4.6	1.2	3.0	4.4	1.2	4.8	ns	–	–	4	3	8	1,16
	t_{4-3+}	↓	1.2	4.6	1.2	3.0	4.4	1.2	4.8	↓	–	–	↓	↓	↓	↓
Rise Time (20 to 80%)	t_{3+}		1.0	3.7	1.0	2.5	3.5	1.0	3.9		–	–				
Fall Time (20 to 80%)	t_{3-}	↓	1.0	3.7	1.0	2.5	3.5	1.0	3.9	↓	–	–	↓	↓	↓	↓

MOTOROLA

MC10124

QUAD TTL TO MECL TRANSLATOR

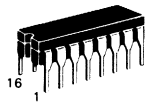
The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10124 has TTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, +5.0 Volts, and −5.2 Volts. Propagation delay of the MC10124 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10115 or MC10116 differential line receivers. The MC10124 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.

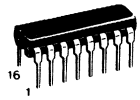
P_D	= 380 mW typ/pkg (No Load)
t_{pd}	= 3.5 ns typ (+ 1.5 Vdc in to 50% out)
t_r, t_f	= 2.5 ns typ (20%–80%)

QUAD TTL TO MECL TRANSLATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

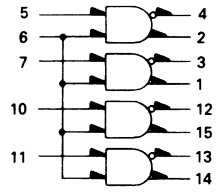
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

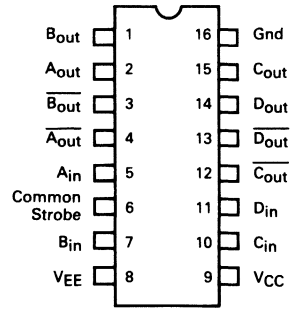
3

LOGIC DIAGRAM



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (−5.2 Vdc) = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

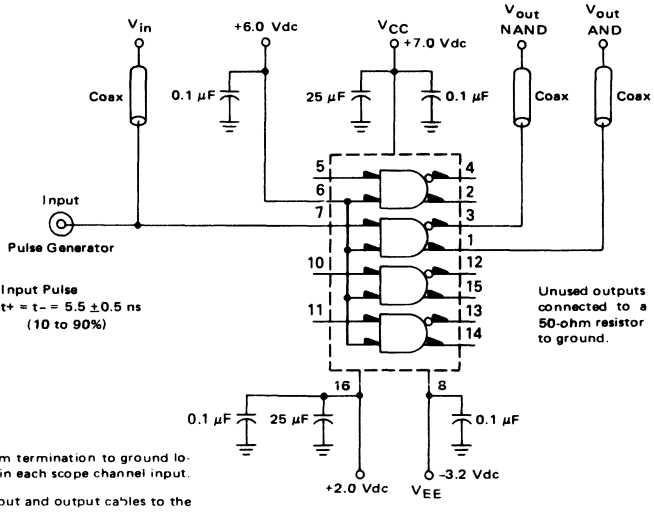
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one translator. The other translators are tested in the same manner.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES									
	Volts								mA	
	V_{IH}	$V_{IL\ max}$	V_{IHA}	V_{ILA}	V_F	V_R	V_{CC}	V_{EE}	I_I	I_{in}
-30°C	+4.0	+0.40	+2.00	+1.10	+0.40	+2.40	+5.00	-5.2	-10	+1.0
+25°C	+4.0	+0.40	+1.80	+1.10	+0.40	+2.40	+5.00	-5.2	-10	+1.0
+85°C	+4.0	+0.40	+1.80	+0.90	+0.40	+2.40	+5.00	-5.2	-10	+1.0

Characteristic	Symbol	Pin Under Test	MC10124 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH}	$V_{IL\ max}$	V_{IHA}	V_{ILA}	V_F	V_R	V_{CC}	V_{EE}	I_I	I_{in}	Gnd
Negative Power Supply Drain Current	I_E	8		72			-66		72	mAdc	–	–	–	–			9	8			16
Positive Power Supply Drain Current	I_{CCH}	9	–	16	–	–	16	–	18	mAdc	5,6,7,10,11	–	–	–	–	–	9	8	–	–	16
	I_{CCL}	9	–	25	–	–	25	–	25	mAdc	–	–	–	–	–	–	9	8	–	–	5,6,7,10,11,16
Reverse Current	I_R	6	–	200	–	–	200	–	200	μAdc	–	–	–	–	5,7,10,11	6	9	8	–	–	16
		7	–	50	–	–	50	–	50	μAdc	–	–	–	–	6	7	9	8	–	–	16
Forward Current	I_F	6	–	-12.8	–	–	-12.8	–	-12.8	mAdc	5,7,10,11	–	–	–	6	–	9	8	–	–	16
		7	–	-3.2	–	–	-3.2	–	-3.2	mAdc	6	–	–	–	7	–	9	8	–	–	16
Input Breakdown Voltage	BV_{in}	6	5.5	–	5.5	–	–	5.5	–	Vdc	–	–	–	–	–	–	9	8	–	6	5,7,10,11,16
		7	5.5	–	5.5	–	–	5.5	–	Vdc	–	–	–	–	–	–	9	8	–	7	6,16
Clamp Input Voltage	V_I	6	–	-1.5	–	–	-1.5	–	-1.5	Vdc	–	–	–	–	–	–	9	8	6	–	16
		7	–	-1.5	–	–	-1.5	–	-1.5	Vdc	–	–	–	–	–	–	9	8	7	–	16
High Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6,7	–	–	–	–	–	9	8	–	–	16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	6,7	–	–	–	–	9	8	–	–	16
Low Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	6,7	–	–	–	–	9	8	–	–	16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	6,7	–	–	–	–	–	9	8	–	–	16
High Threshold Voltage	V_{OHA}	1	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6	–	7	–	–	–	9	8	–	–	16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6	–	–	7	–	–	9	8	–	–	16
Low Threshold Voltage	V_{OLA}	1	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6	–	–	7	–	–	9	8	–	–	16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6	–	7	–	–	–	9	8	–	–	16
Switching Time (50-Ω load)											+6.0 Vdc	Pulse In	Pulse Out				+7.0 Vdc	-3.2 Vdc			+2.0 Vdc
Propagation Delay (+3.5 Vdc to 50%)①	t_{6+1+}	1	1.5	6.8	1.0	3.5	6.0	1.0	6.0	ns	7	6	1	–	–	–	9	8	–	–	16
	t_{6-1-}	↓	1.0	6.0	↓	↓	↓	1.5	6.8		7	6	↓	–	–	–	↓	↓	–	–	↓
	t_{7+1+}		1.5	6.8				1.0	6.0		6	7		–	–	–			–	–	
	t_{7-1-}		1.0	6.0				1.5	6.8		↓	↓		–	↓	–			–	–	
	t_{7+3-}	3	1.5	6.8				1.0	6.0					3	–	–			–	–	
	t_{7-3+}	3	1.0	6.0	↓	↓	↓	1.5	6.8		↓	↓	↓	3	↓	↓	↓	↓	–	–	↓
Rise Time (20% to 80%)	t_{1+}	1	1.0	4.2	1.1	2.5	3.9	1.1	4.3		↓	↓	1	–	–	–	↓	↓	–	–	↓
Fall Time (80% to 20%)	t_{1-}	1	↓	↓	1.1	2.5	3.9	↓	↓	↓	↓	↓	1	–	–	–	↓	↓	–	–	↓

① See switching time test circuit. Propagation delay for this circuit is specified from +1.5 Vdc in to the 50% point on the output waveform. The +3.5 Vdc is shown here because all logic and supply levels are shifted 2 volts positive.)

SWITCHING TIME TEST CIRCUIT



Input Pulse
$t_+ = t_- = 5.5 \pm 0.5$ ns
(10 to 90%)

Unused outputs connected to a 50-ohm resistor to ground.

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

NOTE: All power supply and logic levels are shown shifted 2 volts positive.

MOTOROLA

MC10125

QUAD MECL TO TTL TRANSLATOR

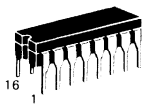
The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on pin 1 for use in single-ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, +5.0 Volts and −5.2 Volts. Propagation delay of the MC10125 is typically 4.5 ns. The MC10125 has fanout of 10 TTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or TTL out. This device has an input common mode noise rejection of ± 1.0 Volt.

An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL logic from the noisy TTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

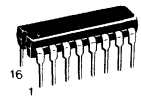
P_D	= 380 mW typ/pkg (No Load)
t_{pd}	= 4.5 ns typ (50% to + 1.5 Vdc out)
t_r, t_f	= 2.5 ns typ (1.0 V to 2.0 V)

QUAD MECL TO TTL TRANSLATOR



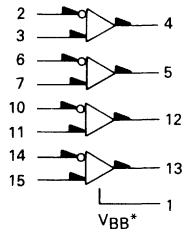
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM

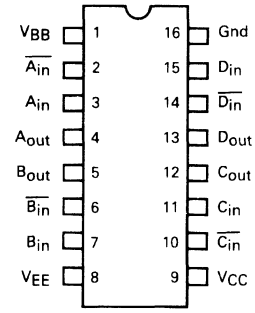


Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (−5.2 Vdc) = Pin 8

*V_{BB} to be used to supply bias to the MC10125 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

When the input pin with the bubble goes positive, the output goes negative.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test procedures are shown for only one translator. The other translators are tested in the same manner.

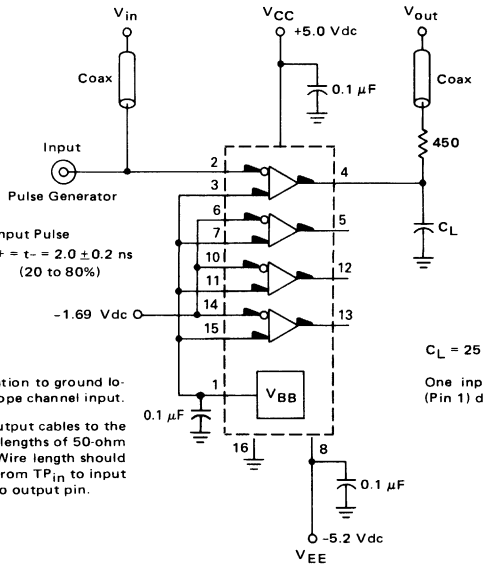
@ Test Temperature	TEST VOLTAGE VALUES (Volts)										
	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	+0.110	-0.890	-1.890	-2.890	From Pin 1	+5.0	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	+0.190	-0.850	-1.810	-2.850		+5.0	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	+0.300	-0.825	-1.700	-2.825		+5.0	-5.2

Characteristic	Symbol	Pin Under Test	MC10125 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}	Gnd	Output Condition
Negative Power Supply Drain Current	I_E	8	–	-44	–	–	-40	–	-44	mAdc	–	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
Positive Power Supply Drain Current	I_{CCH}	9	–	52	–	–	52	–	52	mAdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
	I_{CCL}	9	–	39	–	–	39	–	39	mAdc	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	16	–
Input Current	I_{in} H ①	2	–	180	–	–	115	–	115	μAdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	
Input Leakage Current	I_{CBO}	2	–	1.5	–	–	1.0	–	1.0	μAdc	–	–	–	–	–	–	–	–	3,7,11,15	9	2,6,8,10,14	16	
High Output Voltage	V_{OH}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	16	-2.0 mA
Low Output Voltage	V_{OL}	4	–	0.5	–	–	0.5	–	0.5	Vdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	20 mA
High Threshold Voltage	V_{OHA}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	6,10,14	–	2	–	–	–	–	3,7,11,15	9	8	16	-2.0 mA
Low Threshold Voltage	V_{OLA}	4	–	0.5	–	–	0.5	–	0.5	Vdc	6,10,14	–	2	–	–	–	–	–	3,7,11,15	9	8	16	20 mA
Indeterminate Input Protection Tests	V_{OLS1}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	–	–	–	–	–	9	2,3,6,7,8, 10,11,14,15	16	20 mA
	V_{OLS2}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	–	–	–	–	–	9	8	16	20 mA
Short-Circuit Current	I_{OS}	4	40	100	40	–	100	40	100	mA	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	4,16	
Reference Voltage	V_{BB}	1	-1.420	-1.28	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	–	–	–	
Common Mode Rejection Tests	V_{OH}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	–	–	–	3	2	–	–	–	9	8	16	-2.0 mA
		4	2.5	–	2.5	–	–	2.5	–		–	–	–	–	–	–	3	2	–	9	8	16	-2.0 mA
	V_{OL}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	2	3	–	–	–	9	8	16	20 mA
		4	–	0.5	–	–	0.5	–	0.5		–	–	–	–	–	–	2	3	–	9	8	16	20 mA
Switching Times											Pulse In	Pulse Out	C_L (pF)										
Propagation Delay (50% to +1.5 Vdc)	t_{6+5-}	5	1.0	6.0	1.0	4.5	6.0	1.0	6.0	ns	6	5	25	–	–	–	–	–	3,7,11,15	9	8	16	–
	t_{6-5+}	5	↓	↓	↓	↓	↓	↓	↓		6	5	↓	–	–	–	–	–	↓	↓	↓	↓	–
	t_{2+4-}	4									2	4		–	–	–	–	–					–
	t_{2-4+}	4												–	–	–	–	–					–
Rise Time (+1.0 Vdc to 2.0 Vdc)	t_{4+}	↓	–	3.3	–	–	3.3	–	3.3		↓	↓	↓	–	–	–	–	–	↓	↓	↓	↓	–
Fall Time (+1.0 Vdc to 2.0 Vdc)	t_{4-}	↓	–	3.3	–	–	3.3	–	3.3	↓	↓	↓	↓	–	–	–	–	–	↓	↓	↓	↓	–

① Individually test each input, apply $V_{IH\ max}$ to pin under test.

3

SWITCHING TIME TEST CIRCUIT



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

C_L = 25 pF, including test fixture

One input from each gate must be tied to V_{BB} (Pin 1) during testing.

MOTOROLA

MC10128

BUS DRIVER

The MC10128 is designed to provide outputs which are compatible with IBM-type bus levels; or, if desired, it will drive TTL type loads and/or provide TTL three-state outputs. The inputs accept MECL 10,000 levels. The MC10128 output levels can be accepted by the MC10129 Bus Receiver.

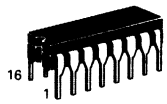
The operating mode IBM or TTL is selected by tying the external control pins to ground or leaving them open. Leaving a control pin open selects the TTL mode, and tying a control pin to ground selects the IBM mode.

The TTL mode will drive a 25-ohm load, terminated to +1.5 Vdc or a 50-ohm load, terminated to ground. The device has totem-pole type outputs, but it also has a disable input for three-state logic operation when the circuit is used in the TTL mode. When in the high state the disable input causes the output to exhibit a high impedance state when it would normally be a positive logic "1" state. When the strobe is in the high state it inhibits the output data in the low state.

Latches are provided on each data input for temporary storage. When the clock input is in the low logic state, information present at the data inputs D1 and D2 will be fed directly to the latch output. When the clock goes high, the input data is latched. The outputs are gated to allow full bus driving and strobing capability.

The MC10128 is useful in interfacing and bus applications in central processors, mini-computers, and peripheral equipment.

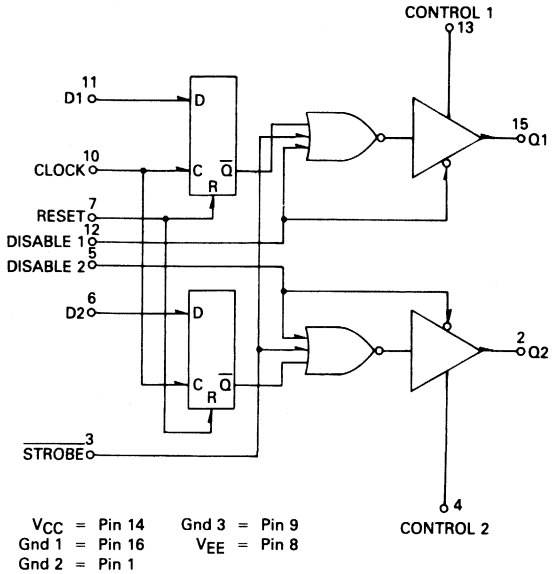
BUS DRIVER



L SUFFIX
CERAMIC PACKAGE
CASE 620

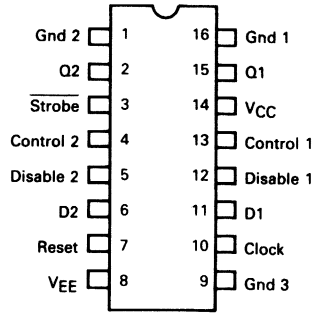
3

LOGIC DIAGRAM



V_{CC} = Pin 14 Gnd 3 = Pin 9
Gnd 1 = Pin 16 V_{EE} = Pin 8
Gnd 2 = Pin 1

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS — TTL MODE

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES: TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	mAdc I_{OH1}	µAdc I_{OH2}	mAdc I_{OL}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	5.00	-50	-100	+56
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	5.00	-50	-100	+56
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	5.00	-50	-100	+56

Characteristic	Symbol	Pin Under Test	MC10128 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	I_{OH1}	I_{OH2}	I_{OL}	Gnd
Negative Power Supply Drain Current	I_E	8	–	100	–	91	–	100	mAdc	6,11	–	–		8	14	–		–	1, 9,16
Positive Power Supply Drain Current	I_{CC}	14	–	50	–	50	–	50	mAdc	6,11	–	–	–	8	14	–		–	1, 9,16
Input Leakage Current	I_{inH}	3	–	490	–	620	–	620	µAdc	3	–	–	–	8	14	–	–	–	1, 9,16
		7	–	560	–	350	–	350		7	–	–	–			–	–	–	
		10	–	425	–	265	–	265		10	–	–	–			–	–	–	
		11	–	425	–	265	–	265		11	–	–	–			–	–	–	
		12	–	775	–	485	–	485		12	–	–	–			–	–	–	
	I_{inL}	All	0.5	–	0.5	–	0.3	–	µAdc	–	*	–	–	8	14	–		–	1, 9,16
Logic "1" Output Voltage	V_{OH}	15	2.5	–	2.5	–	2.5	–	Vdc	11	–	–	–	8	14	2,15	–	–	1, 9,16
		15	2.7	–	2.7	–	2.7	–	Vdc	11	–	–	–	8	14	–	2,15	–	1, 9,16
Logic "0" Output Voltage	V_{OL}	15	–	0.5	–	0.5	–	0.5	Vdc	3	–	–	–	8	14	–	–	2,15	1, 9,16
		2	–	0.5	–	0.5	–	0.5	Vdc	3	–	–	–	8	14	–	–	2,15	1, 9,16
Logic "1" Threshold Voltage	V_{OHA}	15	2.5	–	2.5	–	2.5	–	Vdc	11	7	–	10 ③	8	14	2,15	–	–	1, 9,16
		2	2.5	–	2.5	–	2.5	–	Vdc	6	7	–	10 ③	8	14	2,15	–	–	1, 9,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	0.5	–	0.5	–	0.5	Vdc	11	7,10	3	–	8	14	–	–	2,15	1, 9,16
		2	–	0.5	–	0.5	–	0.5	Vdc	6	7,10	3	–	8	14	–	–	2,15	1, 9,16
Output Short Circuit Current	I_{SC}	15	–	260	–	260	–	260	mAdc	11	–	–	–	8	14	–	–	–	1,2, 9,15,16
		2	–	260	–	260	–	260	mAdc	6	–	–	–	8	14	–	–	–	1,2, 9,15,16
Switching Times † Propagation Delay										-0.890 V	-1.690 V	Pulse In	Pulse Out						
Data Input	t_{11+15+}	15	1.0	17	1.0	18	1.0	24	ns	–	10	11	15	8	14	–	–	–	1, 9 ,16
	t_{11-15-}	15	1.0	17	1.0	18	1.0	24		–	10	11				–	–	–	
Clock Input	t_{10-15+}	15 ①	1.0	20	1.0	20	1.0	25		–	–	10,11				–	–	–	
	t_{10-15-}	15 ②	1.0	20	1.0	20	1.0	25		–	–	10,11				–	–	–	
Reset Input	t_{7+15-}	15 ②	1.0	20	1.0	20	1.0	25		11	–	7,10				–	–	–	
	t_{7+2-}	2 ②	1.0	20	1.0	20	1.0	25		6	–	7,10	2			–	–	–	
STROBE Input	t_{3+15-}	15	1.0	17	1.0	18	1.0	24		11	10	3	15			–	–	–	
	t_{3-15+}	15	1.0	17	1.0	18	1.0	24		–			15			–	–	–	
	t_{3+2-}	2	1.0	17	1.0	18	1.0	24		6			2			–	–	–	
	t_{3-2+}	2	1.0	17	1.0	18	1.0	24		–			2			–	–	–	
Setup Time	t_{setupH}	15	–	–		0.9	–	–		–	–	10,11	15			–	–	–	
	t_{setupL}	15	–	–		0.8	–	–		–	–					–	–	–	
Hold Time	t_{holdH}	15	–	–		1.1	–	–		–	–					–	–	–	
	t_{holdL}	15	–	–		0.8	–	–		–	–					–	–	–	
Rise Time (20% to 80%)	t_{15+}	15	1.0	9.0	1.0	8.0	1.0	9.0		–	10	11				–	–	–	
Fall Time (20% to 80%)	t_{15-}	15	1.0	9.0	1.0	8.0	1.0	9.0		–	10	11				–	–	–	

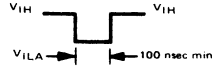
* Apply V_{ILmin} individually to pin under test.

① Output latched to logic Low state prior to test.

② Output latched to logic High state prior to test.

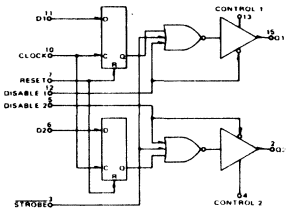
† See waveforms

③ A pulse is applied to pin 10.



ELECTRICAL CHARACTERISTICS — IBM MODE

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.



@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	I_{OH1}	I_{OH2}	I_{OL}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+6.00	-59.3	-30	-230
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+6.00	-59.3	-30	-230
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+6.00	-59.3	-30	230

Characteristic	Symbol	Pin Under Test	MC10128 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	I_{OH1}	I_{OH2}	I_{OL}	Gnd
Negative Power Supply Drain Current	I_E	8	–	107	–	97	–	107	mAdc	6,11	–	–	–	8	14	–	–	–	1,4,9,13,16
Positive Power Supply Drain Current	I_{CC}	14	–	73	–	73	–	73	mAdc	6,11	–	–	–	8	14	–	–	–	1,4,9,13,16
Input Leakage Current	I_{inH}	3	–	990	–	620	–	620	µAdc	3	–	–	–	8	14	–	–	–	1,4,9,13,16
		7	–	560	–	350	–	350		7	–	–	–			–	–	–	
		10	–	425	–	265	–	265		10	–	–	–			–	–	–	
		11	–	425	–	265	–	265		11	–	–	–			–	–	–	
		12	–	775	–	485	–	485		12	–	–	–			–	–	–	
	I_{inL}	All	0.5	–	0.5	–	0.3	–	µAdc	–	*	–	–	8	14	–	–	–	1,4,9,13,16
Logic "1" Output Voltage	V_{OH}	15	3.11	–	3.11	–	3.11	–	Vdc	11	–	–	–	8	14	2,15	–	–	1,4,9,13,16
		15	–	5.85	–	5.85	–	5.85	Vdc	11	–	–	–	8	14	–	2,15	–	1,4,9,13,16
Logic "0" Output Voltage	V_{OL}	15	-0.5	0.15	-0.5	0.15	-0.5	0.15	Vdc	3	–	–	–	8	14	–	–	2,15	1,4,9,13,16
		2	-0.5	0.15	-0.5	0.15	-0.5	0.15	Vdc	3	–	–	–	8	14	–	–	2,15	1,4,9,13,16
Logic "1" Threshold Voltage	V_{OHA}	15	3.11	–	3.11		3.11	–	Vdc	11	7	–	10 ③	8	14	2,15	–	–	1,4,9,13,16
		2	–	–			–	–	Vdc	6	7	–	10 ③	8	14	2,15	–	–	1,4,9,13,16
Logic "0" Threshold Voltage	V_{OLA}	15	-0.5	0.25	-0.5	0.25	-0.5	0.25	Vdc	11	7,10	3	–	8	14	–	–	2,15	1,4,9,13,16
		2	-0.5	0.25	-0.5	0.25	-0.5	0.25	Vdc	6	7,10	3	–	8	14	–	–	2,15	1,4,9,13,16
Output Short Circuit Current	I_{SC}	15	–	320	–	320	–	320	mAdc	11	–	–	–	8	14	–	–	–	1,2,4,9,13,15,16
		2	–	320	–	320	–	320	mAdc	6	–	–	–	8	14	–	–	–	1,2,4,9,13,15,16
Switching Times † Propagation Delay					Min	Max				-0.890 V	-1.690 V	Pulse In	Pulse Out						
Data Input	t_{11+15+}	15	1.0	21	1.0	23.0	1.0	33.0	ns	–	10	11	15	8	14	–	–	–	1,4,9,13,16
	t_{11-15-}	15		21						–	10	11							
Clock Input	t_{10-15+}	15 ①		20							–	10,11				–	–	–	
	t_{10-15-}	15 ②		20						–	–	10,11				–	–	–	
Reset Input	t_{7+15-}	15 ②		20						11	–	7,10				–	–	–	
	t_{7+2-}	2 ②		20						6	–	7,10	2			–	–	–	
$\overline{\text{STROBE}}$ Input	t_{3+15-}	15		21						11	10	3	15						
	t_{3-15+}	15		21						–			15						
	t_{3+2-}	2		21						6			2						
	t_{3-2+}	2		21						–			2						
Setup Time	t_{setupH}	15	–	–	.7	–	–	–		–	–	10,11	15						
	t_{setupL}	15	–	–	.7	–	–	–		–	–								
Hold Time	t_{holdH}	15	–	–	.7	–	–	–		–	–								
	t_{holdL}	15	–	–	.7	–	–	–		–	–								
Rise Time (20% to 80%)	t_{15+}	15	1.0	8.0	1.0	8.0	1.0	9.0		–	10	11							
Fall Time (20% to 80%)	t_{15-}	15	1.0	8.0	1.0	8.0	1.0	9.0		–	10	11							

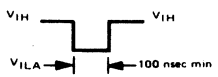
* Apply V_{ILmin} individually to pin under test.

① Output latched to logic Low state prior to test.

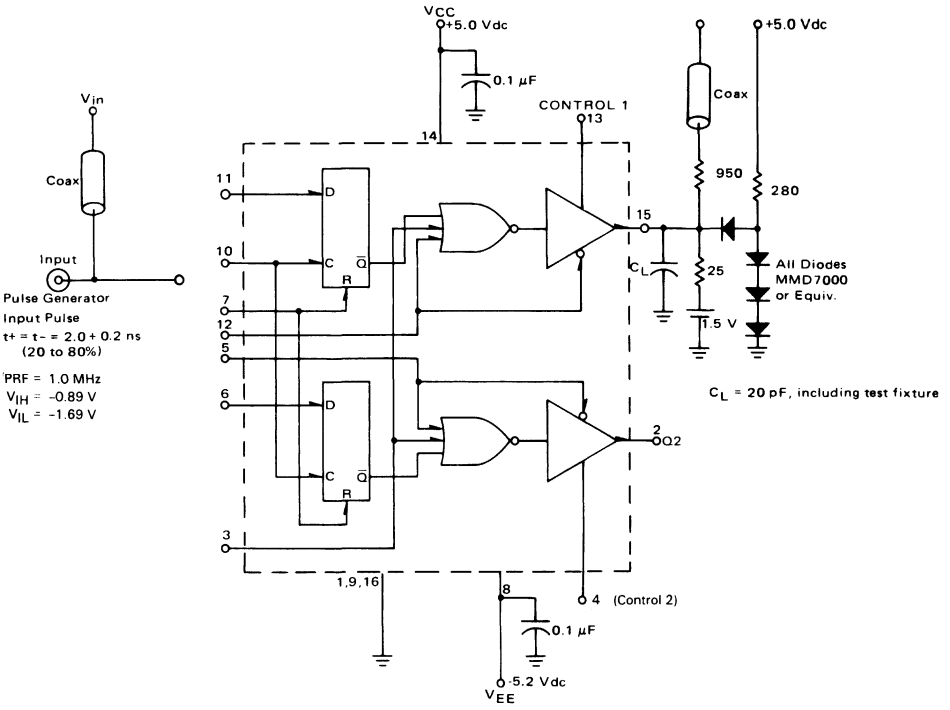
② Output latched to logic High state prior to test.

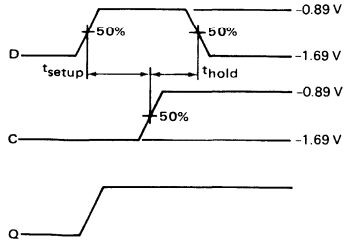
† See waveforms

③ A pulse is applied to pin 10.



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C – TTL MODE

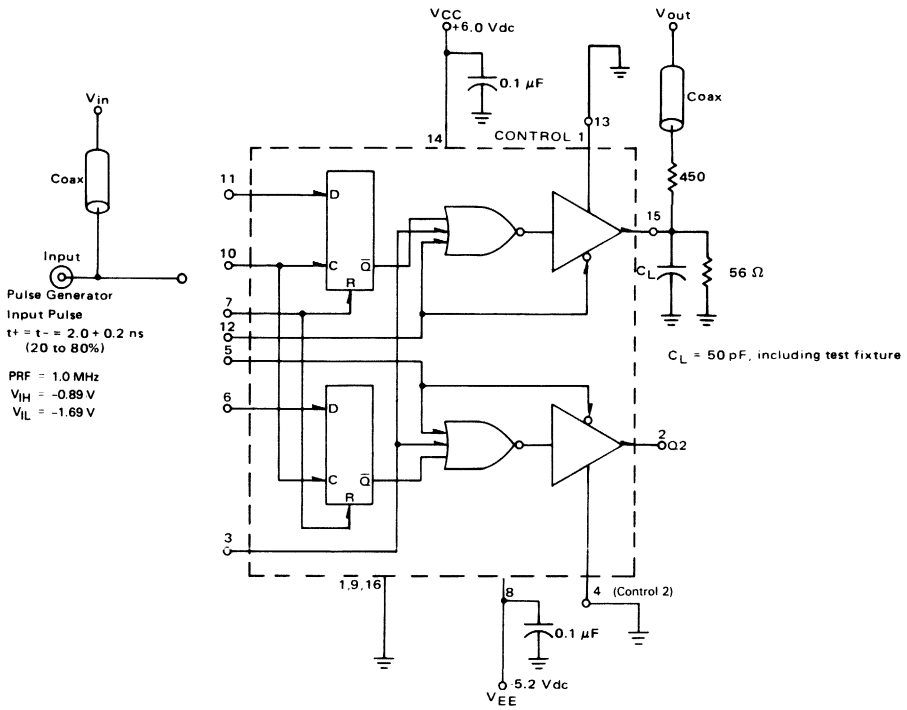


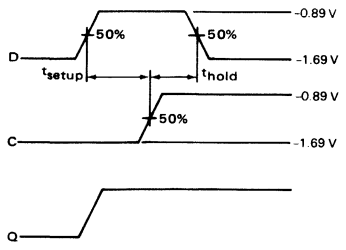


50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C – IBM MODE





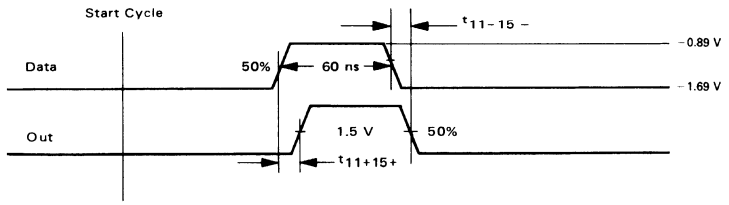
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

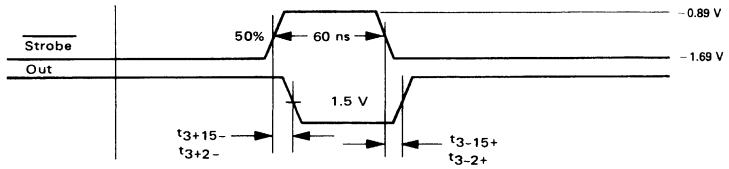
3

VOLTAGE WAVEFORMS

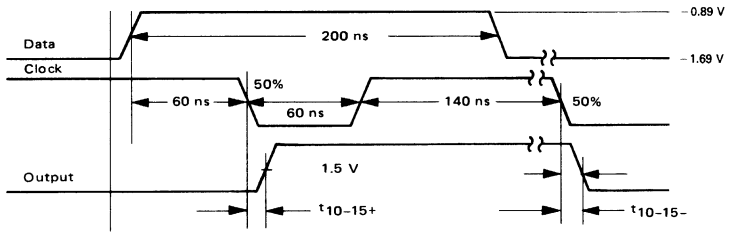
DATA INPUT



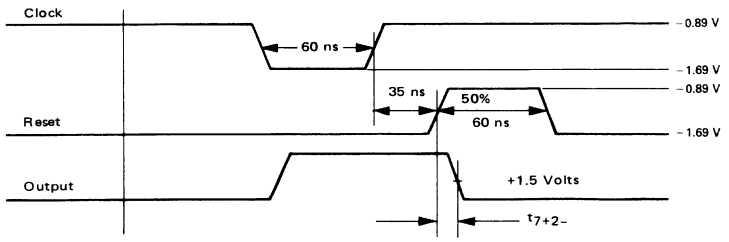
STROBE INPUT



CLOCK INPUT



RESET INPUT



TTL — MODE
V_{OL} = 0.5 Volts Max
V_{OH} = 2.5 Volts Min

IBM — MODE
V_{OL} = 0.25 Volts Max
V_{OH} = 3.11 Volts Min

MOTOROLA

MC10129

QUAD BUS RECEIVER

The MC10129 bus receiver works in conjunction with the MC10128 to allow interfacing of MECL 10,000 to other forms of logic and logic buses. The data inputs are compatible with, and accept TTL logic levels as well as levels compatible with IBM-type buses. The clock, strobe, and reset inputs accept MECL 10,000 logic levels.

The data inputs accept the bus levels, and storage elements are provided to yield temporary latch storage of the information after receiving it from the bus. The outputs can be strobed to allow accurate synchronization of signals and/or connection to MECL 10,000 level buses. When the clock is low, the outputs will follow the D inputs, and the reset input is disabled. The latches will store the data on the rising edge of the clock. The outputs are enabled when the strobe input is high. Unused D inputs must be tied to V_{CC} or Gnd. The clock, strobe, and reset inputs each have 50 k ohm pulldown resistors to V_{EE}. They may be left floating, if not used.

The MC10129 will operate in either of two modes. The first mode is obtained by tying the hysteresis control input to V_{EE}. In this mode, the input threshold points of the D inputs are fixed. The second mode is obtained by tying the hysteresis control input to ground. In this mode, input hysteresis is achieved as shown in the test table. This hysteresis is desirable where extra noise margin is required on the D inputs. The outer input pins are unaffected by the mode of operation used.

The MC10129 is especially useful in interface applications for central processors, mini-computers, and peripheral equipment.

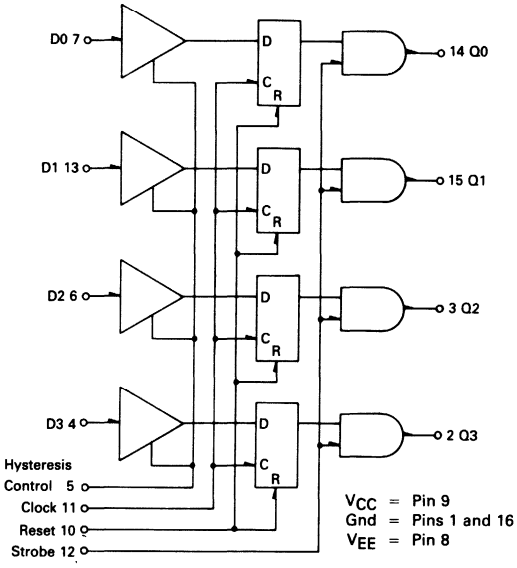
P_D = 750 mW typ/pkg (No Load)
t_{pd} = 10 ns typ
V_{CC} Max = 7.0 Vdc

QUAD BUS RECEIVER

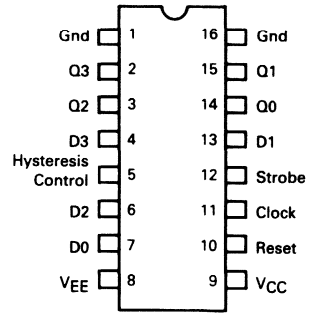
L SUFFIX
CERAMIC PACKAGE
CASE 620

3

LOGIC DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

D	C	STROBE	RESET	Q_{n+1}
ϕ	ϕ	L	ϕ	L
ϕ	H	ϕ	H	L
L	L	H	ϕ	L
ϕ	H	H	L	Q_n
H	L	H	ϕ	H

ϕ = Don't Care

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input/output combination. Other combinations are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC10129 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE VALUES (Volts) — MECL 10,000 INPUT LEVELS @ Test Temperature: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	* TTL INPUT LEVELS: V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	*IBM INPUT LEVELS: V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	HYSTERESIS MODE: $V_{IHA''}$	$V_{ILA''}$	$V_{IHA'''}$	$V_{ILA'''}$	V_{CC} ①	V_{EE}	Gnd
											-30°C: -0.890	-1.890	-1.155	-1.500	3.000	0.400	2.000	0.800	3.11	0.150			2.90	2.00	2.20	1.30	+5.0	-5.2	
											+25°C: -0.810	-1.850	-1.105	-1.475	3.000	0.400	2.000	0.800	3.11	0.150	1.700	0.70	2.600	1.700	1.900	1.000	+5.0	-5.2	
											+85°C: -0.700	-1.825	-1.035	-1.440	3.000	0.400	2.000	0.800	3.11	0.150	–	–	2.30	1.400	1.60	0.70	+5.0	-5.2	
											TEST VOLTAGE APPLIED TO PINS LISTED BELOW:																		
Negative Power Supply Drain Current	I_E	8	–	167	–	–	152	–	167	mAdc	11	12																	9	8	1,5,16
		8	–	189	–	–	172	–	189	mAdc	11	12																	9	5,8	1,16
Positive Power Supply Drain Current	I_{CC}	9	–	8.0	–	–	8.0	–	8.0	mAdc						4,6,7,13				4,6,7,13									9	5,8	1,16
Input Current	I_{inH}	4	–	150	–	–	95	–	95	µAdc					4														9	8	1,16
		6	–	150	–	–	95	–	95						6																
		7	–	150	–	–	95	–	95						7																
		10	–	720	–	–	450	–	450		10,11																				
		11	–	390	–	–	245	–	245		11																				
		12	–	390	–	–	245	–	245		12																				
		13	–	150	–	–	95	–	95						13				13												
	I_{CBO} ⑤	4	–	1.5	–	–	1.0	–	1.0	µAdc						4				4											
		6	–	↓	–	–	↓	–	↓							6				6											
		7	–		–	–		–								7				7											
		13	–		-1.0	–		–								13				13											
	I_{inL}	10	0.5	–	0.5	–	–	0.3	–				10																		
		11	↓	–	↓	–	–	↓	–				11																		
		12											12																		
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	10,11			4	–													9	5,8	1,16
		3	↓	↓	↓	–	↓	↓	↓		↓	↓			6	–													↓	5,8	1,16
		2				–									4	–														8	1,5,16
		3				–									6	–														8	1,5,16
Logic "0" Output Voltage	V_{OL}	2	-1.89	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	12	10,11			–	4			–	4									9	5,8	1,16
		3	↓	↓	↓	–	↓	↓	↓		↓	↓			–	6			–	6									↓	5,8	1,16
		2				–									–	4			–	4										8	1,5,16
		3				–									–	6			–	6										8	1,5,16
Logic "1" Threshold Voltage	V_{OHA}	2 ④	-1.08	–	-0.980	–	–	-0.910	–	Vdc	11,12	–	–	10	4				4										9	5,8	1,16
		2		–		–	–		–		–	10,11	12	–	4				4												
		2		–		–	–		–		10,12	–		11	4				4												
		2		–		–	–		–		12	10,11	–	–			4	–			4	–									
		2 ②		–		–	–		–		↓	↓	–	–				–	–	–		–			4	–	–	–	8	1,5,16	
		2 ③		–		–	–		–				–	–				–	–	–		–							8	1,5,16	
Logic "0" Threshold Voltage	V_{OLA}	2 ④	–	-1.655	–	–	-1.630	–	-1.595	Vdc	11,12	–	10	–	4	–		–	4	–		–							9	5,8	1,16
		2	–		–	–	–	–	–		–	10,11	–	12	4	–		–	4	–		–									
		2 ④	–		–	–	–	–	–		10,12	–	11	–	4	–		–	4	–		–									
		2	–		–	–	–	–	–		12	10,11	–	–		–		4		–		–			4	–	–	–			
		2 ②	–		–	–	–	–	–		↓	↓	–	–		–		–		–		–							8	1,5,16	
		2 ③	–		–	–	–	–	–				–	–		–		–		–		–							8	1,5,16	
Switching Times Propagation Delay Data Input											+1.11 V	+0.31 V	Pulse In	Pulse Out	+5.0 V	+2.40 V	Figure		+5.0 V	+2.40 V	Figure							+7.0 V	-3.2 V	+2.0 V
	t_{7+14+}	14	3.7	15	3.7	10.0	15	3.7	30	ns	12	10,11	7	14	–	–	1		–	–	1		–	–	–	–			9	5,8	1,16
	t_{7-14-}	14	3.7	15	3.7	10.0	15	3.7	40		12	10,11	7	14	–	–	1		–	–	1		–	–	–	–					
Clock Input	t_{11-14+}	14	2.7	11	2.7	5.0	9.0	2.7	11		12	10	7,11	14	–	–	4		–	–	4		–	–	–	–					
	t_{11-14-}	14	2.7	11	2.7	5.0	9.0	2.7	11		12	10	7,11	14	–	–	4		–	–	4		–	–	–	–					
Strobe Input	t_{12+14+}	14	1.6	8.0	1.6	4.0	7.0	1.6	8.0		–	10,11	12	14	7	–	2		7	–	2		–	–	–	–					
	t_{12-14-}	14	1.6	8.0	1.6	4.0	7.0	1.6	8.0		–	10,11	12	14	7	–	2		7	–	2		–	–	–	–					
Reset Input	t_{10+14-}	14	2.0	8.0	2.0	5.0	6.5	2.0	8.0		12	–	10,11	14	7	7	3		7	–	3		–	–	–	–					
Hysteresis Mode	t_{7+14+}	14	6.6	30	6.7	18.0	25	6.6	30		12	10,11	7	14	–	–	1		–	–	1		–	–	–	–			8	1,5,16	
	t_{7-14-}	14	3.7	17	3.7	10.0	15	3.7	40		12	10,11	7	14	–	–	1		–	–	1		–	–	–	–			8	1,5,16	
Setup Time	t_{setup}	14	30	–	2.7	15.0	–	30	–		12	10	7,11	14	–	–	5		–	–	5		–	–	–	–			5,8	1,16	
Hold Time	t_{hold}	14	0	–	-2.0	15.0		-2.0			12	10	7,11	14	–	–	5		–	–	5		–	–	–	–					
Rise Time	t^+	14	1.5	5.0	1.5	2.0	4.3	1.5	5.0		12	10,11	7	14	–	–	1		–	–	1		–	–	–	–					
Fall Time	t^-	14	1.5	5.0	1.5	2.0	4.3	1.5	5.0		12	10,11	7	14	–	–	1		–	–	1		–	–	–	–					

*When testing choose either TTL or IBM Input Levels.

① Operation and limits shown also apply for V_{CC} = +6.0 V.

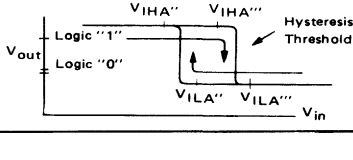
② Input level on data input taken from +0.4 V up to voltage level given.

③ Input level on data input taken from +4.0 V down to voltage level given.

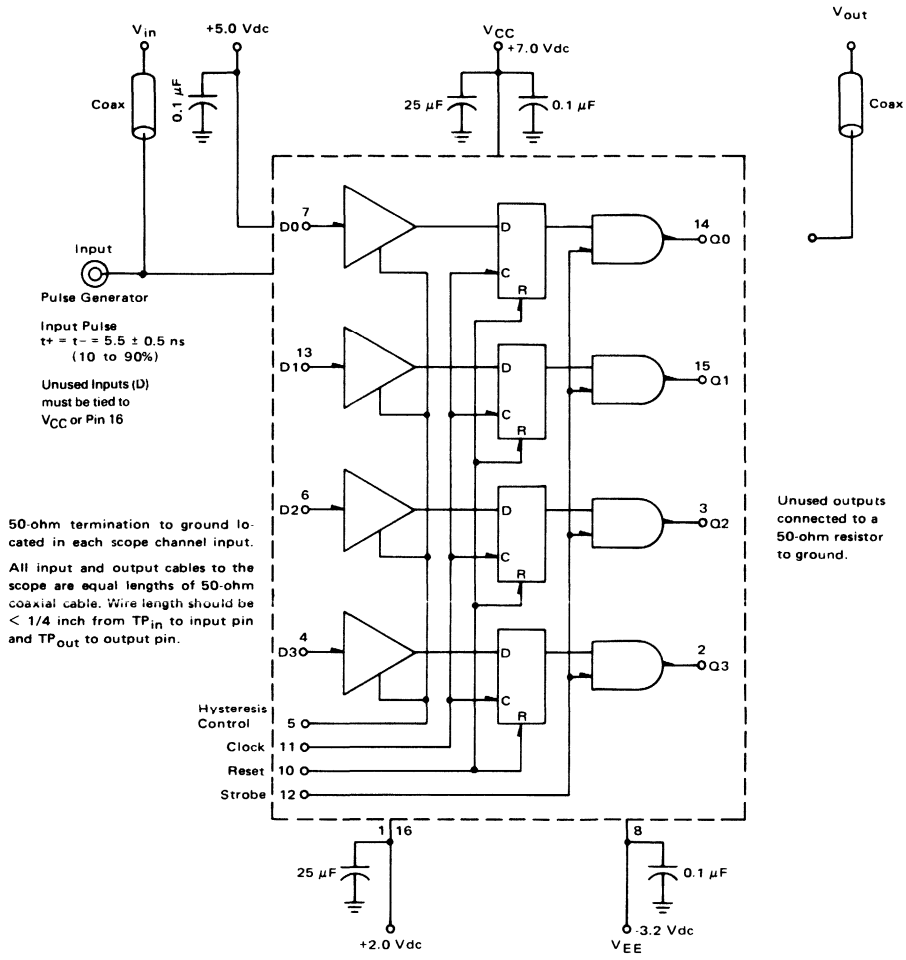
④ Output latched to logic high state prior to test.

$V_{IHA'}$, $V_{ILA'}$ are standard logic "1" and logic "0" MTTL threshold voltages.
$V_{IHA''}$, $V_{ILA''}$, $V_{IHA'''}$ and $V_{ILA'''}$ are logic "1" and logic "0" threshold voltages in the hysteresis mode as shown in diagram.

⑤ Pin 5 to V_{EE}; V_{IL} to Data input one at a time.



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE: All power supplies and logic levels are shifted 2 volts positive.

FIGURE 1 – DATA to OUTPUT
(Clock and Reset are low, Strobe is high)

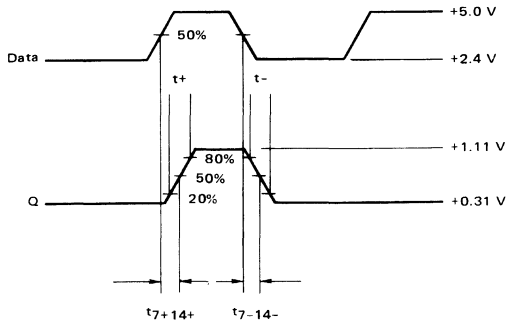


FIGURE 2 – STROBE to OUTPUT
(Data is high, Clock and Reset are low)

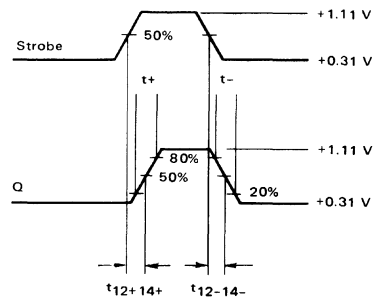


FIGURE 3 – RESET to OUTPUT
(Data and Strobe are high)

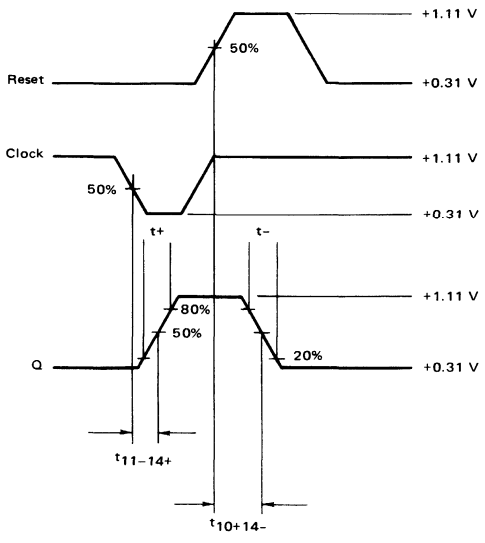


FIGURE 4 – CLOCK to OUTPUT
(Reset is low, Strobe is high)

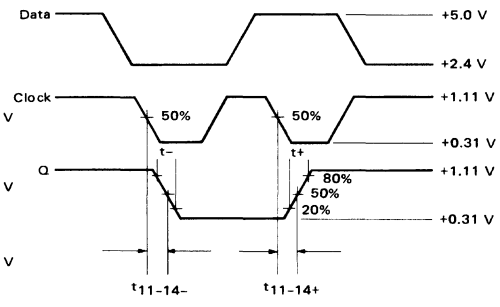
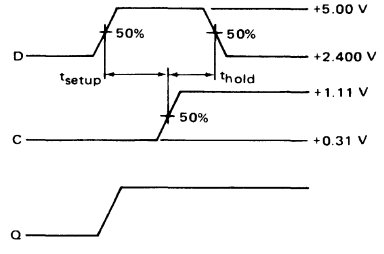


FIGURE 5 – $T_{SET\ UP}$ AND T_{HOLD} WAVEFORMS



MOTOROLA

MC10130

DUAL LATCH

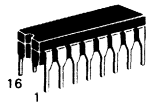
The MC10130 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{C_E}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\overline{C}$).

Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

The set and reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

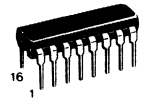
P_D = 155 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
t_r, t_f = 2.7 ns typ (20%–80%)

DUAL LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 620

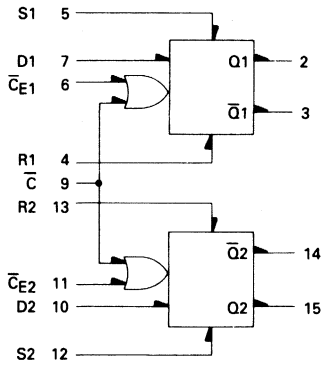
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM



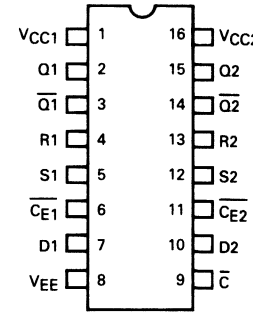
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

D	$\overline{C}$	$\overline{CE}$	Q_{n+1}
L	L	L	L
H	L	L	H
ϕ	L	H	Q_n
ϕ	H	L	Q_n
ϕ	H	H	Q_n

ϕ = Don't Care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one latch. The other latch is tested in the same manner.

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10130 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	38	–	30	35	–	38	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	6,11	–	350	–	–	220	–	220	μAdc	6,11	–	–	–	8	1,16
		9	–	425	–	–	265	–	265	↓	9	–	–	–	↓	↓
		4,5,7	–	–	–	–	–	–	–		4,5	–	–	–		
		10,12,13	–	450	–	–	285	–	285		7,10,12,13	9	–	–		
	I_{inL}	4*	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9	7	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9	–	–	8	1,16
Switching Times (50 Ω Load) (See Figure 1)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+2+}	2	1.0	3.6	1.0	2.5	3.5	1.0	3.8	ns	–	–	7	2	8	1,16
	t_{5+2+}			↓		2.7	↓		3.9		6	–	5	↓	↓	↓
	t_{4+2-}					2.7			3.9		6	–	4			
	t_{6-2+}			4.3	↓	–	4.0	↓	4.1		–	–	6			
Rise Time (20% to 80%)	t_{2+}			3.6	1.1	2.7	3.5	1.1	3.8		–	–	7	↓	↓	
Fall Time (20% to 80%)	t_{2-}	↓	↓	3.6	1.1	2.7	3.5	1.1	3.8	↓	–	–	7			
Setup Time	t_{setup}	2	2.5	–	2.5	–	–	2.5	–	ns	①	–	6,7	2	8	1,16
Hold Time	t_{hold}	2	1.5	–	1.5	–	–	1.5	–	ns	①	–	6,7	2	8	1,16

*All other inputs are tested in the same manner

MOTOROLA

MC10131

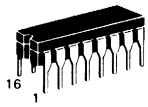
DUAL TYPE D MASTER-SLAVE FLIP-FLOP

The MC10131 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable (C_E) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

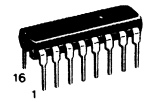
P_D = 235 mW typ/pkg (No Load)
f_{Tog} = 160 MHz typ
t_{pd} = 3.0 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

DUAL TYPE D MASTER-SLAVE FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 620

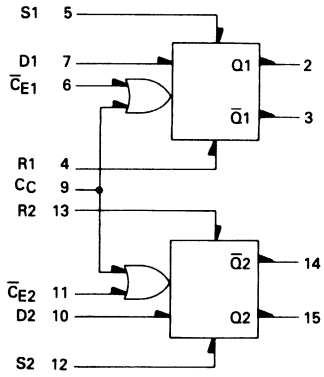
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

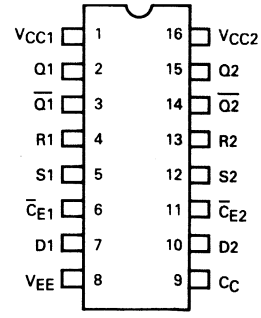
ϕ = Don't Care
C = C_E + C_C.
A clock H is a clock transition from a low to a high state.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

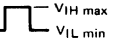
ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10131 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	62	–	45	56	–	62	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	525	–	–	330	–	330	μAdc	4	–	–	–	8	1, 16
		5	–	525	–	–	330	–	330		5	–	–	–		
		6	–	350	–	–	220	–	220		6	–	–	–		
		7	–	390	–	–	245	–	245		7	–	–	–		
		9	–	425	–	–	265	–	265		9	–	–	–		
Input Leakage Current	I_{inL}	4,5,*	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1, 16
		6,7,9*	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	5	–	–	–	8	1, 16
		2†	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	7	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	5	–	–	–	8	1, 16
		3†	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	7	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	5	–	8	1, 16
		2†	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	7	9	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	3	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	5	–	8	1, 16
		3†	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	7	9	8	1, 16
Switching Times Clock Input											+1.11 Vdc		Pulse In	Pulse Out	−3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{9+2-}	2	1.7	4.6	1.8	3.0	4.5	1.8	5.0	ns	–	–	9	2	8	1, 16
	t_{9+2+}	2									7	–	9	2		
	t_{6+2+}	2									7	–	6	2		
	t_{6+2-}	2									–	–	6	2		
Rise Time (20 to 80%)	t_{2+}	2	1.0		1.1	2.5		1.1	4.9		7	–	9	2		
Fall Time (20 to 80%)	t_{2-}	2	1.0		1.1	2.5		1.1	4.9		–	–	9	2		
Set Input Propagation Delay	t_{5+2+}	2	1.7	4.4	1.8	2.8	4.3	1.8	4.8	ns	–	–	5	2	8	1, 16
	t_{12+15+}	15									6	–	12	15		
	t_{5+3-}	3									–	–	5	3		
	t_{12+14-}	14									9	–	12	14		
Reset Input Propagation Delay	t_{4+2-}	2	1.7	4.4	1.8	2.8	4.3	1.8	4.8	ns	–	–	4	2	8	1, 16
	t_{13+15-}	15									6	–	13	15		
	t_{4+3-}	3									–	–	4	3		
	t_{13+14+}	14									9	–	13	14		
Setup Time	t_{setup}	7	2.5	–	2.5	–	–	2.5	–	ns	–	–	6,7	2	8	1, 16
Hold Time	t_{hold}	7	1.5	–	1.5	–	–	1.5	–	ns	–	–	6,7	2	8	1, 16
Toggle Frequency (Max)	f_{Tog}	2	125	–	125	160	–	125	–	MHz	–	–	6	2	8	1, 16

*Individually test each input; apply $V_{IL\ min}$ to pin under test.

†Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ input (pin 6) 

MOTOROLA

MC10132

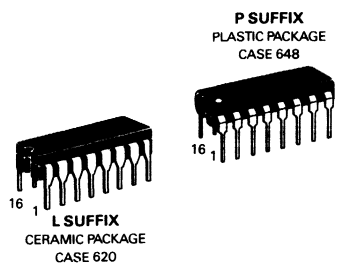
DUAL MULTIPLEXER WITH LATCH AND COMMON RESET

The MC10132 is a dual multiplexer with clocked D type latches. It incorporates common data select and reset inputs. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for a clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

The data select (A) input determines which data input is enabled. A high (H) level enables data inputs D12 and D22 and a low (L) level enables data inputs D11 and D21. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled when the clock is in the high state, and disabled when the clock is low.

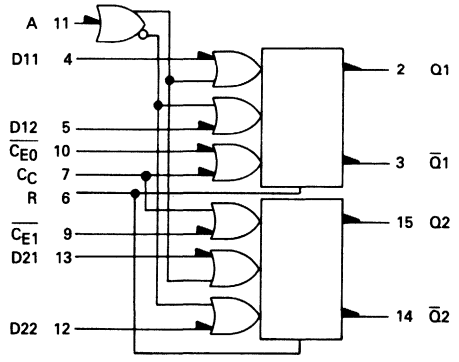
P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

DUAL MULTIPLEXER WITH LATCH AND COMMON RESET



3

LOGIC DIAGRAM



TRUTH TABLE

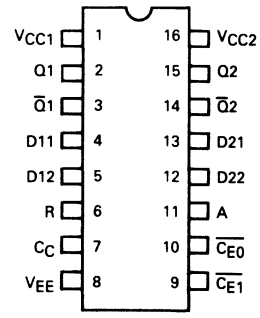
R	D	C_C	$\overline{CE}$	Q_{n+1}
ϕ	L	L	L	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	H	Q_n
ϕ	H	L	L	H
L	H	L	H	Q_n
L	H	H	L	Q_n
L	H	H	H	Q_n
H	ϕ	ϕ	H	L

ϕ = Don't Care

$D = (\overline{A} \bullet D11) + (A \bullet D12)$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one latch. The outer latches are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10132 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Current	I_E	8	–	60	–	44	55	–	60	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	460	–	–	290	–	290	μAdc	4	–	–	–	8	1,16
		5	–	460	–	–	290	–	290		5	–	–	–		
		6	–	620	–	–	390	–	390		6	–	–	–		
		7	–	460	–	–	290	–	290		7	–	–	–		
		10	–	425	–	–	265	–	265		10	–	–	–		
		11	–	425	–	–	265	–	265		11	–	–	–		
	$I_{in\ L}$	4*	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	7,9,10	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5,11	7,9,10	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	7,9,10	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5,11	7,9,10	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	7,9,10	4	–	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	11	7,9,10	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	7,9,10	4	–	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	11	7,9,10	5	–	8	1,16
Switching Times (50-ohm load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data	t_{4+2+}	2	1.0	3.6	1.0	–	3.3	1.0	3.7	ns	–	7,9,10	4	2	8	1,16
Reset	t_{6+2-}			4.0	1.0	–	3.8		4.2		7	–	6			
Clock	t_{7-2+}			6.0	1.0	–	5.7		6.3		4	–	7			
Select	t_{11+2+}			4.8	1.0	–	4.6		5.0		5	7	11			
Setup Time Data	t_{setup}	2	2.5	–	2.5	–	–	2.5	–	ns	–	11	4,10	2	8	1,16
Select	t_{setup}	2	3.5	–	3.5	–	–	3.5	–	ns	5	7	10,11	2	8	1,16
Hold Time Data	t_{hold}	2	1.5	–	1.5	–	–	1.5	–	ns	–	11	4,10	2	8	1,16
Select	t_{hold}	2	1.0	–	1.0	–	–	1.0	–	ns	5	7	10,11	2	8	1,16
Rise Time (20% to 80%)	t_{2+}	2	1.5	3.7	1.5	–	3.5	1.5	3.8	ns	–	7,9,10	4	2	8	1,16
Fall Time (20% to 80%)	t_{2-}	2	1.5	3.7	1.5	–	3.5	1.5	3.8	ns	–	7,9,10	4	2	8	1,16

* All other inputs tested in the same manner.

MOTOROLA

MC10133

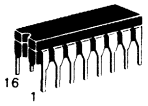
QUAD LATCH

The MC10133 is a high speed, low power, quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs, allowing direct wiring to a bus. When the clock is high, outputs will follow D inputs. Information is latched on the negative going transition of the clock.

The outputs are gated when the output enable ($\overline{G}$) is low. All four latches may be clocked at one time with the common clock (C_C), or each half may be clocked separately with its clock enable ($\overline{CE}$).

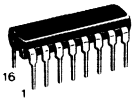
P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

QUAD LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 620

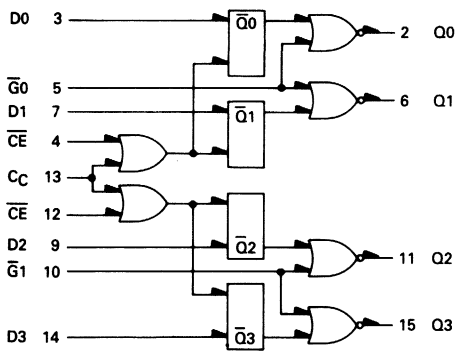
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM



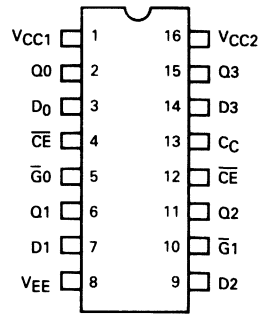
TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H

ϕ = Don't Care
C = C_C + CE

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10133 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	82	–	–	75	–	82	mAdc	–	13	–	–	8	1,16
Input Current	I_{inH}	3	–	390	–	–	245	–	245	µAdc	3	–	–	–	8	1,16
		4	–	425	–	–	265	–	265		4	–	–	–		
		5	–	560	–	–	350	–	350		5	–	–	–		
		13	–	560	–	–	350	–	350		13	–	–	–		
	I_{inL}	3	0.5	–	0.5	–	–	0.3	–	µAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,4	–	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	13	3	–	–	8	1,16
		2				–					3,5,13	–	–	–		
		2				–					4	3	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	3,4	–	–	5	8	1,16
		2		–		–	–		–		4	–	3	–		
		2		–		–	–		–		3,4	–	–	–		
		2†		–		–	–		–		3	–	–	–		
		2††		–		–	–		–		–	–	–	–		
		2††		–		–	–		–		–	–	–	4		
		2		–		–	–		–		3	–	4	–		
		2		–		–	–		–		3	–	13	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	3,4	–	5	–	8	1,16
		2	–		–	–		–			4	–	–	3		
		2	–		–	–		–			4	–	–	–		
		2†	–		–	–		–			–	–	–	–		
		2††	–		–	–		–			3	–	–	–		
		2††	–		–	–		–			3	–	–	13		
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	1.0	5.6	1.0	4.0	5.4	1.1	5.9	ns	4	–	3	2	8	1,16
	t_{4+2+}	2		5.4		4.0	5.4	1.2	6.0		3 *	–	4	2		
	t_{5-2+}	2		3.2		2.0	3.1	1.0	3.4		–	–	5	2		
	t_{Setup}	3	2.5	–	2.5	0.7	–	2.5	–		–	–	3	2		
	t_{Hold}	3	1.5	–	1.5	0.7	–	1.5	–		–	–	3	2		
Rise Time (20% to 80%)	t_{2+}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8		4	–	3	2		
Fall Time (20% to 80%)	t_{2-}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8		4	–	3	2		

†Output level to be measured after a clock pulse has been applied to the clock input (Pin 4).

††Data input at proper high/low level while clock pulse is high so that device latches at proper high/low level for test. Levels are measured after device has latched.

V_{IH} max
V_{IL} min

*Latch set to zero state before test.

MOTOROLA

MC10134

DUAL MULTIPLEXER WITH LATCH

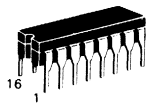
The MC10134 is a dual multiplexer with clocked D type latches. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

The data select inputs determine which data input is enabled. A high (H) level on the A0 input enables data input D12 and a low (L) level on the A0 input enables data input D11. A high (H) level on the A1 input enables data input D22 and a low (L) level on the A1 input enables data input D21.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

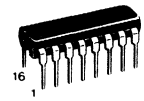
P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

DUAL MULTIPLEXER WITH LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 620

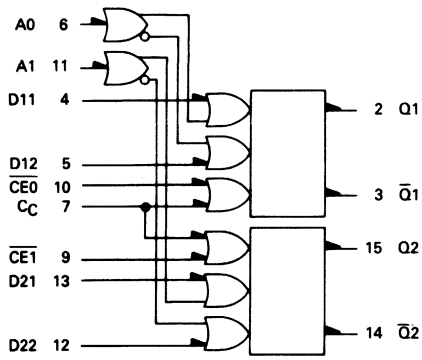
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM



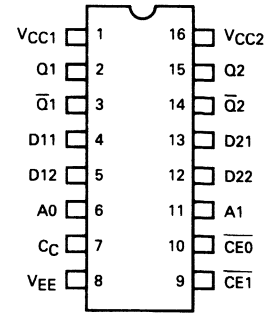
TRUTH TABLE

C	A0	D11	D12	Q_{n+1}
L	L	L	ϕ	L
L	L	H	ϕ	H
L	H	ϕ	L	L
L	H	ϕ	H	H
H	ϕ	ϕ	ϕ	Q_n

ϕ = Don't Care
$C = \overline{CE} + C_C$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one latch. The other latches are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.625	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10134 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	60	–	55	–	60	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	460	–	290	–	290	μAdc	4	–	–	–	8	1,16
		5	–	460	–	290	–	290		5	–	–	–		
		6	–	425	–	265	–	265		6	–	–	–		
		7	–	460	–	290	–	290		7	–	–	–		
		10	–	425	–	265	–	265		10	–	–	–		
	$I_{in\ L}$	4*	0.5	–	0.5	–	0.3	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	4	6,7,10,	–	–	8	1,16
		2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	5,6	7,10	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	–	4,6,7,10,	–	–	8	1,16
		2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	6	5,7,10	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	-0.910	–	Vdc	–	6,7,10	4	–	8	1,16
		2	-1.080	–	-0.980	–	-0.910	–	Vdc	6	7,10	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	-1.630	–	-1.595	Vdc	–	6,7,10	–	4	8	1,16
		2	–	-1.655	–	-1.630	–	-1.595	Vdc	6	7,10	–	5	8	1,16
Switching Times (50-ohm load)										+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data	t_{4+2+}	2	1.0	3.5	1.0	3.3	1.0	3.6	ns	–	6,7,10	4	2	8	1,16
Clock	t_{10-2+}		1.0	6.0	1.0	5.7	1.0	6.3		4	7	10			
Select	t_{6+2+}		1.0	4.8	1.0	4.6	1.0	5.0		5	7,10	6			
Setup Time Data	t_{setup}	2	2.5	–	2.5	–	2.5	–	ns	–	6,7	4,10	2	8	1,16
Select	t_{setup}	2	3.5	–	3.5	–	3.5	–	ns	5	7,11	6,10	2	8	1,16
Hold Time Data	t_{hold}	2	1.5	–	1.5	–	1.5	–	ns	–	6,7	4,10	2	8	1,16
Select	t_{hold}	2	1.0	–	1.0	–	1.0	–	ns	5	7,11	6,10	2	8	1,16
Rise Time (20% to 80%)	t_{2+}	2	1.5	3.7	1.5	3.5	1.5	3.8	ns	–	6,7,10	4	2	8	1,16
Fall Time (20% to 80%)	t_{2-}	2	1.5	3.7	1.5	3.5	1.5	3.8	ns		6,7,10	4	2	8	1,16

*All other inputs tested in the same manner.

MOTOROLA

MC10135

DUAL J-K MASTER-SLAVE FLIP-FLOP

The MC10135 is a dual master-slave dc coupled J-K flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs override the clock.

A common clock is provided with separate $\overline{J}$-$\overline{K}$ inputs. When the clock is static, the $\overline{J}$-$\overline{K}$ inputs do not effect the output.

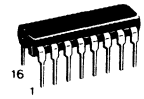
The output states of the flip-flop change on the positive transition of the clock.

P_D = 280 mW typ/pkg (No Load)
f_{Tog} = 140 MHz typ
t_{pd} = 3.0 ns typ
t_r, t_f = 2.5 ns typ (20%–80%)

DUAL J-K MASTER-SLAVE FLIP-FLOP

L SUFFIX
CERAMIC PACKAGE
CASE 620

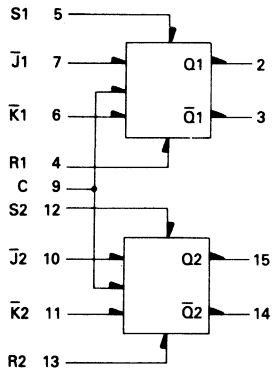
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

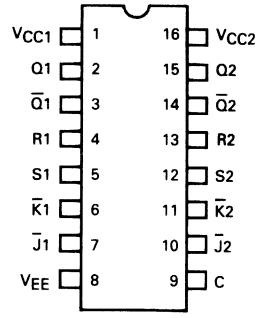
N.D. = Not Defined

CLOCK J-K TRUTH TABLE*

$\overline{J}$	$\overline{K}$	Q_{n+1}
L	L	$\overline{Q_n}$
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transition of clock for $\overline{J}$-$\overline{K}$ input condition present.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10135 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	75	–	54	68	–	75	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	6,7,9,10,11	–	425	–	–	265	–	265	μAdc	①	–	–	–	8	1,16
		4,5,12,13	–	620	–	–	390	–	390	μAdc	①	–	–	–	8	1,16
Input Leakage Current	$I_{in\ L}$	4,5,6,7,9,	0.5	–	0.5	–	–	0.3	–	μAdc	–	②	–	–	8	1,16
		10,11,12,13	0.5	–	0.5	–	–	0.3	–	μAdc	–	②	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
		2 ③	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,16
		3 ③	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	6	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		2 ④	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6	–	–	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,16
		3 ④	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6	–	–	–	8	1,16
Switching Times													Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input Propagation Delay	t_{9+2+}	2	1.8	5.0	1.8	3.0	4.5	1.8	4.6	ns	–	–	9	2	8	1,16
	t_{9+2-}	2	1.8	5.0	1.8	3.0	↓	1.8	4.6	↓	–	–	9	2	↓	↓
Rise Time (20 to 80%)	$t_{2+,3+}$	2,3	1.1	4.8	1.1	2.0	↓	1.1	4.7	↓	–	–	9	2,3	↓	↓
Fall Time (20 to 80%)	$t_{2-,3-}$	2,3	1.1	4.8	1.1	2.0	↓	1.1	4.7	↓	–	–	9	2,3	↓	↓
Set Input Propagation Delay	t_{5+2+}	2	1.8	5.6	1.8	3.0	5.0	1.8	5.2	ns	–	–	5	2	8	1,16
	t_{12+15+}	15	↓	↓	↓	↓	↓	–	↓	↓	–	–	12	15	↓	↓
	t_{5+3-}	3						–			–	–	5	3		
	t_{12+14-}	14						–			–	–	12	14		
Reset Input Propagation Delay	t_{4+2-}	2	1.8	5.6	1.8	3.0	5.0	1.8	5.2	ns	–	–	4	2	8	1,16
	t_{4+3+}	3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	4	3	↓	↓
	t_{13+15-}	15									–	–	13	15		
	t_{13+14+}	14									–	–	13	14		
Setup Time	t_{setup}	7	2.5	–	2.5	1.0	–	2.5	–	ns	–	–	6,9 ⑤	2	8	1,16
Hold Time	t_{hold}	7	1.5	–	1.5	1.0	–	1.5	–	ns	–	–	6,9 ⑤	2	8	1,16
Toggle Frequency	f_{Tog}	2	125	–	125	140	–	125	–	MHz	–	–	9	2	9	1,16

NOTES:

① Individually test each input; apply $V_{IH\ max}$ to pin under test.

② Individually test each input; apply $V_{IL\ min}$ to pin under test.

③ Output level to be measured after a clock pulse has been applied to the C input (pin 9)

④ Output level to be measured after a clock pulse has been applied to the C input (pin 9)

⑤ See Figure 2 for timing test diagram.

MOTOROLA

MC10136

UNIVERSAL HEXADECIMAL COUNTER

The MC10136 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous count feature makes the MC10136 suitable for either computers or instrumentation.

Three control lines (S1, S2, and Carry In) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count, or when the counter is being preset.

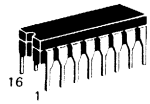
This device is not designed for use with gated clocks. Control is via S1 and S2.

P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ
t_{pd} = 3.3 ns typ (C-Q)
7.0 ns typ (C-C_{out})
5.0 ns typ (C_{in}-C_{out})

FUNCTION TABLE

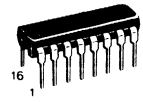
C_{in}	S1	S2	Operating Mode
ϕ	L	L	Preset (Program)
L	L	H	Increment (Count Up)
H	L	H	Hold Count
L	H	L	Decrement (Count Down)
H	H	L	Hold Count
ϕ	H	H	Hold (Stop Count)

UNIVERSAL HEXADECIMAL COUNTER



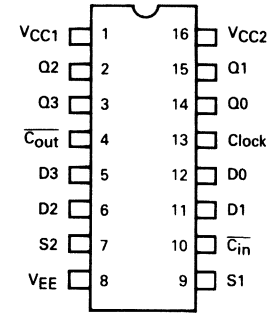
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

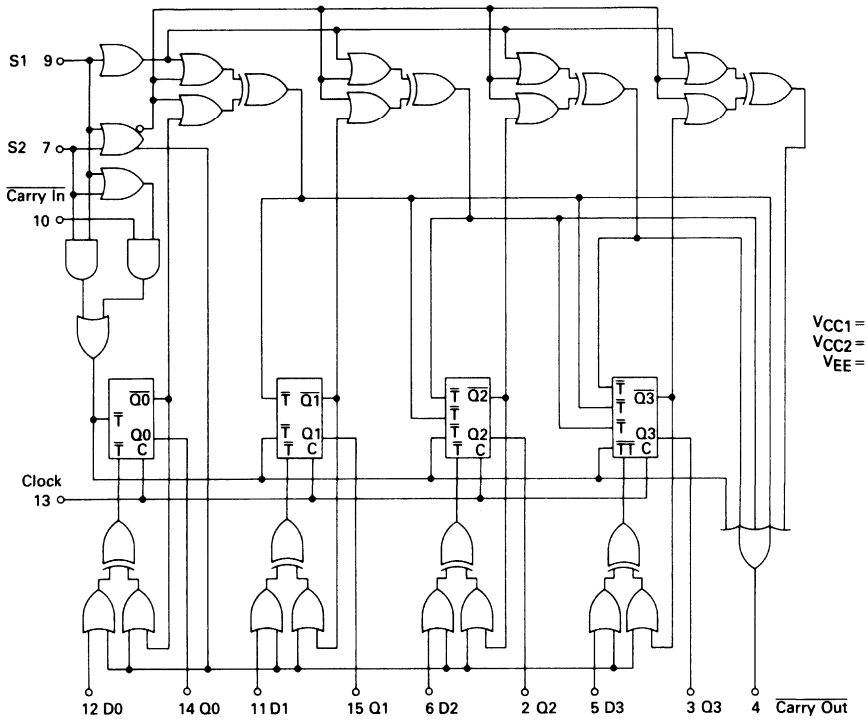
DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

3

LOGIC DIAGRAM



NOTE: Flip-flops will toggle when all $\overline{T}$ inputs are low.

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	L	L	H	H	ϕ	H	L	L	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H
H	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H
L	L	H	H	L	L	ϕ	H	H	H	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	H

ϕ = Don't care.
* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
** A clock H is defined as a clock input transition from a low to a high logic level.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test procedures are shown for only one output. The other outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic		Symbol	Pin Under Test	MC10136 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current		I_E	8		138		100	125		138	mAdc					8	1, 16
Input Current		$I_{in\ H}$	5,6,11,12		350			220		220	μAdc	5,6,11,12				8	1, 16
			7		425			265		265		7					
			9,10		390			245		245		9,10					
			13		460			290		290		13					
		$I_{in\ L}$	All	0.5		0.5			0.3		μAdc		①			8	1, 16
Logic "1" Output Voltage		V_{OH}	14 ②	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	12	7, 9			8	1, 16
Logic "0" Output Voltage	10136	V_{OL}	14 ②	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc		7, 9			8	1, 16
				—	—	—	—	—	—	—							
Logic "1" Threshold Voltage		V_{OHA}	14 ②	-1.080		-0.980			-0.910		Vdc		7, 9	12		8	1, 16
Logic "0" Threshold Voltage		V_{OLA}	14 ②		-1.655			-1.630		-1.595	Vdc		7, 9		12	8	1, 16
Switching Times (50-ohm Load)												+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay																	
Clock Input		t_{13+14+}	14	0.8	4.8	1.0	3.3	4.5	1.4	5.0	ns	12		13	14	8	1, 16
		t_{13+14-}	14	0.8	4.8	1.0	3.3	4.5	1.4	5.0					14		
		t_{13+4+}	4	2.0	10.9	2.5	7.0	10.5	2.4	11.5		7			4		
		t_{13+4-}	4	2.0	10.9	2.5	7.0	10.5	2.4	11.5		7			4		
$\overline{\text{Carry In}}$ To $\overline{\text{Carry Out}}$		t_{10-4-}	4 ③	1.6	7.4	1.6	5.0	6.9	1.9	7.5		7	13	10	4		
		t_{10+4+}	4	1.6	7.4	1.6	5.0	6.9	1.9	7.5		7	13	10	4		
Set Up Time																	
Data Inputs		t_{12+13+}	14	3.5		3.5			3.5				7.9	12, 13	14		
		t_{12-13+}	14	3.5		3.5			3.5				7.9	12, 13			
Select Inputs		t_{9+13+}	14	6.0		6.0			6.0					9, 13			
		t_{7+13+}	14	6.0		6.0			6.0					7, 13			
$\overline{\text{Carry In}}$ Input		t_{10-13+}	14	2.5		2.5			3.0			7	9	10, 13	14		
		t_{10+13-}	14	1.5		1.5			1.5	—		7	9	10, 13	14		
Hold Time																	
Data Inputs		t_{13+12+}	14	0		0			0				7, 9	12, 13	14		
		t_{13+12-}	14	0		0			0				7, 9	12, 13			
Select Inputs		t_{13+9+}	14	-1		-1.0			-1				—	9, 13			
		t_{13+7+}	14	-1		-1.0			-1				—	7, 13			
$\overline{\text{Carry In}}$ Input		t_{13+10-}	14	0		0			0			7	9	10, 13			
		t_{13-10+}	14	0		0			0			7	—	10, 13			
Counting Frequency		$f_{countup}$	14	125		125	150		125		MHz	7		13			
		$f_{countdown}$	14	125		125	150		125		MHz	9			4		
Rise Time (20% to 80%)		t_{4+}	4	0.9	3.3	1.1	2.0	3.3	1.1	3.5	ns	7			4		
		t_{14+}	14				2.0								14		
Fall Time (20% to 80%)		t_{4-}	4				2.0								4		
		t_{14-}	14				2.0								14		

① Individually apply $V_{IL\ min}$ to pin under test.

② Measure output after clock pulse V_{IL} ⌐ V_{IH} appears at clock input (pin 13)

③ Before test set all Q outputs to a logic high.

To preserve reliable performance, the MC10136 (plastic-packaged device only) is to be operated in ambient temperatures above 70°C only when 500 lfpm blown air or equivalent heat sinking is provided.

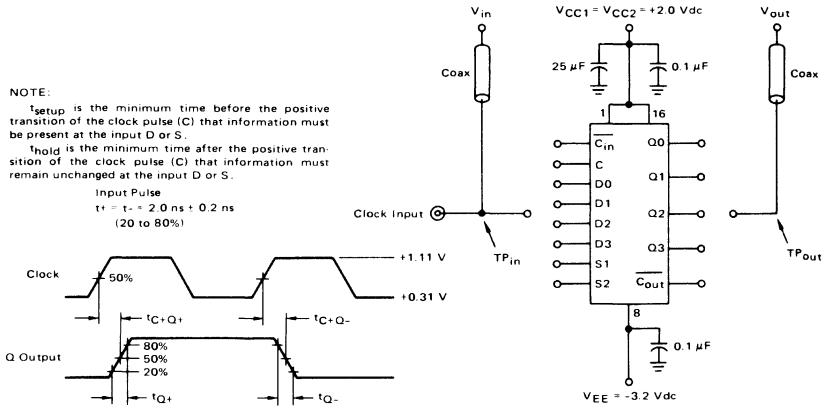
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

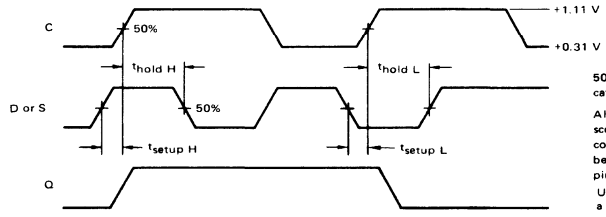
NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.

Input Pulse
$t_+ = t_- = 2.0$ ns ± 0.2 ns
(20 to 80%)



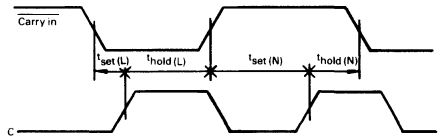


50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are connected to a 50-ohm resistor to ground.

$\overline{\text{CARRY IN}}$ SET UP AND HOLD TIMES



APPLICATIONS INFORMATION

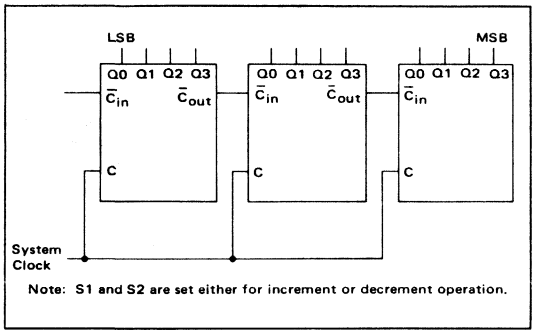
To provide more than four bits of counting capability several MC10136 counters may be cascaded. The $\overline{\text{Carry In}}$ input overrides the clock when the counter is either in the increment mode or the decrement mode of operation. This input allows several devices to be cascaded in a fully synchronous multistage counter as illustrated in Figure 1. The carry is advanced between stages as shown with no external gating. The $\overline{\text{Carry In}}$ of the first device may be left open. The system clock is common to all devices.

The various operational modes of the counter make it useful for a wide variety of applications. If used with MECL III devices, prescalers with input toggle frequencies in excess of 300 MHz are possible. Figure 2 shows such a prescaler using the MC10136 and MC1670. Use of the MC10231 in place of the MC1670 permits 200 MHz operation.

The MC10136 may also be used as a programmable counter. The configuration of Figure 3 requires no additional gates, although maximum frequency is limited to about 50 MHz. The divider modulus is equal to the program input plus one (M = N + 1), therefore, the counter will divide by a modulus varying from 1 to 16.

A second programmable configuration is also illustrated in Figure 4. A pulse swallowing technique is used to speed the counter operation up to 110 MHz typically. The divider modulus for this figure is equal to the program input (M = N). The minimum modulus is 2 because of the pulse swallowing technique, and the modulus may vary from 2 to 15. This programmable configuration requires an additional gate, such as ½MC10109 and a flip-flop such as ½MC10131.

FIGURE 1 — 12 BIT SYNCHRONOUS COUNTER



Note: S1 and S2 are set either for increment or decrement operation.

FIGURE 2 — 300 MHz PRESCALER

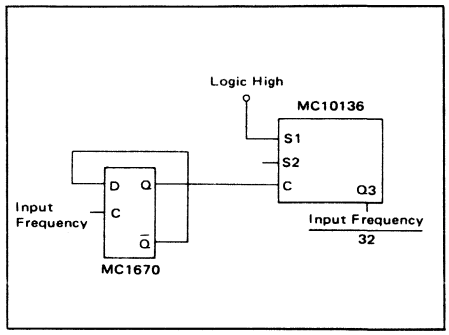
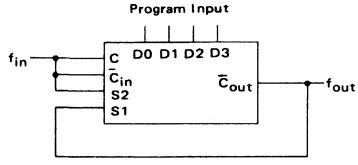


FIGURE 3 — 50 MHz PROGRAMMABLE COUNTER

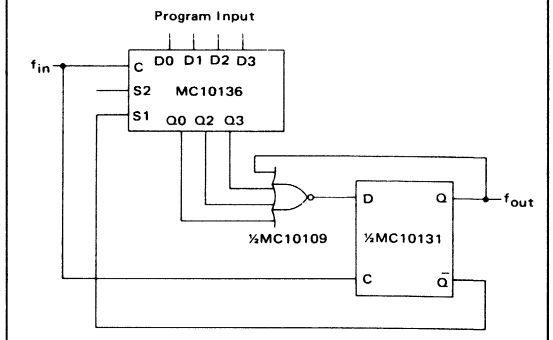


1 $f_{out} = \dfrac{f_{in}}{\text{Program Input} + 1}$

2 $f_{max} \cong 50$ MHz Typ.

3 Divide Ratio is from 1 to 16.

FIGURE 4 — 100 MHz PROGRAMMABLE COUNTER



1 $f_{out} = \dfrac{f_{in}}{\text{Program Input}}$

2 $f_{max} \cong 110$ MHz Typ.

3 Divide Ratio is from 2 to 15.

MOTOROLA

MC10137

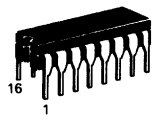
UNIVERSAL DECADE COUNTER

UNIVERSAL DECADE COUNTER

The MC10137 is a high speed synchronous counter that can count up, down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications. The synchronous count feature makes the MC10137 suitable for either computers or instrumentation.

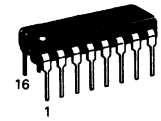
Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count. The $\overline{\text{Carry Out}}$ on the MC10137 is partially decoded from Q1 and Q2 directly, so in the preset mode the condition of the $\overline{\text{Carry Out}}$ after the Clock's positive excursion will depend on the condition of Q1 and/or Q2. The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The sequence for counting out of improper states is as shown in the State Diagrams.

P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ
t_{pd} = 3.3 ns typ (C-Q)
= 7.0 ns typ (C-$\overline{C}_{out}$)
= 5.0 ns typ ($\overline{C}_{in}$-$\overline{C}_{out}$)



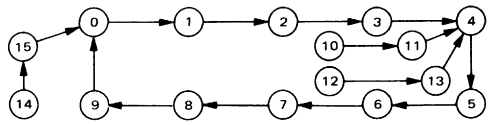
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

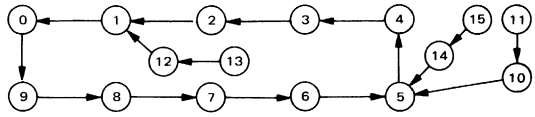


STATE DIAGRAMS

COUNT UP



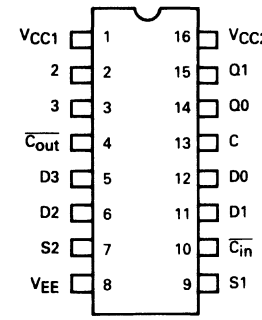
COUNT DOWN



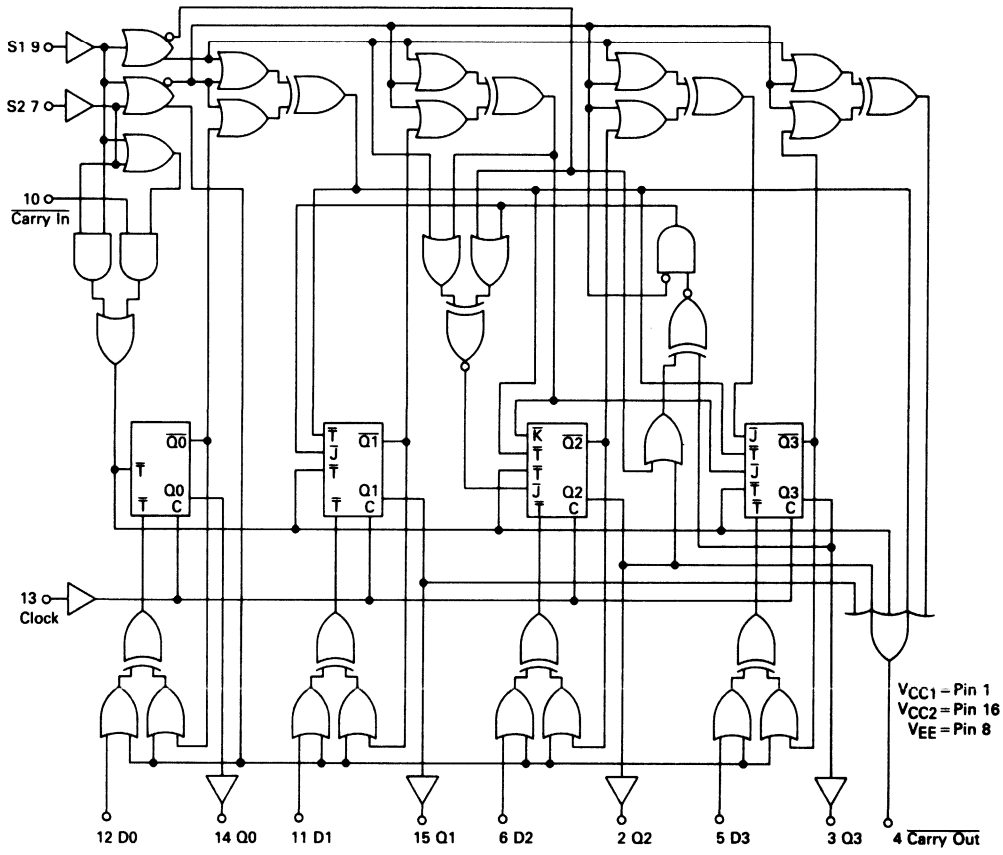
FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

PIN ASSIGNMENT



LOGIC DIAGRAM



NOTE: Flip-flops will toggle when all $\overline{T}$ inputs are low.

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	H	H	H	L	ϕ	H	H	H	H	L	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	L	L	L	H
H	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	L	L	L	H
L	L	H	H	L	L	ϕ	H	H	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L

ϕ = Don't care.
*Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
**A clock H is defined as a clock input transition from a low to a high logic level.

ELECTRICAL CHARACTERISTICS

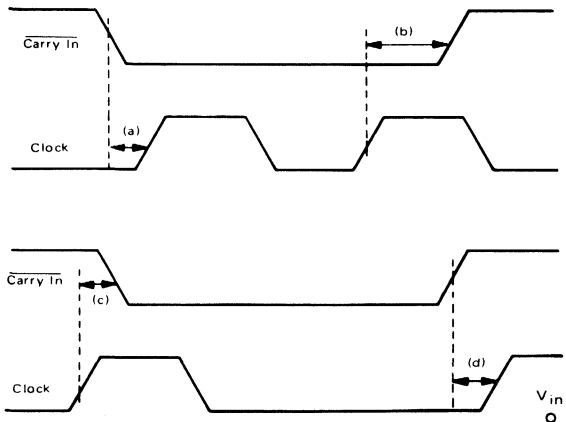
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test Procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10137L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8		165		120	150		165	mAdc					8	1, 16
Input Current	$I_{in\ H}$	5,6,11,12		350			220		220	μAdc	5,6,11,12				8	1, 16
		7		425			265		265		7					
		9,10		390			245		245		9,10					
		13		460			290		290		13					
	$I_{in\ L}$	All	0.5		0.5			0.3		μAdc		①			8	1, 16
Logic "1" Output Voltage	V_{OH}	14 ②	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	12	7, 9			8	1, 16
Logic "0" Output Voltage	V_{OL}	14 ②	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc		7, 9			8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	14 ②	-1.080		-0.980			-0.910		Vdc		7, 9	12		8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	14 ②		-1.655			-1.630		-1.595	Vdc		7, 9		12	8	1, 16
Switching Times (50-ohm Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay																
Clock Input	t_{13+14+}	14	0.8	4.8	1.0	3.3	4.5	1.1	5.0	ns	12		13	14	8	1, 16
	t_{13+14-}	14	0.8	4.8	1.0	3.3	4.5	1.1	5.0					14		
	t_{13+4+}	4	2.0	10.9	2.5	7.0	10.5	2.4	11.5		7			4		
	t_{13+4-}	4	2.0	10.9	2.5	7.0	10.5	2.4	11.5		7			4		
$\overline{\text{Carry In}}$ To $\overline{\text{Carry Out}}$	t_{10-4-}	4 ③	1.6	7.4	1.6	5.0	6.9	1.9	7.5		7	13	10	4		
	t_{10+4+}	4	1.6	7.4	1.6	5.0	6.9	1.9	7.5		7	13	10	4		
Set Up Time																
Data Inputs	t_{12+13+}	14	3.5		3.5	–		3.5				7, 9	12, 13	14		
	t_{12-13+}	14	3.5		3.5	–		3.5				7, 9	12, 13			
Select Inputs	t_{9+13+}	14	7.5		7.5	–		7.5					9, 13			
	t_{7+13+}	14	7.5		7.5	–		7.5					7, 13			
$\overline{\text{Carry In}}$ Input	t_{10-13+}	14	4.5		3.7	–		4.5			7	9	10, 13	14		
	t_{13+10+}	14	−1.0		-1.0	–		−1.0			7	9	10, 13	14		
Hold Time																
Data Inputs	t_{13+12+}	14	0		0	–		0				7, 9	12, 13	14		
	t_{13+12-}	14	0		0	–		0				7, 9	12, 13			
Select Inputs	t_{13+9+}	14	−2.5		-2.5	–		−2.5					9, 13			
	t_{13+7+}	14	−2.5		-2.5	–		−2.5					7, 13			
$\overline{\text{Carry In}}$ Input	t_{13+10-}	14	−1.6		-1.6	–		−1.6			7	9	10, 13			
	t_{10+13+}	14	4.0		3.1	–		4.0			7	9	10, 13			
Counting Frequency	$f_{countup}$	14	125		125	150		125		MHz	7		13			
	$f_{countdown}$	14	125		125	150		125		MHz	9					
Rise Time (20% to 80%)	t_{4+}	4	0.9	3.3	1.1	2.0	3.3	1.1	3.5	ns	7			4		
	t_{14+}	14				2.0								14		
Fall Time (20% to 80%)	t_{4-}	4				2.0								4		
	t_{14-}	14				2.0								14		

① Individually apply $V_{IL\ min}$ to pin under test. ② Measure output after clock pulse V_{IL} ⌐ V_{IH} appears at clock input (pin 13) ③ Before test set Q1 and Q2 outputs to a logic low.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



(a) is the minimum time to wait after the counter has been enabled to clock it.

(b) is the minimum time before the counter has been disabled that it may be clocked.

(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.

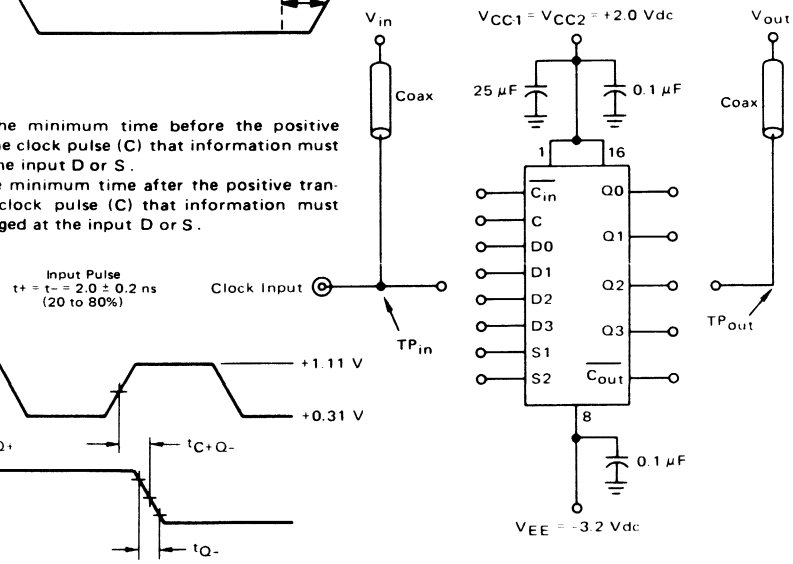
(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.

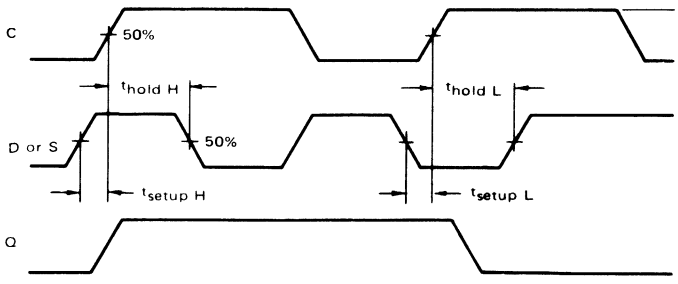
(b) and (c) may be negative numbers.

NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.





50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are connected to a 50-ohm resistor to ground.

MOTOROLA

MC10138

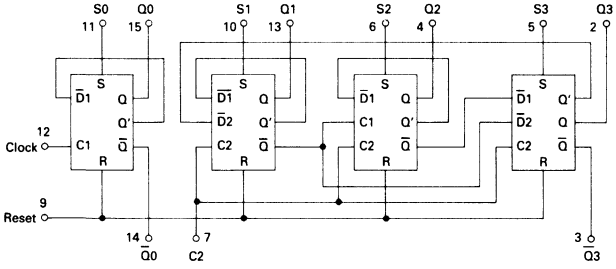
BI-QUINARY COUNTER

The MC10138 is a four bit counter capable of divide by two, five, or ten functions. It is composed of four set-reset master-slave flip-flops. Clock inputs trigger on the positive going edge of the clock pulse.

Set or reset input override the clock, allowing asynchronous "set" or "clear." Individual set and common reset inputs are provided, as well as complementary outputs for the first and fourth bits.

P_D = 370 mW typ/pkg (No Load)
f_{tog} = 150 MHz typ
t_r, t_f = 2.5 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

COUNTER TRUTH TABLES

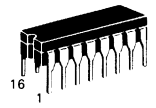
BI-QUINARY
(Clock connected to C2 and $\overline{Q3}$ connected to C1)

COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	H	L	H
9	L	L	H	H

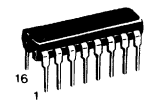
BCD
(Clock connected to C1 and $\overline{Q0}$ connected to C2)

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

BI-QUINARY COUNTER



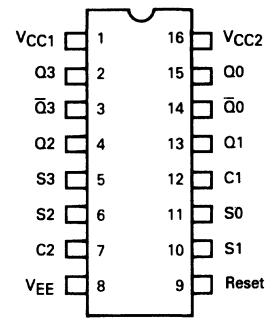
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10138 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8		97		70	88		97	mAdc	9				8	1,16
Input Current	$I_{in\,H}$	12		350			220		220		12					
		5,6,10,11		390			245		245		5,6,10,11					
		7		460			290		290		7					
		9		650			410		—		9					
	$I_{in\,L}$	All	0.5		0.5			0.3		μAdc		•			8	1,16
Logic "1" Output Voltage	V_{OH}	3,14 ②	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	9				8	1,16
		2,4,13,15 ①	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	5,6,10,11				8	1,16
Logic "0" Output Voltage	V_{OL}	3,14 ①	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	5,6,10,11				8	1,16
		2,4,13,15 ②	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	9				8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2,4,13,15 ①	-1.080		-0.980			-0.910		Vdc			5,6,10,11		8	1,16
		3,14 ②	↓		↓			↓		↓			9		↓	↓
		13,15 ①											7,12			
Logic "0" Threshold Voltage	V_{OLA}	2,4,13,15 ②		-1.655			-1.630		-1.595	Vdc				5,6,10,11	8	1,16
		3,14 ①		↓			↓		↓	↓				9	↓	↓
		13,15 ②												7,12		
Switching Times (50-ohm Load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay																
Clock Delays 50 Ω Loads	t_{12+15+}	15	1.4	5.0	1.5	3.5	4.8	1.5	5.3	ns			12	15	8	1,16
	t_{12+14+}	14	↓	5.0	↓	↓	4.8	↓	5.3	↓			12	14	↓	↓
	t_{7+13+}	13		5.2			5.0		5.5				7	13		
	t_{7+4+}	4		↓			↓		↓				↓	4		
	t_{7+2+}	2												2		
	t_{7+3+}	3												3		
	t_{12+15-}	15		5.0			4.8		5.3				12	15		
	t_{12+14-}	14		5.0			4.8		5.3				12	14		
	t_{7+13-}	13		5.2			5.0		5.5				7	13		
	t_{7+4-}	4		↓			↓		↓				↓	4		
	t_{7+2-}	2												2		
	t_{7+3-}	3				↓								3		
Set Delay	t_{11+15+}	15		5.2		—							11	15		
	t_{11+14-}	14		5.2		—							11	14		
Reset Delay	t_{9+14+}	14		↓		—							9	14		
	t_{9+15-}	15	↓		↓	—	↓	↓	↓	↓			9	15		
Rise Time (20% to 80%)	t_{14+}	14	1.1	4.7	1.1	2.5	4.5	1.1	5.0	ns			11	14		
	t_{15+}	15	1.1	4.7	1.1	↓	4.5	1.1	5.0	↓			11	15		
Fall Time (20% to 80%)	t_{14-}	14	↓	↓	↓		↓	↓	↓				9	14		
	t_{15-}	15											9	15		
Counting Frequency	f_{count}	2	125		125	150		125		MHz			7	2	↓	↓
		15	125		125	150		125		MHz			12	15		

*Individually apply V_{ILmin} to pin under test.

① Set all four flip-flops by applying pulse

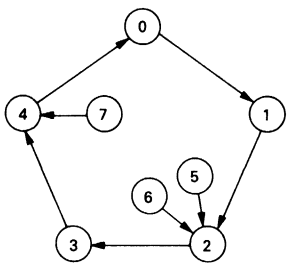
② Reset all four flip-flops by applying pulse

V_{IHmax} / V_{ILmin} to pins 5,6,10,11 prior to applying test voltage indicated.

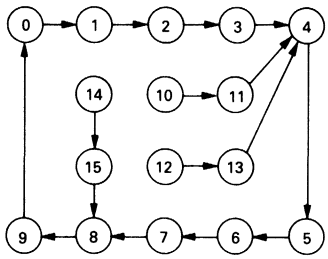
V_{IHmax} / V_{ILmin} to pin 9 prior to applying test voltage indicated.

COUNTER STATE DIAGRAM — POSITIVE LOGIC

Clock connected to C2



$\overline{Q0}$ connected to C2



MOTOROLA

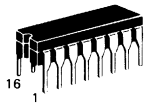
MC10141

FOUR-BIT UNIVERSAL SHIFT REGISTER

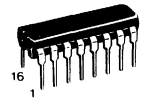
The MC10141 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

P_D = 425 mW typ/pkg (No Load)
f_{Shift} = 200 MHz typ
t_r, t_f = 2.0 ns typ (20%–80%)

FOUR-BIT UNIVERSAL SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

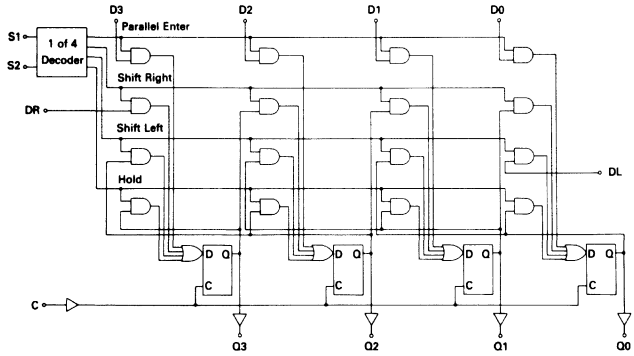


P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM



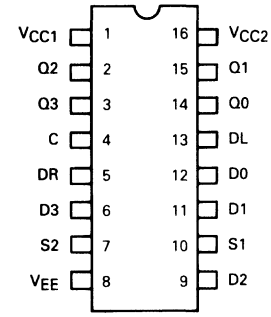
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

SELECT			OUTPUTS			
S1	S2	OPERATING MODE	$Q0_{n+1}$	$Q1_{n+1}$	$Q2_{n+1}$	$Q3_{n+1}$
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	$Q1_n$	$Q2_n$	$Q3_n$	DR
H	L	Shift Left*	DL	$Q0_n$	$Q1_n$	$Q2_n$
H	H	Stop Shift	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$

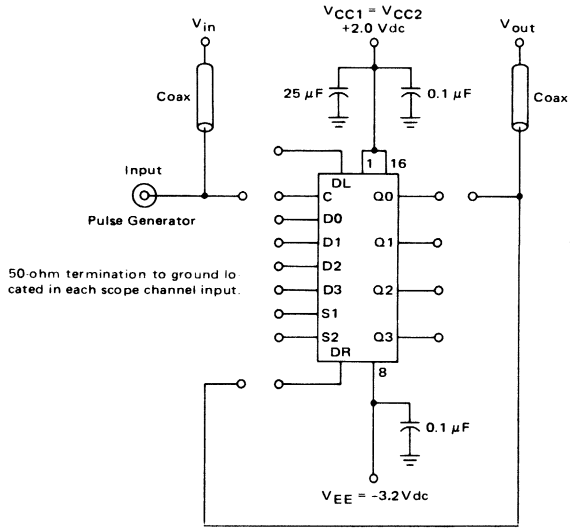
*Outputs as exist after pulse appears at "C" input with input conditions as shown. (Pulse = Positive transition of clock input).

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

SHIFT FREQUENCY TEST CIRCUIT



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Test Procedures:

1. Set D1, D2, D3 = +0.31 Vdc (Logic L)
   D0 = +1.11 Vdc (Logic H)
2. Apply Clock pulse V_{IH} / V_{IL} to set Q0 high.
3. Maintain Clock Low.
   Set S1 = +0.31 Vdc (Logic L)
   S2 = +1.11 Vdc (Logic H)
4. Test Shift Frequency

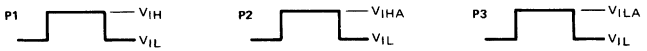
3

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10141 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P1	P2	P3	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	112	–	82	102	–	112	mAdc	–	–	–	–	8	–	–	–	1,16
Input Current	$I_{in\ H}$	5	–	350	–	–	220	–	220	μAdc	5	–	–	–	8	–	–	–	1,16
		6	–	350	–	–	220	–	220		6	–	–	–		–	–	–	
		7	–	390	–	–	245	–	245		7	–	–	–		–	–	–	
		4	–	425	–	–	265	–	265		4	–	–	–		–	–	–	
	$I_{in\ L}$	12	0.5	–	0.5	–	–	0.3	–	μAdc	4,5,6,7,9, 10,11,13	12	–	–	8	–	–	–	1,16
Logic "1" Output Voltage	V_{OH}	3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	–	–	–	8	4	–	–	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	4	–	–	1,16
Logic "1" Threshold Voltage	V_{OHA} ①	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	6	–	8	4	–	–	1,16
				–		–	–		–		6	④	–	7		4	–	–	
				–		–	–		–		6	④	–	–		–	4	–	
				–		–	–		–		–	–	–	–		–	–	4	
Logic "0" Threshold Voltage	V_{OLA} ①	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	6	8	4	–	–	1,16
			–		–	–		–			–	⑤	–	7		4	–	–	
			–		–	–		–			–	⑤	–	–		–	4	–	
			–		–	–		–			6	–	–	–		–	–	4	
Switching Times (50 Ω Load)																			
Propagation Delay	t_{4+3+}	3	1.7	3.9	1.8	2.9	3.8	2.0	4.2	ns	②	–	–	–	-3.2 V	–	–	–	+2.0 V
Setup Time (t_{setup})	t_{12+4+}	14	2.5	–	2.5	–	–	2.5	–		–	–	–	–	8	–	–	–	1,16
	t_{10+4+}	14	5.5	–	5.0	–		5.5	–		–	–	–	–		–	–	–	
Hold Time (t_{hold})	t_{4+12+}	14	1.5	–	1.5	–	–	1.5	–		–	–	–	–		–	–	–	
Rise Time (20% to 80%)	t_{3+}	3	1.0	3.4	1.1	2.0	3.3	1.1	3.6		②	–	–	–		–	–	–	
Fall Time (20% to 80%)	t_{3-}	3	1.0	3.4	1.1	2.0	3.3	1.1	3.6		②	–	–	–		–	–	–	
Shift Frequency	f_{Shift}	–	150	–	150	200	–	150	–	MHz	③	–	–	–		–	–	–	



① These tests to be performed in sequence as shown.
② See switching time test circuit for test procedures.
③ See shift frequency test circuit for test procedures.
④ Reset to zero before performing test
⑤ Reset to one before performing test.

MOTOROLA

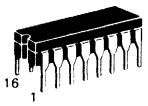
MC10153

QUAD LATCH

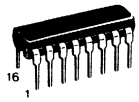
The MC10153 is a high speed, low power, MECL quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs. Open emitters allow a large number of outputs to be wire-ORed together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is low, outputs will follow D inputs. Information is latched on positive going transition of the clock. The MC10153 provides the same logic function as the MC10133, except for inversion of the clock.

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

QUAD LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 620

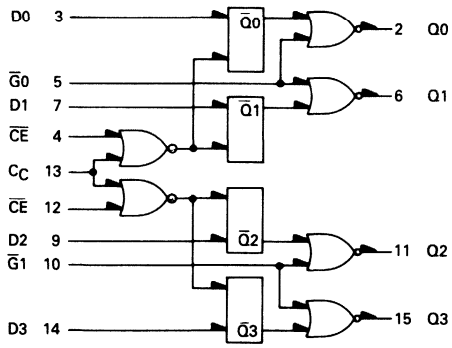


P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM



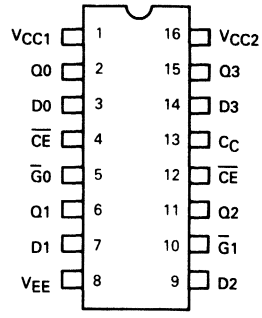
TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	H	ϕ	Q_n
L	L	L	L
L	L	H	H

ϕ = Don't Care
C = C_C + $\overline{CE}$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10153 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	83	–	–	75	–	83	mAdc	–	13	–	–	8	1,16
Input Current	I_{inH}	3	–	390	–	–	245	–	245	µAdc	3	–	–	–	8	1,16
		4	–	390	–	–	245	–	245		4	–	–	–		
		5	–	560	–	–	350	–	350		5	–	–	–		
		13	–	460	–	–	290	–	290		13	–	–	–		
	I_{inL}	3	0.5	–	0.5	–	–	0.3	–	µAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3	4	–	–	8	1,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3	13	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	3,13	–	–	8	1,16
		2				–					3,5	13	–	–		
		2				–					–	3,4	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	3	4	–	5	8	1,16
		2		–		–	–		–		–	4	3	–		
		2		–		–	–		–		3	4	–	–		
		2†		–		–	–		–		3	–	–	–		
		2††		–		–	–		–		–	–	–	–		
		2††		–		–	–		–		–	–	–	–		
		2		–		–	–		–		3	–	–	4		
		2		–		–	–		–		3	–	–	13		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	3	4	5	–	8	1,16
		2	–		–	–		–			–	4	–	3		
		2	–		–	–		–			–	4	–	–		
		2†	–		–	–		–			–	–	–	–		
		2††	–		–	–		–			3	–	–	–		
		2††	–		–	–		–			3	–	–	13		
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	1.0	5.6	1.0	4.0	5.4	1.1	5.9	ns	–	–	3	2	8	1,16
	t_{4-2+}	2	1.0	5.6	1.0	4.0	5.6	1.2	6.2		3 *	–	4	2		
	t_{5-2+}	2	1.0	3.2	1.0	2.0	3.1	1.0	3.4		–	–	5	2		
	t_{Setup}	3	2.5	–	2.5	0.7	–	2.5	–		–	–	3	2		
	t_{Hold}	3	1.5	–	1.5	0.7	–	1.5	–		–	–	3	2		
Rise Time (20% to 80%)	t_{2+}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8		–	–	3	2		
Fall Time (20% to 80%)	t_{2-}	2	1.0	3.6	1.1	2.0	3.5	1.1	3.8		–	–	3	2		

†Output level to be measured after a clock pulse has been applied to the clock input (Pin 4). ⌐⌐ V_{IH} max, V_{IL} min

††Data input at proper high/low level while clock pulse is low so that device latches at proper high/low level for test. Levels are measured after device has latched.

*Latch set to zero state before test.

MOTOROLA

MC10154

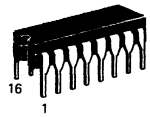
BINARY COUNTER

The MC10154 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight or a divide-by-sixteen function.

Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous "set" or "clear." Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

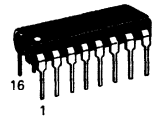
P_D = 370 mW typ/pkg (No Load)
f_{toggle} = 150 m Hz (typ)
t_{pd} = 3.5 ns typ (C to Q_0)
t_{pd} = 11 ns typ (C to Q_3)

BINARY COUNTER

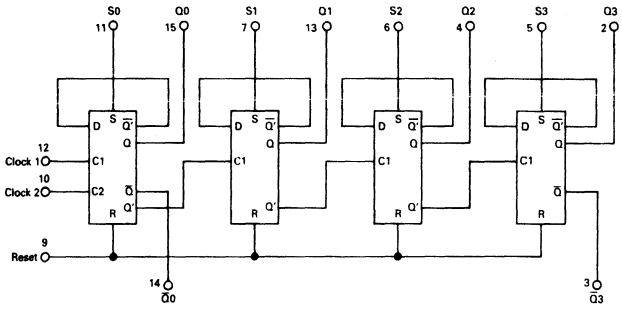


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



LOGIC DIAGRAM



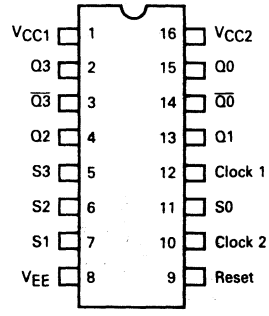
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

INPUTS						OUTPUTS			
R	S_0	S_1	S_2	S_3	C_1	C_2	Q_0	Q_1	Q_2	Q_3
H	L	L	L	L	ϕ	ϕ	L	L	L	L
L	H	H	H	H	ϕ	ϕ	H	H	H	H
L	L	L	L	L	H	ϕ	No Count			
L	L	L	L	L	ϕ	H	No Count			
L	L	L	L	L	*	*	H	H	H	H
L	L	L	L	L	*	*	L	H	H	H
L	L	L	L	L	*	*	H	L	H	H
L	L	L	L	L	*	*	L	L	H	H
L	L	L	L	L	*	*	H	H	L	H
L	L	L	L	L	*	*	L	H	L	H
L	L	L	L	L	*	*	H	L	L	H
L	L	L	L	L	*	*	L	L	L	H
L	L	L	L	L	*	*	H	H	H	L
L	L	L	L	L	*	*	L	H	H	L
L	L	L	L	L	*	*	H	L	H	L
L	L	L	L	L	*	*	L	L	H	L
L	L	L	L	L	*	*	H	H	L	L
L	L	L	L	L	*	*	L	H	L	L
L	L	L	L	L	*	*	H	L	L	L
L	L	L	L	L	*	*	L	L	L	L

ϕ = Don't Care
* V_{IL} → V_{IH} Clock transitions from V_{IL} to V_{IH} may be applied to C_1 or C_2 or both for same effect.

PIN ASSIGNMENT



3

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10154 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	97	–	–	88	–	97	mAdc	9	–	–	–	8	1,16
Input Current	I_{inH}	12	–	390	–	–	245	–	245	µAdc	12	–	–	–	8	1,16
		11	–	350	–	–	220	–	220	µAdc	11	–	–	–	8	1,16
		9	–	650	–	–	410	–	410	µAdc	9	–	–	–	8	1,16
	I_{inL}	*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	14	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	11	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	14	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	11	–	–	–	8	1,16
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		14	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	11	–	8	1,16
		15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	9	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		14	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	11	8	1,16
		15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	9	8	1,16
Switching Times													Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input Propagation Delay	t_{12+15+}	15	1.4	5.0	1.5	3.5	4.8	1.5	5.3	ns	–	–	12	15	8	1,16
	t_{12-13-}	13	1.9	9.4	2.0	6.0	9.2	2.0	9.8		–	–		13		
	t_{12+4-}	4	2.9	12.3	3.0	8.5	12	3.0	12.8		–	–		4		
	t_{12-3+}	3	3.9	14.9	4.0	11	14.5	4.0	15.5		–	–		3		
Rise Time (20 to 80%)	t_{15+}	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0		–	–		15		
Fall Time (20 to 80%)	t_{15-}	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0		–	–		15		
Set Input	t_{11-15+}	15	1.4	5.2	1.5	—	5.0	1.5	5.5	ns	–	–	11	15	8	1,16
Reset Input	t_{9-15+}	15	1.4	5.2	1.5	—	5.0	1.5	5.5	ns	–	–	9	15	8	1,16
Counting Frequency	f_{count}	15	125	–	125	150	–	125	–	MHz	–	–	12	15	8	1,16

*Individually test each input applying V_{IL} to input under test.

MOTOROLA

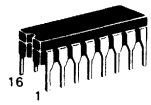
MC10158

QUAD 2-INPUT MULTIPLEXER (NON-INVERTING)

The MC10158 is a quad two channel multiplexer. A common select input determines which data inputs are enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, and D31.

P_D = 197 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to Q)
3.2 ns typ (Select to Q)
t_r, t_f = 2.5 ns typ (20%–80%)

QUAD 2-INPUT MULTIPLEXER (NON-INVERTING)

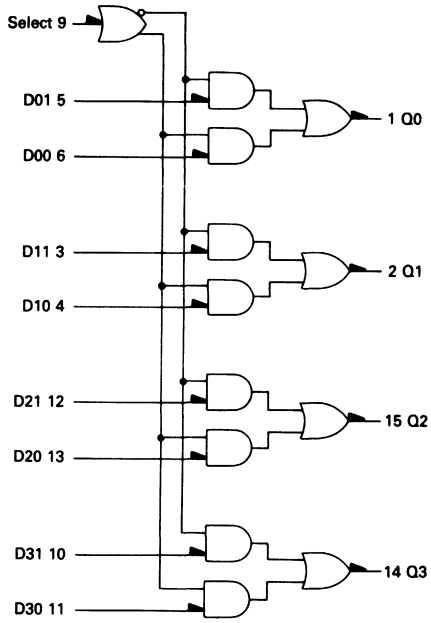


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM



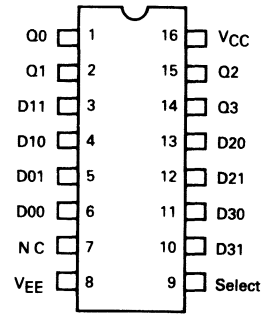
TRUTH TABLE

Select	D0	D1	Q
L	ϕ	L	L
L	ϕ	H	H
H	L	ϕ	L
H	H	ϕ	H

ϕ = Don't care

V_{CC} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

3

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10158 TEST LIMITS -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	53	–	38	48	–	53	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	9	–	360	–	–	225	–	225	µAdc	9	–	–	–	8	16
		5	–	400	–	–	250	–	250	µAdc	5	–	–	–	8	16
	I_{inL}	5	0.5		0.5		–	0.3	–	µAdc	–	5	–	–	8	16
Logic "1" Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	16
Logic "0" Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	16
Logic "1" Threshold Voltage	V_{OHA}	1	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	16
Logic "0" Threshold Voltage	V_{OLA}	1	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	16
Switching Times (50 Ω Load)											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay										ns					8	16
Data Input	t_{5-1-}	1	1.3	3.1	1.2	2.5	3.0	1.3	3.2		–	–	5	1		
Select Input	t_{9+1+}	1	2.5	4.8	2.4	3.2	4.5	2.5	4.8		6	–	9	1		
Rise Time (20% to 80%)	t_{1+}	1	1.6	3.4	1.5	2.5	3.3	1.6	3.4		–	–	5	1		
Fall Time (20% to 80%)	t_{1-}	1	1.6	3.4	1.5	2.5	3.3	1.6	3.4		–	–	5	1		

MOTOROLA

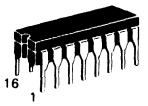
MC10159

QUAD 2-INPUT MULTIPLEXER (INVERTING)

The MC10159 is a quad two channel multiplexer with enable. It incorporates common enable and common data select inputs. The select input determines which data inputs are enabled. A high (H) level enables data inputs D00, D10, D20, and D30. A low (L) level enables data inputs D01, D11, D21, and D31. Any change on the data inputs will be reflected at the outputs while the enable is low. Input levels are inverted at the output.

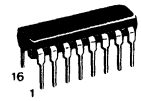
P_D = 218 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to Q)
3.2 ns typ (Select to Q)
t_r, t_f = 2.5 ns typ (20%–80%)

QUAD 2-INPUT MULTIPLEXER (INVERTING)



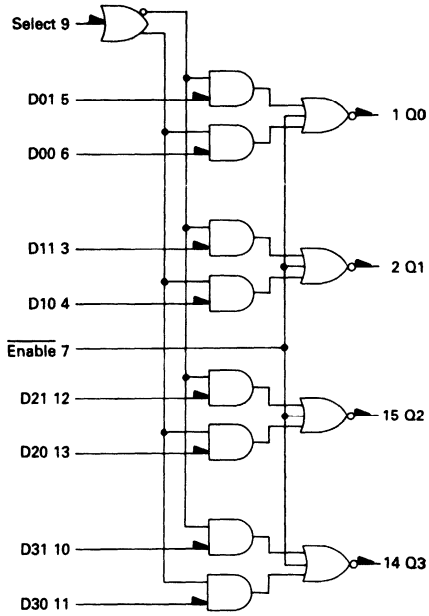
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM



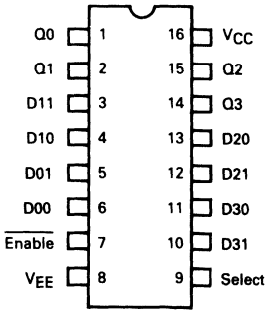
TRUTH TABLE

Enable	Select	D0	D1	Q
L	L	ϕ	L	H
L	L	ϕ	H	L
L	H	L	ϕ	H
L	H	H	ϕ	L
H	ϕ	ϕ	ϕ	L

ϕ = Don't Care

V_{CC} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10159 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	58	–	42	53	–	58	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	9	–	360	–	–	225	–	225	µAdc	9	–	–	–	8	16
		5	–	400	–	–	250	–	250	µAdc	5	–	–	–	8	16
	I_{inL}	5	0.5		0.5		–	0.3	–	µAdc	–	5	–	–	8	16
Logic "1" Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	16
Logic "0" Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	16
Logic "1" Threshold Voltage	V_{OHA}	1	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9	–	–	6	8	16
Logic "0" Threshold Voltage	V_{OLA}	1	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	–	6	–	8	16
Switching Times (50 Ω Load)											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay										ns					8	16
Data Input	t_{5+1-}	1	1.1	3.8	1.2	2.5	3.3	1.1	3.8		–	–	5	1		
Select Input	t_{9+1-}	1	1.5	5.3	1.5	3.2	5.0	1.5	5.3		6	–	9	1		
Enable Input	t_{7+1-}	1	1.4	5.3	1.5	2.5	5.0	1.4	5.3		3,12	–	7	1		
Rise Time (20% to 80%)	t_{1+}	1	1.0	3.7	1.1	2.5	3.5	1.0	3.7		9	–	5	1		
Fall Time (20% to 80%)	t_{1-}	1	1.0	3.7	1.1	2.5	3.5	1.0	3.7		9	–	5	1		

MOTOROLA

MC10160

12-BIT PARITY GENERATOR-CHECKER

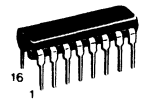
The MC10160 consists of nine EXCLUSIVE-OR gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high. Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

P_D = 320 mW typ/pkg (No Load)
t_{pd} = 5.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

12-BIT PARITY GENERATOR-CHECKER

L SUFFIX
CERAMIC PACKAGE
CASE 620

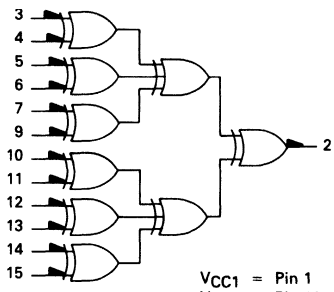
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

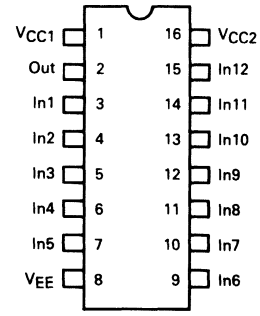
LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for one set of conditions. Complete testing according to truth table.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10160 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	86	–	62	78	–	86	mAdc	4,5,9,10,13,14	–	–	–	8	1,16
Input Current	I_{inH}*	3	–	425	–	–	265	–	265	µAdc	3	–	–	–	8	1,16
		4	–	350	–	–	220	–	220	µAdc	4	–	–	–	8	1,16
	I_{inL}	3	0.5	–	0.5	–	–	0.3	–	µAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3	4,5,6,7,9,10, 11,12,13,14,15	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	3,4,5,6,7,9,10, 11,12,13,14,15	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	4,5,6,7,9,10,11, 12,13,14,15	3	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	3,5,6,7,9,10,11 12,13,14,15	–	4	8	1,16
Switching Times (50 Ω Load) Propagation Delay											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
	t_{3+2+}	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	ns	–	–	3	2	8	1,16
	t_{3+2-}	↓	↓	↓	↓	↓	↓	↓	↓	↓	4	–	↓	↓	↓	↓
	t_{3-2-}										–	–				
	t_{3-2+}										4	–	↓			
	t_{4+2+}										–	–	4			
	t_{4+2-}										3	–	↓			
	t_{4-2-}										–	–				
	t_{4-2+}	↓	↓	↓	↓	↓	↓	↓	↓		3	–	↓			
Rise Time (20% to 80%)	t_{2+}		1.1	3.5	1.1	2.0	3.3	1.0	3.5		–	–	3			
Fall Time (20% to 80%)	t_{2-}	↓	1.1	3.5	1.1	2.0	3.3	1.0	3.5	↓	–	–	3	↓	↓	↓

*Pins 3, 6, 7, 11, 12, 15 are similar
Pins 4, 5, 9, 10, 13, 14 are similar

MOTOROLA

MC10161

BINARY TO 1-8 DECODER (LOW)

The MC10161 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high.

The MC10161 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This design provides the identical 4 ns delay from any address or enable input to any output.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1. This system, using the MC10136 control counters, has the capability of incrementing, decrementing or holding data channels. When both S0 and S1 are low, the index counters reset, thus initializing both the mux and demux units. The four binary outputs of the counter are buffered by the MC10101s to send twisted-pair select data to the multiplexer/demultiplexer units.

P_D = 315 mW typ/pkg (No Load)

t_{pd} = 4.0 ns type

t_r, t_f = 2.0 ns typ (20%–80%)

BINARY TO 1-8 DECODER (LOW)

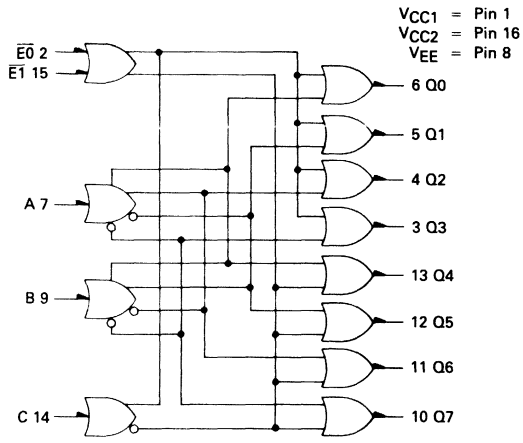
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

3

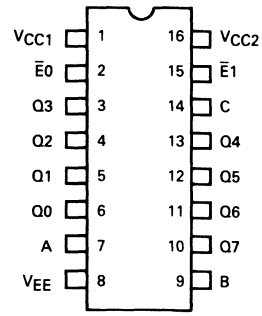
LOGIC DIAGRAM



TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E1}$	$\overline{E0}$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H
ϕ	H	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H

DIP PIN ASSIGNMENT



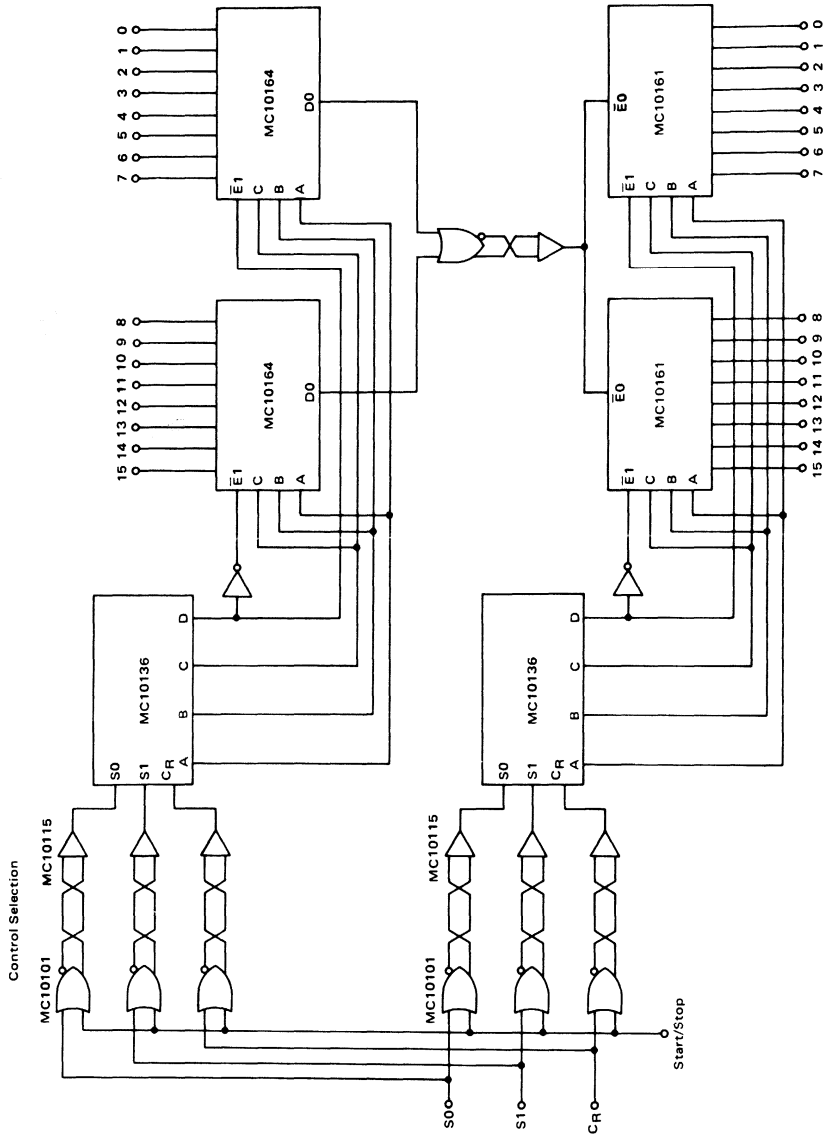
Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input/output combination. Other combinations are tested according to the truth table.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10161 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	**84**	–	61	76	–	**84**	mAdc	2,7,9,14,15				8	1,16
Input Current	I_{inH}	14	–	**350**	–	–	220	–	**220**	µAdc	14				8	1,16
	I_{inL}	14	**0.5**	–	0.5	–	–	**0.3**	–	µAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	2				8	1,16
		13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	15				8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	14		–		8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	2	–	8	1,16
		13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	15	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	14	–	8	1,16
Switching Times (50 Ω Load)													**Pulse In**	**Pulse Out**	**-3.2 V**	**+2.0 V**
Propagation Delay	t_{14+13-}	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	–		14	13	8	1,16
	t_{14-13+}	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4		–					
Rise Time (20% to 80%)	t_{13+}	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		–					
Fall Time (20% to 80%)	t_{13-}	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		–					

FIGURE 1 – HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER



MOTOROLA

MC10162

BINARY TO 1-8 DECODER (HIGH)

The MC10162 is designed to convert three lines of input data to a one-of-eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

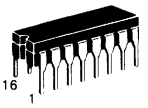
The MC10162 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders.

This device is ideally suited for demultiplexer applications. One of the two enable inputs is used as the data input, while the other is used as a data enable input.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1 of the MC10161 data sheet.

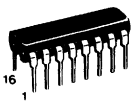
P_D = 315 ns typ/pkg (No Load)
t_{pd} = 4.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

BINARY TO 1-8 DECODER (HIGH)



L SUFFIX
CERAMIC PACKAGE
CASE 620

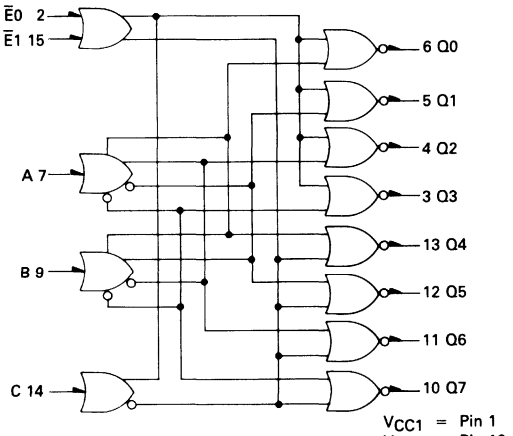
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM



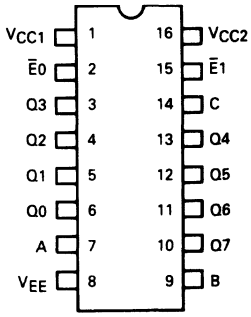
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

INPUTS					OUTPUTS							
Ē0	Ē1	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L
ϕ	H	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L

ϕ = Don't Care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only input/output combination. Other combinations are tested according to the truth table.

@Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10162 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	84	–	61	76	–	84	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	14	–	350	–	–	220	–	220	µAdc	14	–	–	–	8	1,16
	I_{inL}	14	0.5	–	0.5	–	–	0.3	–	µAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	2	–	–	–	8	1,16
		13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	15	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	14	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	2	–	8	1,16
		13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	15	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{14+13+}	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	–	–	14	13	8	1,16
	t_{14-13-}	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4		–	–				
Rise Time (20% to 80%)	t_+	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		–	–				
Fall Time (20% to 80%)	t_-	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5		–	–				

MOTOROLA

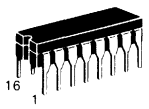
MC10164

8-LINE MULTIPLEXER

The MC10164 is a high speed, low power eight-channel data selector which routes data present at one-of-eight inputs to the output. The data is routed according to the three bit code present on the address inputs. An enable input is provided for easy bit expansion.

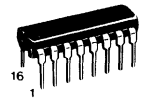
P_D = 310 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ (Data to Output)
t_r, t_f = 2.0 ns typ (20%–80%)

8-LINE MULTIPLEXER



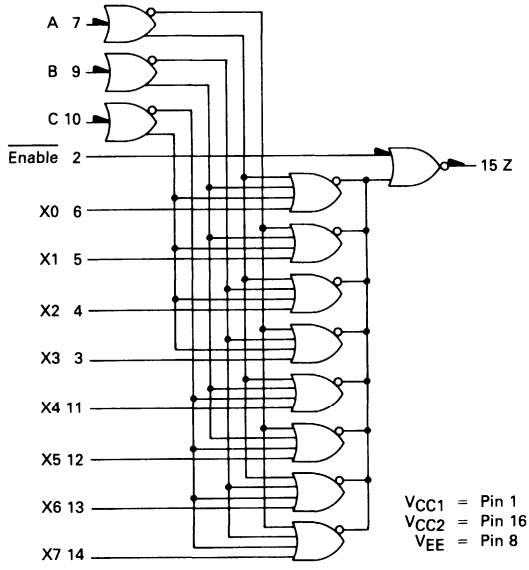
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM

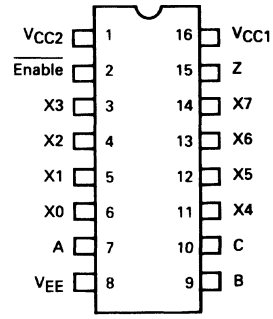


TRUTH TABLE

	ADDRESS INPUTS			
ENABLE	C	B	A	Z
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	ϕ	ϕ	ϕ	L

ϕ = Don't Care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10164 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	83	–	60	75	–	83	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	2	–	425	–	–	265	–	265	μAdc	4	–	–	–	8	1,16
	$I_{in\ L}$	4	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	4,9	–	–	2	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	–	–	2	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+15+}	15	1.5	4.9	1.5	3.0	4.7	1.6	5.0	ns	9	–	4	15	8	1,16
	t_{4-15-}	15	1.5	4.9	1.5	3.0	4.7	1.6	5.0		9	–	4			
	t_{7+15+}	15	1.9	6.5	2.0	4.0	6.2	2.2	6.7		5	–	7			
	t_{7-15-}	15	1.9	6.5	2.0	4.0	6.2	2.2	6.7		5	–	7			
	t_{2+15-}	15	0.9	3.5	1.0	2.0	3.1	1.0	3.3		7,5	–	2			
	t_{2-15+}	15			1.0		3.1	1.0	3.3		7,5	–	2			
Rise Time (20% to 80%)	t_+	15		3,3	1.1		3.3	1.2	3.6		9	–	4			
Fall Time (20% to 80%)	t_-	15			1.1		3.3	1.2	3.6		9	–	4			

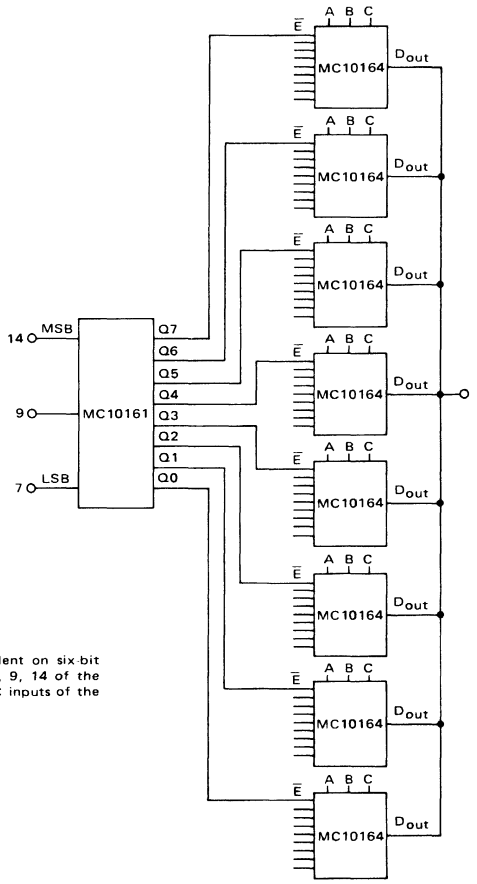
3

APPLICATION INFORMATION

The MC10164 can be used wherever data multiplexing or parallel to serial conversion is desirable. Full parallel gating permits equal delays through any data path. The output of the MC10164 incorporates a buffer gate with eight data inputs and an enable. A high level on the enable forces the output low. The MC10164 can be connected directly to a data bus, due to its open emitter output and output enable.

Figure one illustrates how a 1-of-64 line multiplexer can be built with eight MC10164's wire ORed at their outputs and one MC10161 to drive the enables on each multiplexer, without speed degradation over a single MC10164 being experienced.

FIGURE 1 – 1-OF-64 LINE MULTIPLEXER



The Bit chosen is dependent on six-bit code present on inputs 7, 9, 14 of the MC10161 and the A, B, C inputs of the MC10164.

MOTOROLA

MC10165

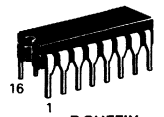
8-INPUT PRIORITY ENCODER

The MC10165 is a device designed to encode eight inputs to a binary coded output. The output code is that of the highest order input. Any input of lower priority is ignored. Each output incorporates a latch allowing synchronous operation. When the clock is low the outputs follow the inputs and latch when the clock goes high. This device is very useful for a variety of applications in checking system status in control processors, peripheral controllers, and testing systems.

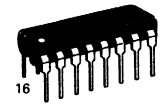
The input is active when high, (e.g., the three binary outputs are low when input D0 is high). The Q3 output is high when any input is high. This allows direct extension into another priority encoder when more than eight inputs are necessary. The MC10165 can also be used to develop binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.

P_D = 545 mW typ/pkg (No Load)
t_{pd} = 4.5 ns typ (Data to Output)
t_r, t_f = 2.0 ns typ (20%–80%)

8-INPUT PRIORITY ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

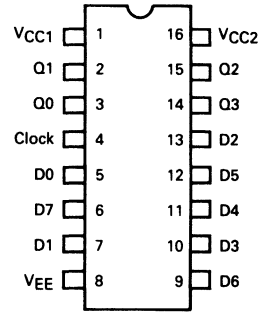
3

TRUTH TABLE

DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	L
L	H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	H
L	L	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	H	L
L	L	L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H
L	L	L	L	H	ϕ	ϕ	ϕ	H	H	L	L
L	L	L	L	L	H	ϕ	ϕ	H	H	L	H
L	L	L	L	L	L	H	ϕ	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

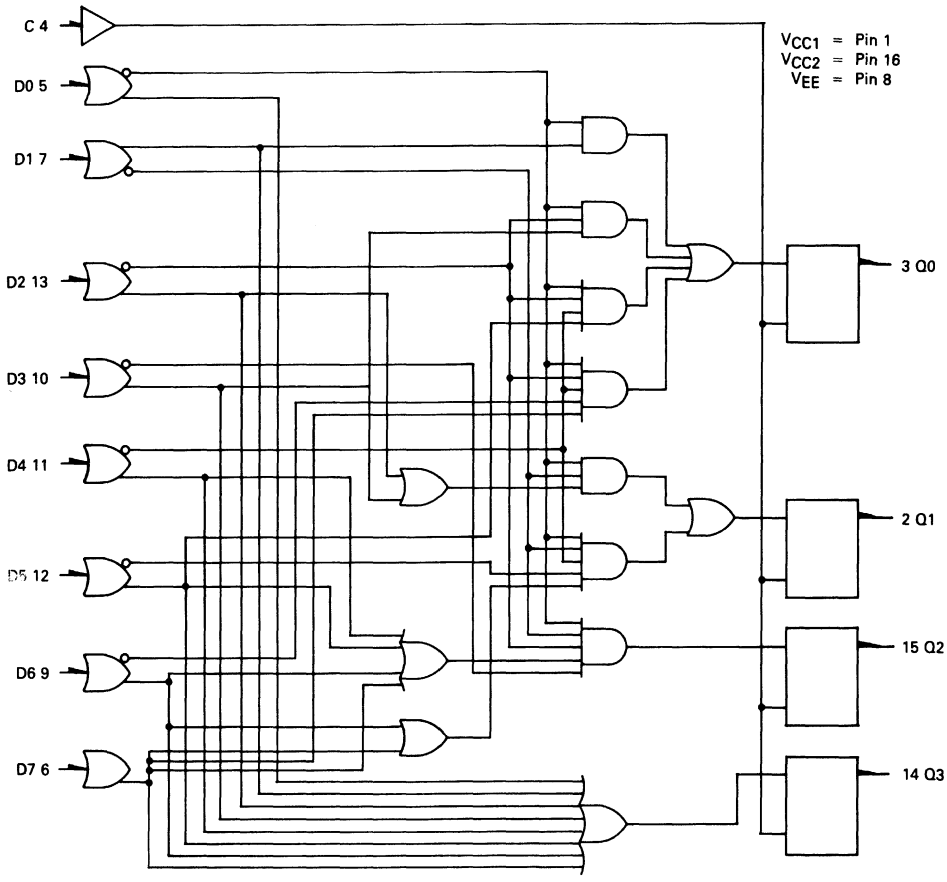
ϕ = Don't Care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

LOGIC DIAGRAM



Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10165 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	144	–	105	131	–	144	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	390	–	–	245	–	245	μAdc	4	–	–	–	8	1,16
		5	–	350	–	–	220	–	220	μAdc	5 ①	–	–	–	8	1,16
	$I_{in\ L}$	4	0.5	–	0.5	–	–	0.3	–	μAdc	–	4	–	–	8	1,16
		5	0.5	–	0.5	–	–	0.3	–	μAdc	–	5①	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	4	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700				–	–		
		14	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700				–	–		
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700				–	–		
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	4	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		–		–	–		
		14	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		–		–	–		
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615		–		–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	4	6	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–		–			–		
		14	-1.080	–	-0.980	–	–	-0.910	–		–			–		
		15	-1.080	–	-0.980	–	–	-0.910	–		–			–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	4	–	6	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595		–		–			
		14	–	-1.655	–	–	-1.630	–	-1.595		–		–			
		15	–	-1.655	–	–	-1.630	–	-1.595		–		–			
Switching Times (50-ohm Load)										Unit	+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data Input	t_{5+14+}	14	2.0	7.0	3.0	–	7.0	2.0	8.0	ns	–	4	5	14	8	1,16
	t_{5-14-}	14				–					–		5	14		
	t_{7+3+}	3				–					–		7	3		
	t_{11+15+}	15				–					–		11	15		
	t_{13+2+}	2				–					–		13	2		
Clock Input	t_{4-3+}	3 ②	1.5	4.5	2.0	–	4.0	1.5	4.5		7	–	4	3		
	t_{4-3-}	3 ③				–					–	–		3		
	t_{4-14+}	14②				–					7	–		14		
	t_{4-14-}	14③				–					–	–		14		
Setup Time	$t_{setup\ H}$	3	6.0	–	6.0	3.4	–	6.0	–		–	–	4,7	3		
	$t_{setup\ L}$		6.0	–	6.0	3.0	–	6.0	–		–	–				
Hold Time	$t_{hold\ H}$		1.0	–	1.0	-2.3	–	1.0	–		–	–				
	$t_{hold\ L}$		1.0	–	1.0	-2.7	–	1.0	–		–	–				
Rise Time (20% to 80%)	t_{3+}		1.1	3.5	1.1	2.0	3.3	1.1	3.5		–	4	7			
Fall Time (20% to 80%)	t_{3-}		1.1	3.5	1.1	2.0	3.3	1.1	3.5		–	4	7			

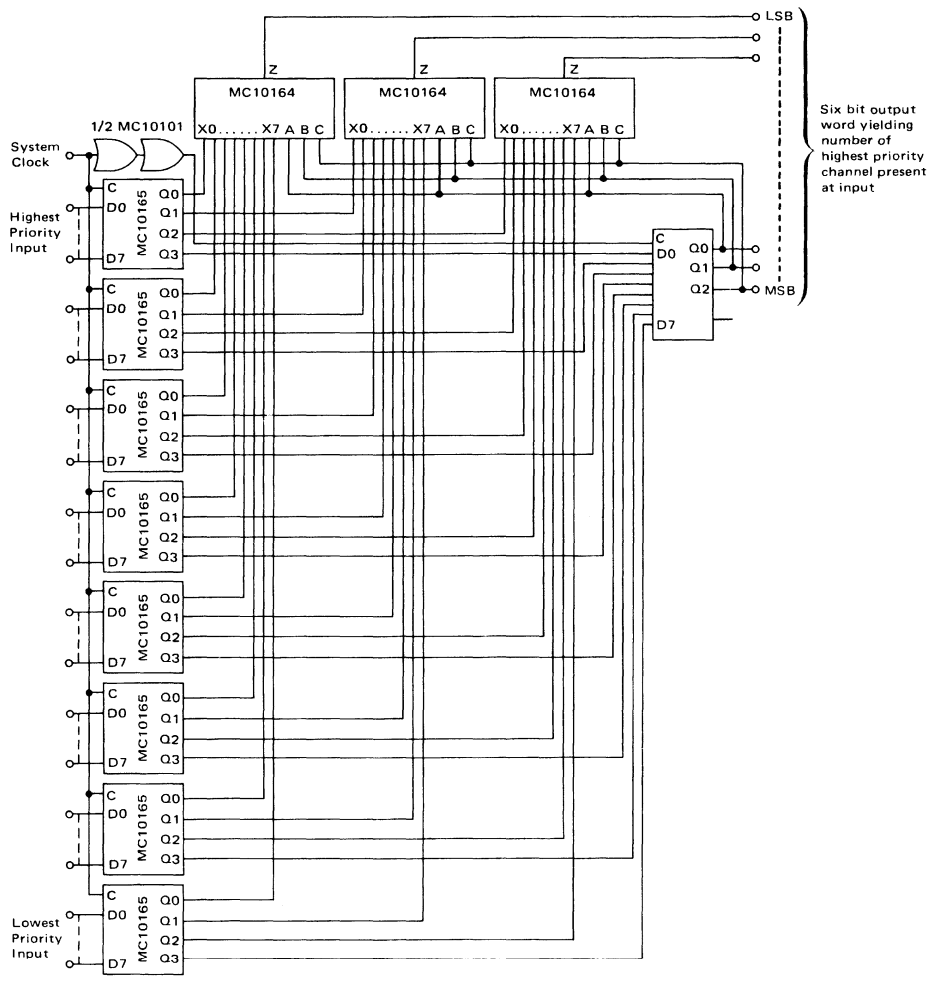
① The same limit applies for all D type input pins. To test input currents for other D inputs, individually apply proper voltage to pin under test.
② Output latched to low state prior to test.
③ Output latched to high state prior to test.

* To preserve reliable performance, the MC10165P (plastic-packaged device only) is to be operated in ambient temperatures above 70°C only when 500 lfpm blown air or equivalent heat sinking is provided.

APPLICATION INFORMATION

A typical application of the MC10165 is the decoding of system status on a priority basis. A 64 line priority encoder is shown in the figure below. System status lines are connected to this encoder such that, when a given condition exists, the respective input will be at a logic high level. This scheme will select the one of 64 different system conditions, as represented at the encoder inputs, which has priority in determining the next system operation to be performed. The binary code showing the address of the highest priority input present will appear at the encoder outputs to control other system logic functions.

64-LINE PRIORITY ENCODER



MOTOROLA

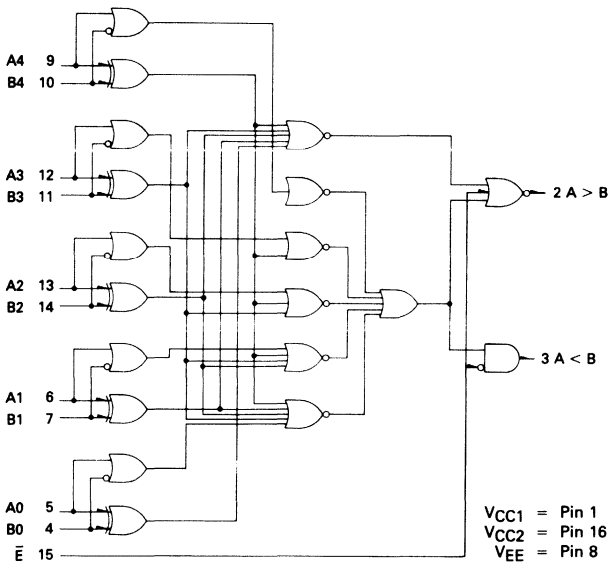
MC10166

5-BIT MAGNITUDE COMPARATOR

The MC10166 is a high speed expandable 5-bit comparator for comparing the magnitude of two binary words. Two outputs are provided: A < B and A > B. A = B can be obtained by NORing the two outputs with an additional gate. A high level on the enable function forces both outputs low. Multiple MC10166s may be used for larger word comparisons.

P_D = 440 mW typ/pkg (No Load)
t_{pd} = Data to output 6.0 ns typ
$\overline{E}$ to output 2.5 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

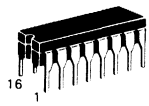
LOGIC DIAGRAM



TRUTH TABLE

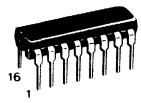
Inputs			Outputs	
$\overline{E}$	A	B	A < B	A > B
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A > Word B		L	H
L	Word A < Word B		H	L

5-BIT MAGNITUDE COMPARATOR



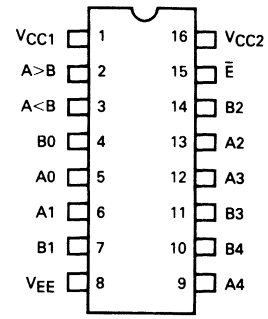
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

3

ELECTRICAL CHARACTERISTICS

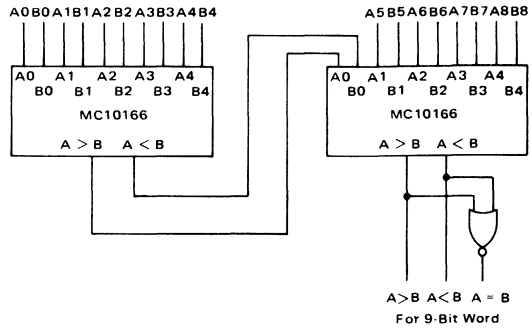
Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10166 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	117	–	85	106	–	117	mAdc	–	4,7,10,11,14	–	–	8	1,16
Input Current	I_{inH}	5	–	350	–	–	220	–	220	μAdc	5	–	–	–	8	1,16
	I_{inL}	5	0.5	–	0.5	–	–	0.3	–	μAdc	–	5	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5,15	–	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,15	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	5	–	–	15	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	4	–	–	15	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	5	–	15	–	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	4	–	15	–	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay Data to Output	t_{9+2+}	2	1.0	8.0	1.0	6.0	7.6	1.0	8.4	ns	–	–	9	2	8	1,16
	t_{9-2-}	2									–	–	9	2		
	t_{11-2+}	2									12	–	11	2		
	t_{11+2-}	2									12	–	11	2		
	t_{7+3+}	3									6	–	7	3		
	t_{7-3-}	3									6	–	7	3		
Enable to Output	t_{15-3+}	3		3.8		2.5	3.6		4.0		10	–	15	3		
	t_{15+3-}	3		3.8		2.5	3.6		4.0		10	–	15	3		
Rise Time (20% to 80%)	t_{2+}	2		3.6	1.1	2.0	3.5	1.1	3.8		–	–	9	2		
Fall Time (20% to 80%)	t_{2-}	2		3.6	1.1	2.0	3.5	1.1	3.8		–	–	9	2		

APPLICATION INFORMATION

FIGURE 1 — 9-BIT MAGNITUDE COMPARATOR



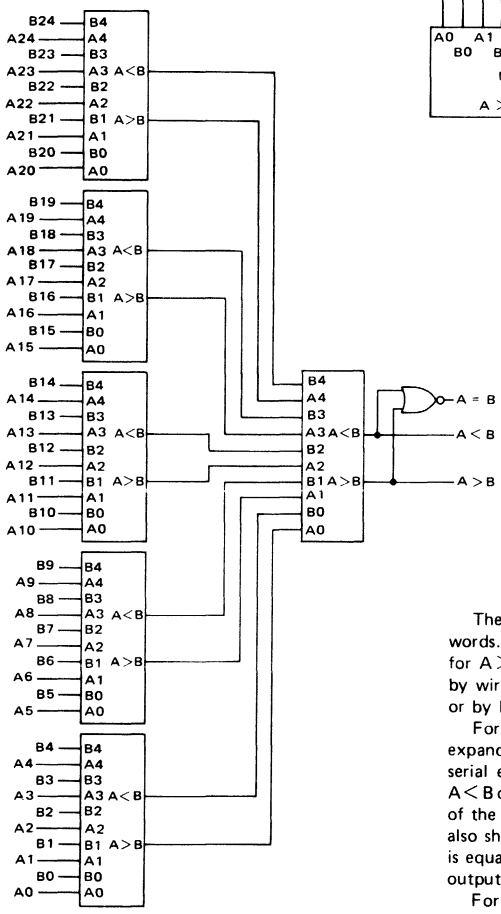


FIGURE 2 — 25-BIT MAGNITUDE COMPARATOR

The MC10166 compares the magnitude of two 5-bit words. Two outputs are provided which give a high level for A > B and A < B. The A = B function can be obtained by wire-ORing these outputs (a low level indicates A = B) or by NORing the outputs (a high level indicates A = B).

For longer word lengths, the MC10166 can be serially expanded or cascaded. Figure 1 shows two devices in a serial expansion for a 9-bit word length. The A > B and A < B outputs are fed to the A0 and B0 inputs respectively of the next device. The connection for an A = B output is also shown. The worst case delay time of serial expansion is equal to the number of comparators times the data-to-output delay.

For shorter delay times than possible with serial expansion, devices can be cascaded. Figure 2 shows a 25-bit cascaded comparator whose worst case delay is two data-to-output delays. The cascaded scheme can be extended to longer word lengths.

MOTOROLA

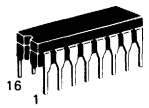
MC10168

QUAD LATCH

The MC10168 is a Quad Latch with common clocking to all four latches. Separate output enabling gates are provided for each latch, allowing direct wiring to a bus. When the clock is high, outputs will follow the D inputs. Information is latched on the negative-going transition of the clock.

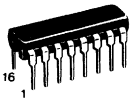
P_D = 310 mW typ/pkg (No Load)
t_{pd} = $\overline{G}$ to Q = 2 ns typ
D to Q = 3 ns typ
C to Q = 4 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

QUAD LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 620

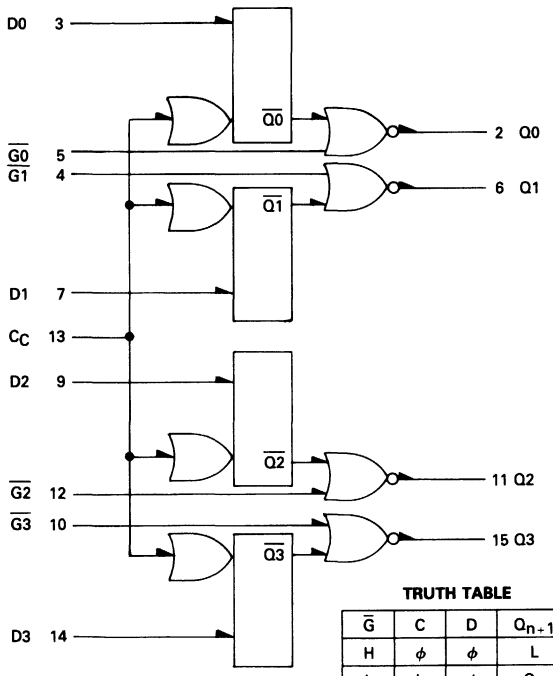
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM



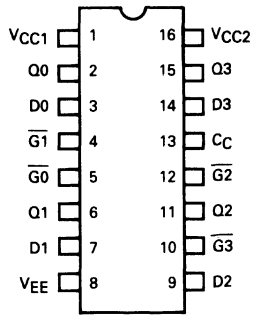
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H

ϕ = don't care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-1.890	-1.890	-1.205	-1.500	-5.2
+25°C	-1.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10168 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	82	–	60	75	–	82	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	3,7,9,14	–	390	–	–	245	–	245	µAdc	*	–	–	–	8	1,16
		4,5,10,12	–	425	–	–	265	–	265	↓	*	–	–	–	↓	↓
		13	–	460	–	–	290	–	290		13	–	–	–		
	I_{inL}	*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,13	–	–	–	8	1,16
		6	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7,13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	3,5	–	–	–	8	1,16
		6	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,7	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	13	–	3	–	8	1,16
		6	-1.080	–	-0.980	–	–	-0.910	–	Vdc	13	–	7	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	13	–	–	3	8	1,16
		6	–	-1.655	–	–	-1.630	–	-1.595	Vdc	13	–	–	7	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay: Data	t_{3+2+}	2	1.0	5.6	1.0	3.0	5.4	1.1	5.9	ns	–	–	3	2	8	1,16
Gate	t_{5-2+}	2	↓	3.2	↓	2.0	3.1	1.0	3.4	↓	–	–	5	2	↓	↓
Clock	t_{13+2+}	2	↓	5.8	↓	4.0	5.6	1.2	6.2		–	–	13	2		
Setup Time	t_{3+13+}	2	2.5	–	2.5	–	–	2.5	–		–	–				
Hold Time	t_{13+3+}	2	1.0	–	1.0	–	–	1.0	–		–	–				
Rise Time (20% to 80%)	t_{2+}	2	↓	3.6	1.1	2.0	3.5	1.1	3.8	↓	–	–	3	2	↓	↓
Fall Time (20% to 80%)	t_{2-}	2	↓	3.6	1.1	2.0	3.5	1.1	3.8		–	–	3	2		

*Individually test each input applying V_{IH} or V_{IL} to input under test.

MOTOROLA

MC10170

9 + 2-BIT PARITY GENERATOR-CHECKER

The MC10170 is a 11-bit parity circuit, which is segmented into 9 data bits and 2 control bits.

Output A generates odd parity on 9 bits; that is, Output A goes high for an odd number of high logic levels on the bit inputs in only 2 gate delays.

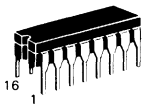
The Control Inputs can be used to expand parity to larger numbers of bits with minimal delay or can be used to generate even parity. To expand parity to larger words, the MC10170 can be used with the MC10160 or other MC10170's. The MC10170 can generate both even and odd parity.

P_D = 300 mW typ/pkg (No Load)

t_{pd} = 2.5 ns typ (Control Inputs to B Output)
4.0 ns typ (Data Inputs to A Output)
6.0 ns typ (Data Inputs to B Output)

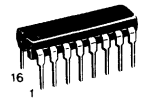
t_r, t_f = 2.0 ns typ (20%–80%)

9 + 2-BIT PARITY GENERATOR-CHECKER



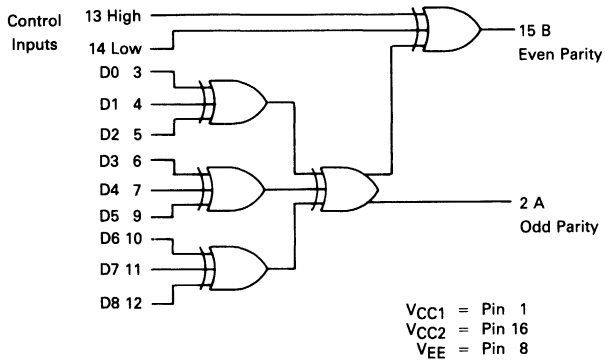
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

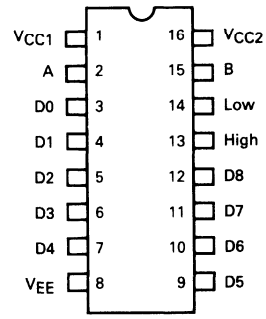
LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

INPUTS	OUTPUTS	
Sum of D Inputs at High Level	Odd Parity Output A	Even Parity Output B
Even	Low	High
Odd	High	Low

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECI 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10170 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	78	–	57	71	–	78	mAdc	–	–	–	–	–	1,16
Input Current	I_{inH}	3	–	350	–	–	200	–	220	µAdc	3	–	–	–	8	1,16
		5	–	350	–	–	220	–	220	µAdc	5	–	–	–	8	1,16
	I_{inL}	3	0.5	–	0.5	–	–	0.3	–	µAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	3,4,5	–	–	–	8	1,16
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4,5	–	–	–	8	1,16
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	13,14	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	13	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	13	8	1,16
Switching Times (50-ohm Load) Propagation Delay													Pulse In	Pulse Out	-3.2 V	+2.0 V
	t_{13+15+}	15	1.5	4.2	1.5	2.5	4.0	1.5	4.4	ns	–	–	13	15	8	1,16
	t_{14-15-}	15	1.5	4.2	1.5	2.5	4.0	1.5	4.4	↓	–	–	14	15	↓	↓
	t_{3+2-}	2	2.0	6.6	2.0	4.0	6.0	2.0	6.6	↓	–	–	3	2	↓	↓
	t_{3-15+}	15	4.0	9.5	4.0	6.0	8.8	4.0	9.5	↓	–	–	3	15	↓	↓
Rise Time (20% to 80%)	t_{2+}	2	1.5	4.3	1.5	2.0	3.9	1.5	4.3	ns	–	–	3	2	8	1,16
Fall Time (20% to 80%)	t_{2-}	2	1.5	4.3	1.5	2.0	3.9	1.5	4.3	ns	–	–	3	2	8	1,16

MOTOROLA

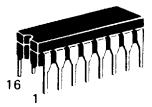
MC10171

DUAL BINARY TO 1-4-DECODER (LOW)

The MC10171 is a binary coded 2 line to dual 4 line decoder with selected outputs low. With either $\overline{E}0$ or $\overline{E}1$ high, the corresponding selected 4 outputs are high. The common enable $\overline{E}$, when high, forces all outputs high.

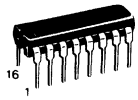
P_D = 325 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

BINARY TO 1-4-DECODER (LOW)



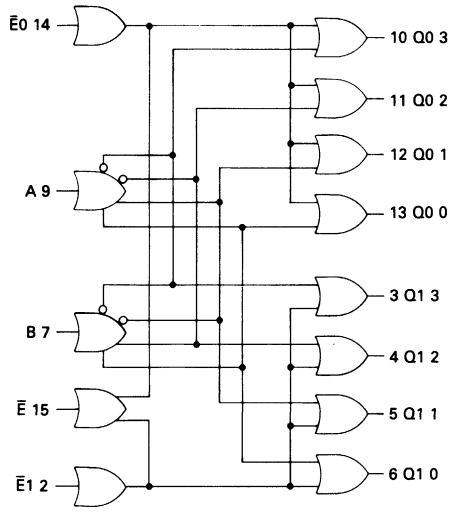
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM



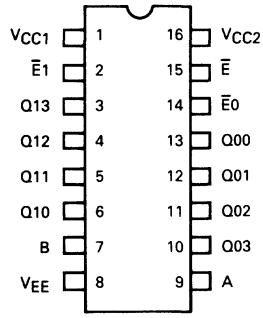
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

ENABLE INPUTS			INPUTS		OUTPUTS							
$\overline{E}$	$\overline{E}$0	$\overline{E}$1	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H

ϕ = Don't Care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test Procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
−30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10171 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	85	–	65	77	–	85	mAdc	2,7,9,14,15	–	–	–	8	1,16
Input Current	I_{inH}	14	–	350	–	–	220	–	220	μAdc	14	–	–	–	8	1,16
	I_{inL}	14	0.5	–	0.5	–	–	0.3	–	μAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	6	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	15	–	–	–	8	1,16
		13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	15	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	2,7,9,14,15	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	6	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	15	–	8	1,16
		13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	15	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,9,14,15	–	7	8	1,16
		13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,7,14,15	–	9	8	1,16
Switching Times (50 Ω Load)												+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+6+}	6	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	–	2,9,14,15	7	6	8	1,16
	t_{7-6-}	6	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	↓	6	↓	↓
	t_{7+13+}	13	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	↓	13	↓	↓
	t_{7-13-}	13	↓	↓	↓	↓	↓	↓	↓	↓	–	↓	↓	13	↓	↓
Rise Time (20% to 80%)	t_{6+}	6	1.0	3.3	1.1	2.0	3.3	1.1	3.4	↓	–	–	↓	6	↓	↓
	t_{13+}	13	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	13	↓	↓
Fall Time (20% to 80%)	t_{6-}	6	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	6	↓	↓
	t_{13-}	13	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	13	↓	↓

MOTOROLA

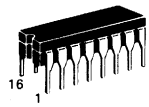
MC10172

DUAL BINARY TO 1-4-DECODER (HIGH)

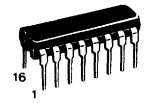
The MC10172 is a binary-coded 2 line to dual 4 line decoder with selected outputs high. With either $\overline{E}0$ or $\overline{E}1$ low, the corresponding selected 4 outputs are low. The common enable $\overline{E}$, when high, forces all outputs low.

P_D = 325 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

DUAL BINARY TO 1-4-DECODER (HIGH)



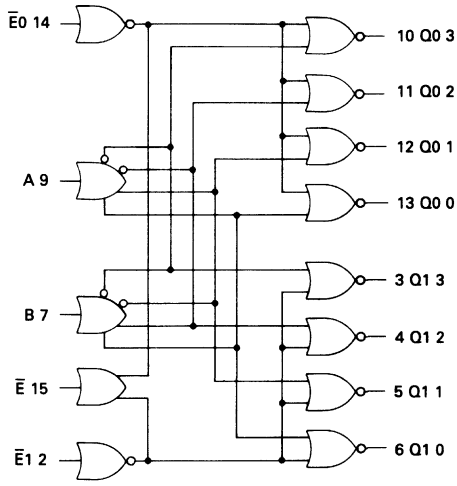
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM



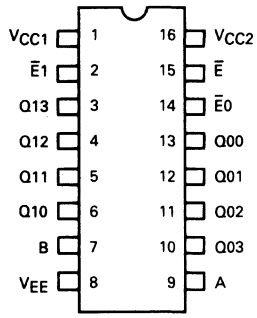
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

$\overline{E}$	$\overline{E}1$	$\overline{E}0$	A	B	Q1 0	Q1 1	Q1 2	Q1 3	Q0 0	Q0 1	Q0 2	Q0 3
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	L	H	L	H	L	L	L	H	L	L
L	H	H	H	L	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	L	L	H	L	L	L	L	L	L	L
H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L

ϕ = Don't Care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10172 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	85	–	62	77	–	85	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	14	–	350	–	–	220	–	220	µAdc	14	–	–	–	8	1,16
	I_{inL}	14	0.5	–	0.5	–	–	0.3	–	µAdc	–	14	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	6	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	2	–	–	–	8	1,16
		13	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	14	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	13	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	15	2,7,9,14	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	6	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	2	–	8	1,16
		13	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	14	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,9,14	–	7	8	1,16
		13	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	2,7,14	–	9	8	1,16
Switching Times (50 Ω Load)											+1.11 V	+0.31 V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{7+6-}	6	1.5	6.2	1.5	4.0	6.0	1.5	6.4	ns	2	9,14	7	6	8	1,16
	t_{7-6+}	6									2	9,14		6		
	t_{7+13-}	13									14	2,9		13		
	t_{7-13+}	13									14	2,9		13		
Rise Time (20% to 80%)	t_{6+}	6	1.0	3.3	1.1	2.0	3.3	1.1	3.4		2	9,14		6		
	t_{13+}	13									14	2,9		13		
Fall Time (20% to 80%)	t_{6-}	6									2	9,14		6		
	t_{13-}	13									14	2,9		13		

MOTOROLA

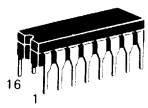
MC10173

QUAD 2-INPUT MULTIPLEXER/LATCH

The MC10173 is a quad two channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

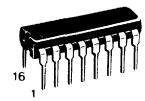
P_D = 275 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

QUAD 2-INPUT MULTIPLEXER/LATCH



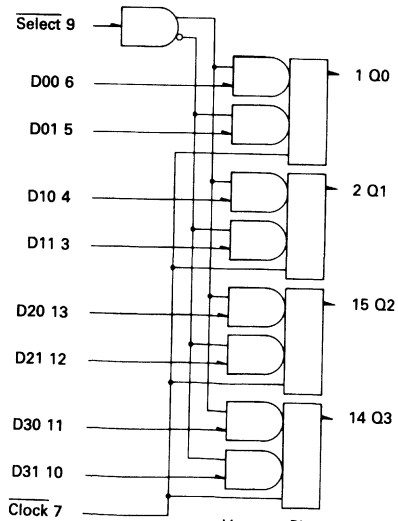
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM



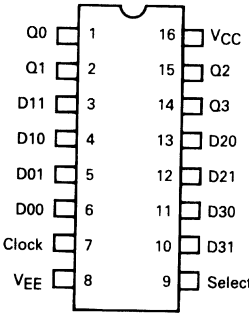
V_{CC} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

SELECT	CLOCK	$Q0_{n+1}$
H	L	D00
L	L	D01
ϕ	H	$Q0_n$

ϕ = Don't Care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10173 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8		73			66		73	mAdc					8	16
Input Current	I_{inH}	5		470			295		295	µAdc	5				8	16
		6		470			295		295		6					
		7		400			250		250		7					
		9		400			250		250		9					
Input Leakage Current	I_{inL}	All	0.5		0.5			0.3		µAdc		*			8	16
Logic "1" Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	6.9	7			8	16
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	5	7			8	16
Logic "0" Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	9	7			8	16
		2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc		7			8	16
Logic "1" Threshold Voltage	V_{OHA}	1	-1.080		-0.980			-0.910		Vdc	9	7	6		8	16
		2	-1.080		-0.980			-0.910		Vdc		7	5		8	16
Logic "0" Threshold Voltage	V_{OLA}	1		-1.655			-1.630		-1.595	Vdc	9	7		6	8	16
		2		-1.655			-1.630		-1.595	Vdc		7		5	8	16
Switching Times											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay																
Data Input	t_{6+1+}	1	0.8	3.7	1.0	2.5	3.5	1.1	5.3	ns	9	7	6	1	8	16
	t_{6-1-}										9		6			
	t_{5+1+}												5			
	t_{5-1-}												5			
Clock Input	t_{7-1+}		1.6	7.2	1.6	4.5	6.8	1.4	6.8		-		5.7			
	t_{7-1-}		1.6	7.2	1.6	4.5	6.8	1.4	6.8				5.7			
Select Input	t_{9+1+}		1.1	6.2	1.3	3.5	5.7	1.2	6.7		6	7	9			
	t_{9+1-}										5					
	t_{9-1+}										5					
	t_{9-1-}										6					
Setup Time																
Data Input	t_{setup}		2.0		2.0	1.5	-	2.0	-				5.7			
Select Input	t_{setup}		3.0		3.0	2.5		3.0			6		7.9			
Hold Time																
Data Input	t_{hold}		2.5		2.5	0.0	-	2.5	-				5.7			
Select Input	t_{hold}		1.5		1.5	-0.5	-	1.5	-		6		7.9			
Rise Time (20 to 80%)	t_+		1.2	4.0	1.5	2.0	3.5	1.4	4.0		5		7			
Fall Time (20 to 80%)	t_-		1.2	4.0	1.5	2.0	3.5	1.4	4.0				7			

*V_{ILmin} applied to each input pin, one at a time.

MOTOROLA

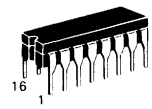
MC10174

DUAL 4 TO 1 MULTIPLEXER

The MC10174 is a high speed dual channel multiplexer with output enable capability. The select inputs determine one of four active data inputs for each multiplexer. An output enable forces both outputs low when in the high state.

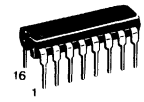
P_D = 305 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ (Data to output)
t_r, t_f = 2.0 ns typ (20%–80%)

DUAL 4 TO 1 MULTIPLEXER



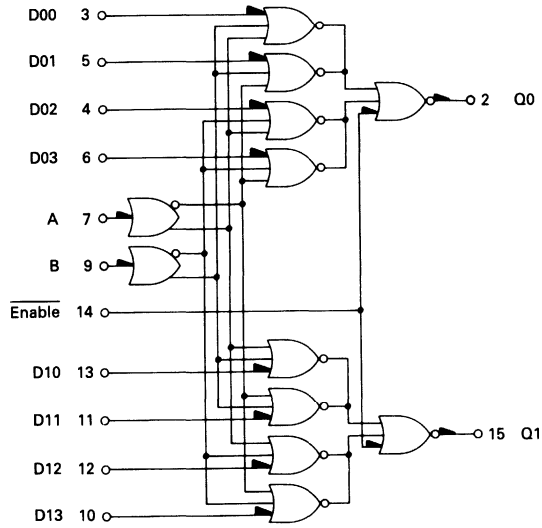
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM



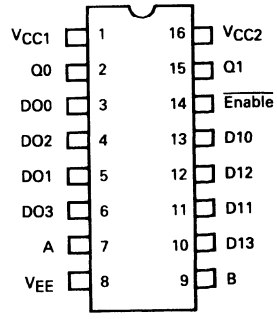
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	B	A	Q0	Q1
H	ϕ	ϕ	L	L
L	L	L	D00	D10
L	L	H	D01	D11
L	H	L	D02	D12
L	H	H	D03	D13

ϕ = Don't Care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established in an ambient temperature of 25°C, while the circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10174 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	80	–	58	73	80	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	4	–	350	–	–	220	–	220	µAdc	4	–	–	–	8	1,16
		14	–	525	–	–	330	–	330		14	–	–	–	8	1,16
	$I_{in\ L}$	4	0.5	–	0.5	–	–	0.3	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	13	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	14	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	13	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	14	–	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{13+15+}	15	1.4	5.0	1.5	3.5	4.7	1.4	5.0	ns	–	–	13	15	8	1,16
	t_{13-15-}	15	1.4	5.0	1.5	3.5	4.7	1.4	5.0		–	–	13			
	t_{7+15-}	15	1.9	6.6	2.0	5.0	6.2	2.1	6.6		11	–	7			
	t_{7-15+}	15	1.9	6.6	2.0	5.0	6.2	2.1	6.6		11	–	7			
	t_{14+15-}	15	1.0	3.3	1.0	2.0	3.1	0.9	3.4		13	–	14			
	t_{14-15+}	15		3.3	1.0	2.0	3.1	0.9	3.4			–	14			
Rise Time (20% to 80%)	t_+	15		3.4	1.1	2.0	3.3	1.1	3.6			–	14			
Fall Time (20% to 80%)	t_-	15		3.4	1.1	2.0	3.3	1.1	3.6			–	14			

MOTOROLA

MC10175

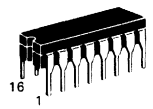
QUINT LATCH

The MC10175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

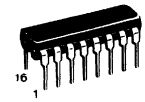
P_D = 400 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to Output)
t_r, t_f = 2.0 ns typ (20%–80%)

QUINT LATCH



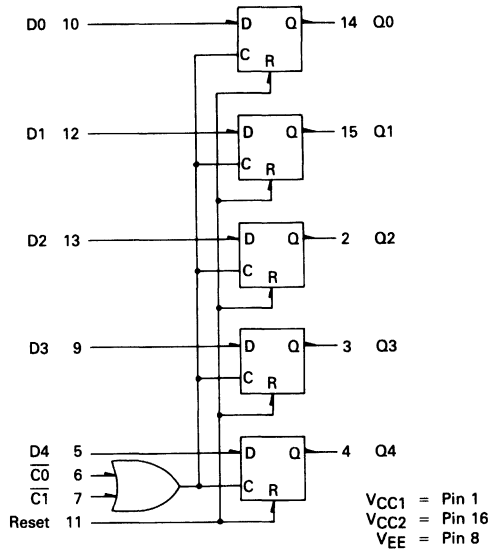
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM

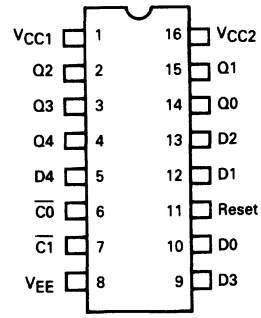


TRUTH TABLE

D	$\overline{C0}$	$\overline{C1}$	Reset	Q_{n+1}
L	L	L	ϕ	L
H	L	L	ϕ	H
ϕ	H	ϕ	L	Q n
ϕ	ϕ	H	L	Q n
ϕ	H	ϕ	H	L
ϕ	ϕ	H	H	L

ϕ = Don't Care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10175L Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	107	–	78	97	–	107	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	6	–	460	–	–	290	–	290	µAdc	6	–	–	–		
		7	–	460	–	–	290	–	290	↓	7	–	–	–	↓	↓
		10	–	460	–	–	290	–	290		10	–	–	–		
		11	–	1000	–	–	650	–	650		11	–	–	–		
Input Leakage Current	I_{inL}	All	0.5	–	0.5	–	–	0.3	–	µAdc	–	①	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	14	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	10	6	–	–	8	1,16
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	6	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	14	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	6,10	–	–	8	1,16
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	6,12	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	14	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	6	10	–	8	1,16
		15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	6	12	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	14	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	6	–	10	8	1,16
		15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	6	–	12	8	1,16
Switching Times											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Data Input	t_{10+14+}	14	1.0	3.6	1.0	–	3.5	1.0	3.6	ns	–	6.7	10	14	8	1,16
	t_{10-14-}	↓	↓	3.6	↓	–	3.5	↓	3.6	↓	–	6,7	10	↓	↓	↓
Clock Input	t_{6-14+}			4.7		–	4.3		4.4		–	7	10,6			
	t_{6-14-}			4.7		–	4.3		4.4		–	7	10,6			
Reset Input	t_{11+4-}	4	1.0	4.0	1.0	–	3.9	1.0	4.2	ns	5	6	7,11	4 ②	8	1,16
	t_{11+14-}	14	1.0	4.0	1.0	–	3.9	1.0	4.2	↓	10	6	7,11	14 ②	8	1,16
Setup Time	t_{setup}	14	2.5	–	2.5	–	–	2.5	–	ns	–	7	6,10	14	8	1,16
Hold Time	t_{hold}	14	1.5	–	1.5	–	–	1.5	–		–	7	6,10			
Rise Time (20 to 80%)	t+	14	1.0	3.6	1.1	–	3.5	1.1	3.7		–	6,7	10			
Fall Time (20 to 80%)	t-	14	1.0	3.6	1.1	–	3.5	1.1	3.7	↓	–	6,7	10	↓	↓	↓

① Individually test each input; apply $V_{IL\ min}$ to pin under test.

② Output latched to high logic state prior to test.

MOTOROLA

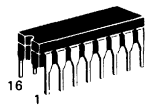
MC10176

HEX "D" MASTER-SLAVE FLIP-FLOP

The MC10176 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.

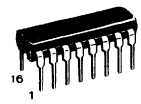
P_D = 460 mW typ/pkg (No Load)
f_{toggle} = 150 MHz (typ)
t_r, t_f = 2.0 ns typ (20%–80%)

HEX "D" MASTER-SLAVE FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 620

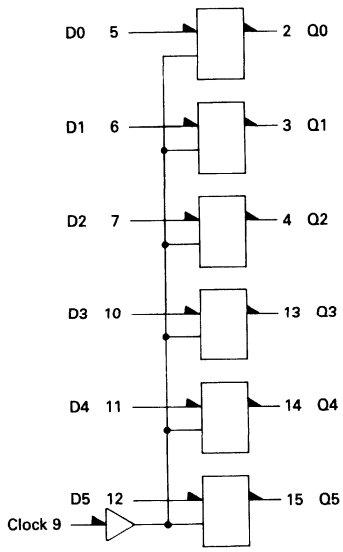
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM



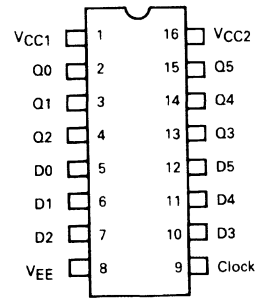
CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H*	L	L
H*	H	H

ϕ = Don't Care
*A clock H is a clock transition from a low to a high state.

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one data input, and the clock input, and for one output. Other inputs and outputs tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10176 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	121	–	88	110	–	121	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	5	–	350	–	–	220	–	220	µAdc	5	–	–	–	8	1,16
		9	–	495	–	–	310	–	310		9	–	–	–	8	1,16
Input Leakage Current	I_{inL}	5	0.5	–	0.5	–	–	0.3	–	µAdc	–	5	–	–	8	1,16
		9	0.5	–	0.5	–	–	0.3	–	µAdc	–	9	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
		15†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	5	–	–	8	1,16
		15†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	12	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		15†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	12	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		15†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	12	8	1,16
Switching Times Clock Input **											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{9+2+}	2	1.6	4.6	1.6	–	4.5	1.6	5.0	ns	–	–	5,9	2	8	1,16
	t_{9+2-}	2	1.6	4.6	1.6	–	4.5	1.6	5.0		–	–				
Rise Time (20 to 80%)	t_{2+}	2	1.0	4.1	1.1	–	4.0	1.1	4.4		–	–				
Fall Time (20 to 80%)	t_{2-}	2	1.0	4.1	1.1	–	4.0	1.1	4.4		–	–				
Setup Time	t_{setup}	2	2.5	–	2.5	–	–	2.5	–	ns	–	–	5.9	2	8	1,16
Hold Time	t_{hold}	2	1.5	–	1.5	–	–	1.5	–	ns	–	–	5,9	2	8	1,16
Toggle Frequency	f_{tog}	2	125	–	125	150	–	125	–	MHz	–	–	–	–	8	1,16

† Output level to be measured after a clock pulse has been applied to C input (pin 9) ⎍⎍ $V_{IH\ max}$ / $V_{IL\ min}$

MOTOROLA

MC10178

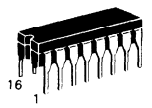
BINARY COUNTER

The MC10178 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight or a divide-by-sixteen function.

Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous "set" or "clear." Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

P_D = 370 mW typ/pkg (No Load)
f_{toggle} = 150 MHz (typ)
t_r, t_f = 2.7 ns typ (20%–80%)

BINARY COUNTER



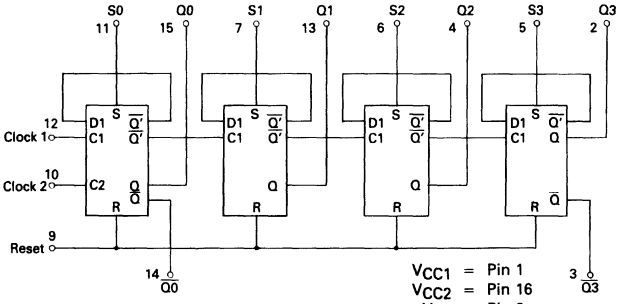
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM



TRUTH TABLE

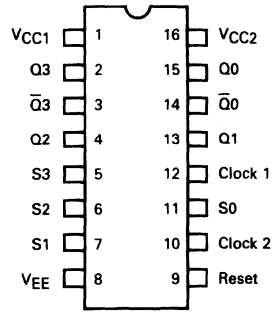
INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
H	L	L	L	L	ϕ	ϕ	L	L	L	L
L	H	H	H	H	ϕ	ϕ	H	H	H	H
L	L	L	L	L	H	ϕ	No Count			
L	L	L	L	L	ϕ	H	No Count			
L	L	L	L	L	**		L	L	L	L
L	L	L	L	L	**		H	L	L	L
L	L	L	L	L	**		L	H	L	L
L	L	L	L	L	**		H	H	L	L
L	L	L	L	L	**		L	L	H	L
L	L	L	L	L	**		H	L	H	L
L	L	L	L	L	**		L	H	H	L
L	L	L	L	L	**		H	H	H	L
L	L	L	L	L	**		L	L	L	H
L	L	L	L	L	**		H	L	L	H
L	L	L	L	L	**		L	H	L	H
L	L	L	L	L	**		H	H	L	H
L	L	L	L	L	**		L	L	H	H
L	L	L	L	L	**		H	L	H	H
L	L	L	L	L	**		L	H	H	H
L	L	L	L	L	**		H	H	H	H

ϕ = Don't Care

** V_{IL} to V_{IH}

Clock transition from V_{IL} to V_{IH} may be applied to C1 or C2 or both for same effect.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10178 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	97	–	–	88	–	97	mAdc	9	–	–	–	8	1,16
Input Current	I_{inH}	12	–	390	–	–	245	–	245	µAdc	12	–	–	–	8	1,16
		11	–	350	–	–	220	–	220	µAdc	11	–	–	–	8	1,16
		9	–	650	–	–	410	–	410	µAdc	9	–	–	–	8	1,16
	I_{inL}	*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	14	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	11	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	14	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	11	–	–	–	8	1,16
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		14	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	11	–	8	1,16
		15	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	9	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,16
		14	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	11	8	1,16
		15	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	9	8	1,16
Switching Times													Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input Propagation Delay	t_{12+15+}	15	1.4	5.0	1.5	3.5	4.8	1.5	5.3	ns	–	–	12	15	8	1,16
	t_{12-13-}	13	1.9	9.4	2.0	6.0	9.2	2.0	9.8		–	–		13		
	t_{12+4-}	4	2.9	12.3	3.0	8.5	12	3.0	12.8		–	–		4		
	t_{12-3+}	3	3.9	14.9	4.0	11	14.5	4.0	15.5		–	–		3		
Rise Time (20 to 80%)	t_{15+}	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0		–	–		15		
Fall Time (20 to 80%)	t_{15-}	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0		–	–		15		
Set Input	t_{11-15+}	15	1.4	5.2	1.5	–	5.0	1.5	5.5	ns	–	–	11	15	8	1,16
Reset Input	t_{9-15+}	15	1.4	5.2	1.5	–	5.0	1.5	5.5	ns	–	–	9	15	8	1,16
Counting Frequency	f_{count}	15	125	–	125	150	–	125	–	MHz	–	–	12	15	8	1,16

*Individually test each input applying V_{IL} to input under test.

MOTOROLA

MC10181

4-BIT ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

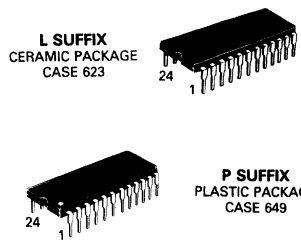
The MC10181 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation.

Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the MC10179, full-carry look-ahead, as a second order look ahead block, the MC10181 provides high speed arithmetic operations on very long words.

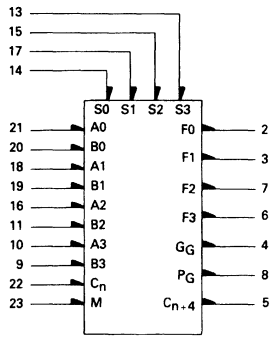
P_D = 600 mW typ/pkg (No Load)
t_{pd} (typ): A1 to F = 6.5 ns
C_n to C_{n+4} = 3.1 ns
A1 to P_G = 5.0 ns
A1 to G_G = 4.5 ns
A1 to C_{n+4} = 5.0

4-BIT ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR



3

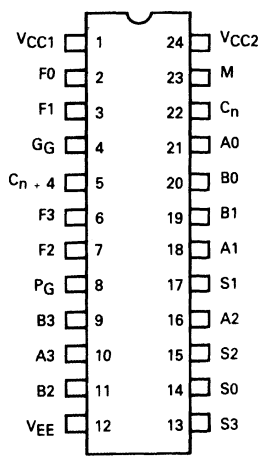
LOGIC DIAGRAM



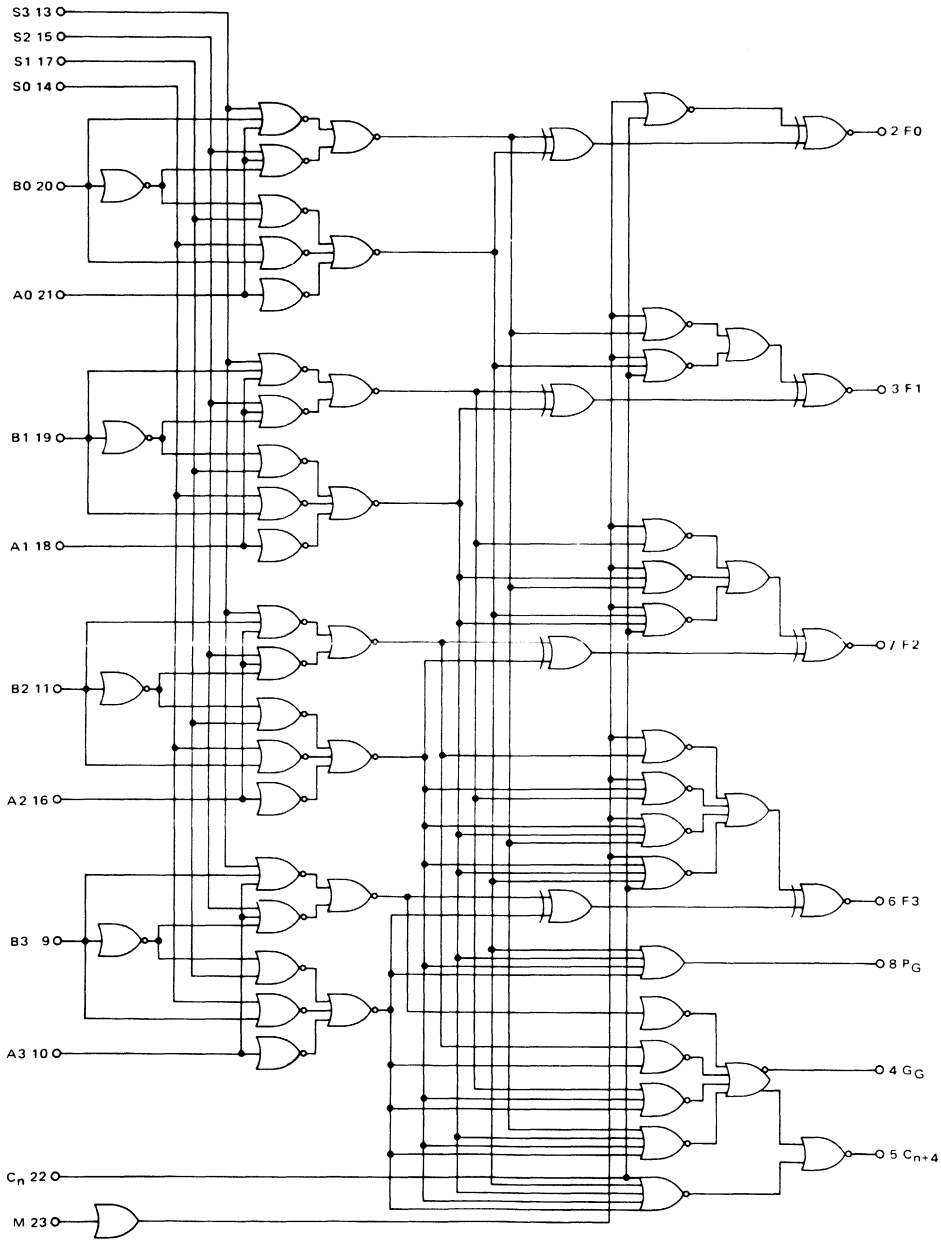
V_{CC1} = Pin 1
V_{CC2} = Pin 24
V_{EE} = Pin 12

Function Select S3	S2	S1	S0	Logic Functions M is High C = D.C. F	Arithmetic Operation M is Low C_n is low F
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A} + \overline{B}$	F = A plus $(A \cdot \overline{B})$
L	L	H	L	$F = \overline{A} + B$	F = A plus (A • B)
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	$F = \overline{A} \cdot \overline{B}$	F = (A + B) plus 0
L	H	L	H	$F = \overline{B}$	F = (A + B) plus $(A \cdot \overline{B})$
L	H	H	L	$F = A \odot B$	F = A plus B
L	H	H	H	$F = A + \overline{B}$	F = A plus (A + B)
H	L	L	L	$F = \overline{A} \cdot B$	F = (A + $\overline{B}$) plus 0
H	L	L	H	$F = A \oplus B$	F = A minus B minus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) plus (A • B)
H	L	H	H	$F = A + B$	F = A plus (A + $\overline{B}$)
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	$F = A \cdot \overline{B}$	F = $(A \cdot \overline{B})$ minus 1
H	H	H	L	$F = A \cdot B$	F = (A • B) minus 1
H	H	H	H	F = A	F = A minus 1

PIN ASSIGNMENT



POSITIVE LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10181 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	12	–	159	–	–	145	–	159	mAdc	–	–	–	–	12	1,24
Input Current	I_{inH}	9	–	**390**	–	–	245	–	**245**	µAdc	9	–	–	–	12	1,24
		10	–	**350**	–	–	220	–	**220**		10	–	–	–		
		11	–	**390**	–	–	245	–	**245**		11	–	–	–		
		13	–	**320**	–	–	200	–	**200**		13	–	–	–		
		14	–	**425**	–	–	265	–	**265**		14	–	–	–		
		15	–	**425**	–	–	265	–	**265**		15	–	–	–		
		16	–	**350**	–	–	220	–	**220**		16	–	–	–		
		17	–	**425**	–	–	265	–	**265**		17	–	–	–		
		18	–	**350**	–	–	220	–	**220**		18	–	–	–		
		19	–	**390**	–	–	245	–	**245**		19	–	–	–		
		20	–	**390**	–	–	245	–	**245**		20	–	–	–		
		21	–	**350**	–	–	220	–	**220**		21	–	–	–		
		22	–	**460**	–	–	290	–	**290**		22	–	–	–		
		23	–	**320**	–	–	200	–	**200**		23	–	–	–		
Input Leakage Current	I_{inL}	9	**0.5**	–	0.5	–	–	**0.3**	–	µAdc	–	9	–	–	12	1,24
		10	–	–	–	–	–	–	–		–	10	–	–		
		11	–	–	–	–	–	–	–		–	11	–	–		
		13	–	–	–	–	–	–	–		–	13	–	–		
		14	–	–	–	–	–	–	–		–	14	–	–		
		15	–	–	–	–	–	–	–		–	15	–	–		
		16	–	–	–	–	–	–	–		–	16	–	–		
		17	–	–	–	–	–	–	–		–	17	–	–		
		18	–	–	–	–	–	–	–		–	18	–	–		
		19	–	–	–	–	–	–	–		–	19	–	–		
		20	–	–	–	–	–	–	–		–	20	–	–		
		21	–	–	–	–	–	–	–		–	21	–	–		
		22	–	–	–	–	–	–	–		–	22	–	–		
		23	–	–	–	–	–	–	–		–	23	–	–		
High Output Voltage	V_{OH}	*	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	*	*	–	–	12	1,24
Low Output Voltage	V_{OL}	*	-2.000	-1.675	-1.990	–	-1.650	-1.920	-1.615	Vdc	*	*	–	–	12	1,24
High Threshold Voltage	V_{OHA}	*	-1.080	—	-0.980	–	—	-0.910	—	Vdc	—	—	**	**	12	1,24
Low Threshold Voltage	V_{OLA}	*	–	-1.655	—	–	-1.630	—	-1.595	Vdc	—	—	**	**	12	1,24

*Test all input-output combinations according to Function Table.

**For threshold level test, apply threshold input level to only one input pin at a time.

Characteristic	Symbol	Input	Output	Conditions†	AC Switching Characteristics							Unit
					-30°C *		+25°C			+85°C *		
					Min	Max	Min	Typ	Max	Min	Max	
Propagation Delay	t++, t--	C_n	C_{n+4}	A0,A1,A2,A3	1.0	5.1	1.1	3.1	5.0	1.1	5.4	ns
Rise Time, Fall Time	t+,t-	C_n	C_{n+4}	A0,A1,A2,A3	1.0	3.2	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++, t+-	C_n	F1	A0	1.7	7.2	2.0	4.5	7.0	2.0	7.5	ns
	t-+, t--	↓	↓	↓	1.7	7.2	2.0	4.5	7.0	2.0	7.5	↓
Rise Time, Fall Time	t+, t-	↓	↓	↓	1.3	5.3	1.5	3.0	5.0	1.5	5.3	↓
Propagation Delay	t++, t+-	A1	F1	—	2.6	10.4	3.0	6.5	10	3.0	10.8	ns
	t-+, t- -	↓	↓		2.6	10.4	3.0	6.5	10	3.0	10.8	↓
Rise Time, Fall Time	t+, t-	↓	↓	—	1.3	5.4	1.5	3.0	5.0	1.5	5.3	↓
Propagation Delay	t++, t--	A1	P_G	S0,S3	1.6	7.0	2.0	5.0	6.5	2.0	7.0	ns
Rise Time, Fall Time	t+, t-	A1	P_G	S0,S3	0.8	3.7	1.1	2.0	3.5	1.1	3.8	ns
Propagation Delay	t++, t--	A1	G_G	A0,A2,A3,C_n	1.1	7.4	2.0	4.5	7.0	1.3	7.7	ns
Rise Time, Fall Time	t+, t-	A1	G_G	A0,A2,A3,C_n	1.2	5.1	1.5	4.0	5.0	1.2	5.3	ns
Propagation Delay	t+-, t-+	A1	C_{n+4}	A0,A2,A3,C_n	1.7	7.3	2.0	5.0	7.0	2.0	7.8	ns
Rise Time, Fall Time	t+, t-	A1	C_{n+4}	A0,A2,A3,C_n	1.0	3.1	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++, t-+	B1	F1	S3, C_n	2.7	11.3	3.0	8.0	11	3.0	11.9	ns
Rise Time, Fall Time	t+, t-	B1	F1	S3,C_n	1.2	5.3	1.5	3.5	5.0	1.5	5.3	ns
Propagation Delay	t++, t--	B1	P_G	S0, A1	1.6	7.7	2.0	6.0	7.5	2.0	8.0	ns
Rise Time, Fall Time	t+, t-	B1	P_G	S0, A1	1.0	3.6	1.1	2.0	3.5	1.1	3.9	ns
Propagation Delay	t++, t--	B1	G_G	S3, C_n	1.7	8.2	2.0	6.0	8.0	2.0	8.6	ns
Rise Time, Fall Time	t+, t-	B1	G_G	S3,C_n	1.4	5.2	1.5	3.0	5.0	1.2	5.4	ns
Propagation Delay	t+-, t-+	B1	C_{n+4}	S3, C_n	1.8	8.2	2.0	6.0	8.0	2.0	8.7	ns
Rise Time, Fall Time	t+, t-	B1	C_{n+4}	S3,C_n	0.9	3.1	1.0	2.0	3.0	1.0	3.2	ns
Propagation Delay	t++, t+-	M	F1	—	2.4	10.3	3.0	6.5	10	3.0	10.8	ns
Rise Time, Fall Time	t+, t-	M	F1	—	1.1	5.1	1.5	4.0	5.0	1.5	5.3	ns
Propagation Delay	t+-, t-+	S1	F1	A1, B1	2.5	10.7	3.0	6.5	10	3.0	10.8	ns
Rise Time, Fall Time	t+, t-	S1	F1	A1, B1	1.0	5.4	1.5	3.0	5.0	1.5	5.4	ns
Propagation Delay	t-+, t+-	S1	P_G	A3, B3	1.7	8.3	2.0	6.0	8.0	2.0	8.4	ns
Rise Time, Fall Time	t+, t-	S1	P_G	A3, B3	0.8	5.1	1.1	3.0	5.0	1.1	5.2	ns
Propagation Delay	t+-, t-+	S1	C_{n+4}	A3, B3	1.6	9.3	2.0	6.0	9.0	2.0	9.9	ns
Rise Time, Fall Time	t+, t-	S1	C_{n+4}	A3, B3	0.9	5.3	1.1	3.0	5.0	1.0	5.2	ns
Propagation Delay	t+-, t-+	S1	G_G	A3, B3	1.5	9.6	2.0	6.0	9.0	1.9	9.7	ns
Rise Time, Fall Time	t+, t-	S1	G_G	A3, B3	0.8	6.2	0.8	3.0	6.0	0.8	6.5	ns

†Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc.
$V_{CC1} = V_{CC2} = +2.0$ Vdc, $V_{EE} = -3.2$ Vdc

*L Suffix Only

3

MOTOROLA

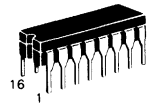
MC10186

HEX "D" MASTER-SLAVE FLIP-FLOP/WITH RESET

The MC10186 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device. **A COMMON RESET IS INCLUDED IN THIS CIRCUIT. RESET ONLY FUNCTIONS WHEN CLOCK IS LOW.**

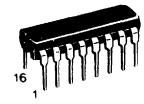
P_D = 460 mW typ/pkg (No Load)
f_{toggle} = 150 MHz (typ)
t_r, t_f = 2.0 ns typ (20%–80%)

HEX "D" MASTER-SLAVE FLIP-FLOP/WITH RESET



L SUFFIX
CERAMIC PACKAGE
CASE 620

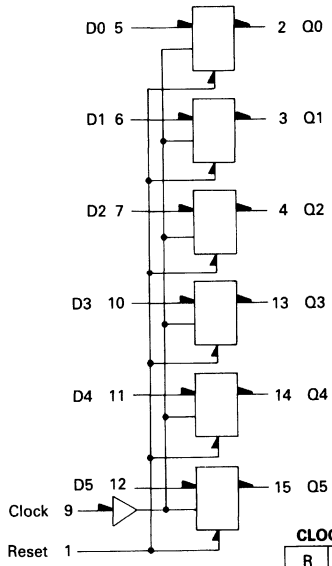
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM



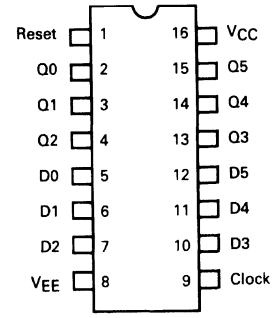
V_{CC} = Pin 16
V_{EE} = Pin 8

CLOCKED TRUTH TABLE

R	C	Q	Q_{n+1}
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H
H	L	ϕ	L

ϕ = Don't Care
*A clock H is a clock transition from a low to a high state.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one data input, the clock input, and the reset input, and for one output. Other inputs and outputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-1.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10186 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	121	–	88	110	–	121	mAdc	–	–	–	–	8	16
Input Current	I_{inH}	5	–	350	–	–	220	–	220	μAdc	5	–	–	–	8	16
		9	–	495	–	–	310	–	310	↓	9	–	–	–	8	16
		1	–	920	–	–	575	–	575	↓	1	–	–	–	8	16
Input Leakage Current	I_{inL}	5	0.5	–	0.5	–	–	0.3	–	μAdc	–	5	–	–	8	16
Logic "1" Output Voltage	V_{OH}	2†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	16
		15†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	–	–	–	8	16
Logic "0" Output Voltage	V_{OL}	2†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	5	–	–	8	16
		15†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	12	–	–	8	16
Logic "1" Threshold Voltage	V_{OHA}	2†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	16
		15†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	12	–	8	16
Logic "0" Threshold Voltage	V_{OLA}	2†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	16
		15†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	12	8	16
Switching Times											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay (50 Ω Load)	t_{1+3-}	3	1.6	4.6	1.6	2.5	4.5	1.6	5.0	ns	6	–	1,9	3	8	16
	t_{1+4-}	4	↓	↓	↓	2.5	↓	↓	↓	↓	7	–	1,9	4	↓	↓
	t_{g+2+}	2				3.5					–	–	5,9	2		
	t_{g+2-}	2				3.5					–	–	↓	↓		
Rise Time (20 to 80%)	t_{2+}	2	1.0	4.1	1.1	1.8	4.0	1.1	4.4		–	–				
Fall Time (20 to 80%)	t_{2-}	2	1.0	4.1	1.1	1.8	4.0	1.1	4.4	↓	–	–	↓	↓	↓	↓
Setup Time	t_{setup}	2	2.5	–	2.5	2.5	–	2.5	–	ns	–	–	5,9	2	8	16
Hold Time	t_{hold}	2	1.5	–	1.5	-1.5	–	1.5	–	ns	–	–	5,9	2	8	16
Toggle Frequency	f_{tog}	2	125	–	125	150	–	125	–	MHz	–	–	–	–	8	16

†Output level to be measured after a clock pulse. V_{IL} ⟋ V_{IH} appears at clock input (pin 9).

MOTOROLA

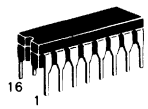
MC10188

HEX BUFFER WITH ENABLE

The MC10188 is a high-speed hex buffer with a common Enable input. When Enable is in the high state, all outputs are in the low state. When Enable is in the low state, the outputs take the same state as the inputs.

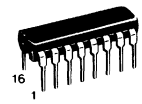
Power Dissipation = 180 mW typ/pkg (No Load)
Propagation Delay = 2.0 ns typ (B - Q)
2.5 ns typ (A - Q)

HEX BUFFER WITH ENABLE



L SUFFIX
CERAMIC PACKAGE
CASE 620

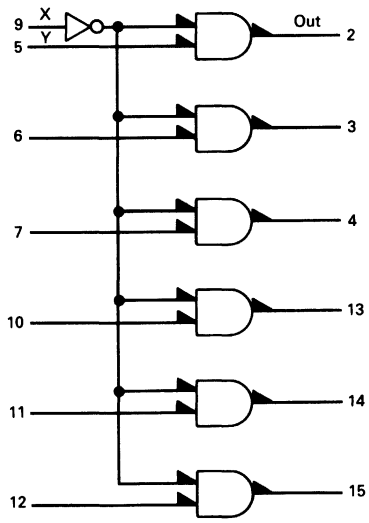
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM

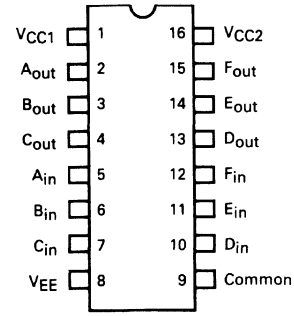


TRUTH TABLE

Inputs		Output
X	Y	OUT
L	L	L
L	H	H
H	L	L
H	H	L

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for one set of conditions. Complete testing according to truth table.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	—	46	—	42	—	46	mAdc	—	—	—	—	8	1,16
Input Current	I_{inH}	5	—	425	—	265	—	265	μAdc	5	—	—	—	8	1,16
	I_{inH}	9	—	460	—	290	—	290	μAdc	9	—	—	—	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	5	—	—	—	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	—	9	—	—	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	—	-0.980	—	-0.910	—	Vdc	—	—	5	—	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	—	-1.655	—	-1.630	—	-1.595	Vdc	—	—	—	5	8	1,16
Switching Times (50 Ω Load)									ns			Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{PHL} t_{PLH}														
Enable		2	1.1	3.9	1.1	3.5	1.1	3.9		—	—	9	2	8	1, 16
Data		2	1.0	3.3	1.0	2.9	1.0	3.3		—	—	5			
Rise Time, Fall Time (20% to 80%)	t_{TLH}, t_{THL}	2	1.1	3.7	1.1	3.3	1.1	3.7		—	—				

MOTOROLA

MC10189

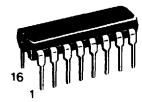
HEX INVERTER WITH ENABLE

The MC10189 provides a high-speed Hex Inverter with a common Enable input. The hex inverting function is provided when Enable is in the low state. When Enable is in the high state all outputs are low.

P_D = 200 MW typ/pkg (No Load)
t_{pd} = 2.0 ns (Y-Q)
= 2.5 ns (X-Q)

HEX INVERTER WITH ENABLE

L SUFFIX
CERAMIC PACKAGE
CASE 620

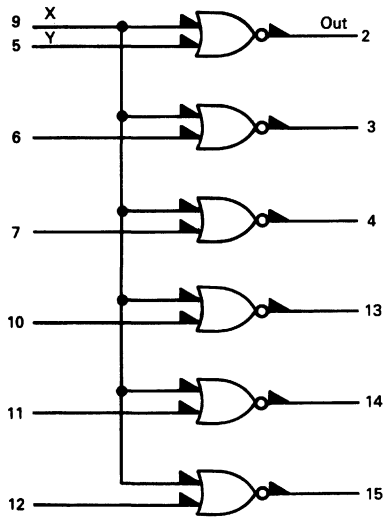


P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM

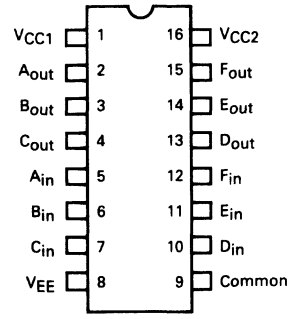


TRUTH TABLE

Inputs		Output
X	Y	OUT
L	L	H
L	H	L
H	L	L
H	H	L

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for one set of conditions. Complete testing according to truth table.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	—	44	—	40	—	44	mAdc	—	—	—	—	8	1,16
Input Current	I_{inH}	5	—	425	—	265	—	265	μAdc	5	—	—	—	8	1,16
	I_{inH}	9	—	890	—	555	—	555	μAdc	9	—	—	—	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	Vdc	—	5	—	—	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	Vdc	9	—	—	—	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	—	-0.980	—	-0.910	—	Vdc	—	—	—	5	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	—	-1.655	—	-1.630	—	-1.595	Vdc	—	—	5	—	8	1,16
Switching Times (50 Ω Load) Propagation Delay	t_{PHL}, t_{PLH}								ns			Pulse In	Pulse Out	-3.2 V	+2.0 V
Enable		2	1.1	3.9	1.1	3.5	1.1	3.9		—	—	9	2	8	1, 16
Data		2	1.0	3.3	1.0	2.9	1.0	3.3		—	—	5			
Rise Time, Fall Time (20% to 80%)	t_{TLH}, t_{THL}	2	1.1	3.7	1.1	3.3	1.1	3.7		—	—				

MOTOROLA

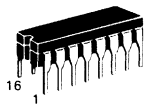
MC10190

QUAD MST TO MECL 10,000 TRANSLATOR

The MC101090 is a quad translator for interfacing from IBM MST-type logic signals to standard MECL 10,000 logic levels. This circuit features differential inputs for high noise environments or may be used with single ended lines by tieing one of the inputs to ground. Since the MC10190 is designed to accept signals centered around ground, it is a useful interface element for many communication systems. When pin 9 is connected to V_{CC} the circuit becomes a line receiver for MECL signals. The outputs go to a low level whenever the inputs are left floating.

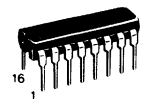
P_D = 215 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

QUAD MST TO MECL 10,000 TRANSLATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

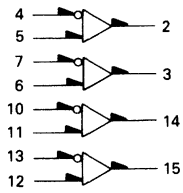
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

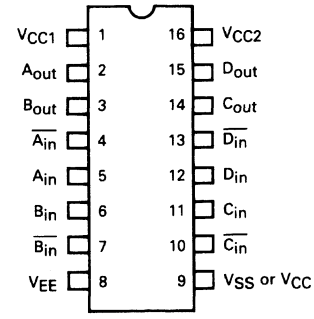
3

LOGIC DIAGRAM



V_{CC1} = Pin1
V_{CC2} = Pin 16
V_{EE} = Pin 8
V_{SS} = Pin 9 Translator
V_{CC} = Pin 9 Receiver

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

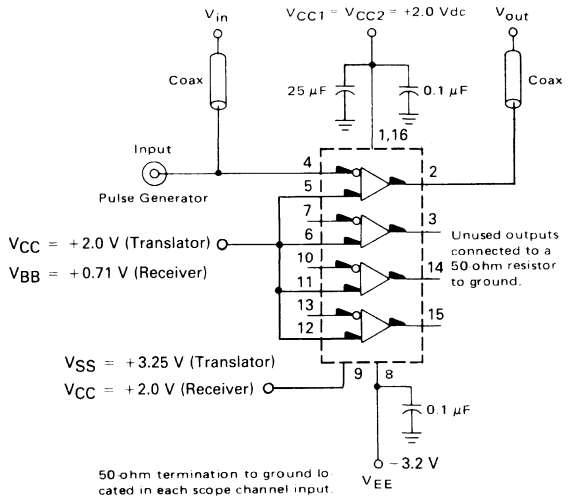
@ Test Temperature	TEST VOLTAGE VALUES (Volts)											
	V_{IHmax}	$V_{IL\,min}$	V_{ILAmin}	V_{ILAmax}	V_{IHM}*	V_{ILM}*	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{SS}*	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	+0.374	-0.523	+0.186	-0.850	-1.486	-2.53	+1.25	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	+0.440	-0.490	+0.186	-0.850	-1.486	-2.53	+1.25	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	+0.548	-0.454	+0.186	-0.850	-1.486	-2.53	+1.25	-5.2

Characteristic	Symbol	Pin Under Test	MC10190 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	$V_{IL\,min}$	V_{ILAmin}	V_{ILAmax}	V_{IHM}*	V_{ILM}*	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{SS}*	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	57	–	41	52	–	57	mAdc	4,6,10,12	5,7,11,13	–	–	–	–	–	–	–	–	9	8	1,16
	I_{CC}	9	–	27	–	22	27	–	27	mAdc	4,6,10,12	5,7,11,13	–	–	–	–	–	–	–	–	9	8	1,16
Input Current	I_{inH}	4	–	70	–	–	45	–	45	μAdc	4	5	–	–	–	–	–	–	–	–	9	8	1,16
		5	–	70	–	–	45	–	45	μAdc	5	4	–	–	–	–	–	–	–	–	9	8	1,16
Reverse Leakage Current	I_{CBO}	4	–	1.5	–	–	1.0	–	1.0	μAdc	–	–	–	–	–	–	–	–	–	–	9	4,8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	4	–	–	–	–	–	–	–	–	–	8	1,9,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	5	4	–	–	–	–	9	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	5	–	–	–	–	–	–	–	–	–	8	1,9,16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	4	5	–	–	–	–	9	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	4	–	–	–	–	–	–	–	8	1,9,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	4	5	–	–	–	–	–	–	–	8	1,9,16
Common Mode Rejection Test	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	–	–	5	4	–	–	–	8	1,9,16
		2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	–	–	–	–	5	4	–	8	1,9,16
	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	–	–	4	5	–	–	–	8	1,9,16
		2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	–	–	–	–	4	5	–	8	1,9,16
Switching Times (50 ohm load)													Pulse In	Pulse Out							+3.25 V	-3.2 V	+2.0 V
Propagation Delay	t_{4-2+}	2	1.0	3.9	1.0	2.5	3.7	1.0	4.1	ns	–	–	4	2	–	–	–	–	–	–	9	8	1,5,6,11,12
	t_{4+2-}	2	1.0	3.9	1.0	2.5	3.7	1.0	4.1	ns	–	–	4	2	–	–	–	–	–	–	9	8	1,5,6,11,12
Rise Time (20% to 80%)	t_{2+}	2	1.1	4.5	1.5	2.0	4.3	1.1	4.7	ns	–	–	4	2	–	–	–	–	–	–	9	8	1,5,6,11,12
Fall Time (20% to 80%)	t_{2-}	2	1.1	4.5	1.5	2.0	4.3	1.1	4.7	ns	–	–	4	2	–	–	–	–	–	–	9	8	1,5,6,11,12

*V_{SS} = IBM Supply Voltage.
V_{IHM} = Input Logic "1" for IBM levels.
V_{ILM} = Input Logic "0" for IBM levels.
V_{IHH} = Input logic "1" level shifted positive for common mode rejection tests.
V_{ILH} = Input logic "0" level shifted positive for common mode rejection tests.
V_{IHL} = Input logic "1" level shifted negative for common mode rejection tests.
V_{ILL} = Input logic "0" level shifted negative for common mode rejection tests.

3

SWITCHING TIME TEST CIRCUIT



50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

MOTOROLA

MC10192

QUAD BUS DRIVER

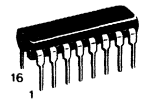
The MC10192 contains four line drivers with complementary outputs. Each driver has a Data (D) input and shares an Enable ($\overline{E}$) input with another driver. The two driver outputs are the uncommitted collectors of a pair of NPN transistors operating as a current switch. Each driver accepts 10K MECL input signals and provides a nominal signal swing of 800 mV across a 50 Ω load at each output collector. Outputs can drive higher values of load resistance, provided that the combination of I_R drop and load return voltage V_{LR} does not cause an output collector to go more negative than −2.4 V with respect to V_{CC}. To avoid output transistor breakdown, the load return voltage should not be more positive than +5.5 V with respect to V_{CC}. When the $\overline{E}$ input is high, both output transistors of a driver are nonconducting. When not used, the $\overline{E}$ inputs, as well as the D inputs, may be left open.

- Open Collector Outputs Drive Terminated Lines or Transformers
- 50 kΩ Input Pulldown Resistors on All Inputs (Unused Inputs May Be Left Open)
- Power Dissipation = 575 mW typ/pkg (No Load)
- Propagation Delay = 3.5 ns typ ($\overline{E}$ — Output)
  3.0 ns typ (D — Output)

QUAD BUS DRIVER

L SUFFIX
CERAMIC PACKAGE
CASE 620

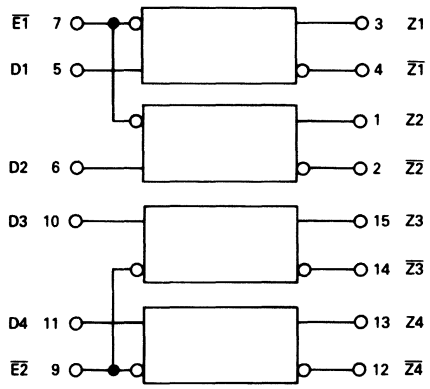
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM



TRUTH TABLE

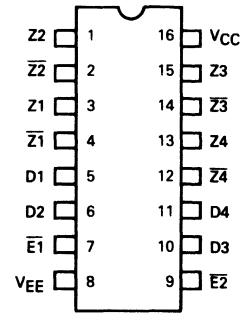
Inputs		Output	
$\overline{E}$	D	Z	$\overline{Z}$
H	X	H	H
L	H	H	L
L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

V_{CC} = Pin 16
V_{EE} = Pin 8

Note: Unused outputs must be terminated to V_{CC} for proper operation.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to ground volts. Test procedures are shown for one set of conditions. Complete testing according to truth table.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	—	154	—	140	—	154	mAdc	—	—	—	—	8	16
Input Current	I_{inH}	5	—	350	—	220	—	220	µAdc	5	—	—	—	8	16
	I_{inL}	5	0.5	—	0.5	—	0.3	—	µAdc	—	5	—	—	8	16
Logic "1" Output Current High	I_{OH}	2	—	—	—	2.0	—	—	mAdc	—	5,6,10,11	—	—	8	16
Logic "0" Output Current Low	I_{OL}	2	13.5	+18	14	18	14	19	mAdc	5,6,10,11	—	—	—	8	16
Logic "1" Output Current High	I_{OHC}	2	—	2.0	—	2.0	—	2.0	mAdc	—	5,7,9,10,11	—	6	8	16
Logic "0" Output Current Low	I_{OLC}	2	13.5	—	14	—	14	—	mAdc	5,10,11	7,9	6	—	8	16
Logic "0" Output Sink Current Low	I_{OS}	2	13.3	—	13.9	—	13.3	—	mAdc	5,6,10,11	—	—	—	8	16
Load Return Voltage Absolute Max Rating (Note 1)	V_{LR}			5.5		5.5		5.5	Volts	—	—	—	—	8	16
Output Voltage Low (Note 2)	V_{OLS}				−2.4				Volts	—	—	—	—	8	16
Switching Times (50 Ω Load) Propagation Delay	t_{PHL} t_{PLH}								ns						
E to Output		—	—	—	2.0	6.0	—	—							
D to Output		—	—	—	1.5	4.5	—	—							
Rise Time, Fall Time (20% to 80%)	t_{TLH} t_{THL}	—	—	—	—	3.3	—	—							

NOTE 1 The 5.5 V value is a maximum rating, do not exceed. A 270 OHM resistor will prevent output transistor breakdown.
NOTE 2 Limitations of load resistor and load return voltage combinations. Refer to page 1 description.

MOTOROLA

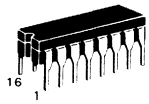
MC10195

HEX INVERTER/BUFFER

The MC10195 is a Hex Buffer Inverter which is built using six EXCLUSIVE NOR gates. There is a common input to these gates which when placed low or left open allows them to act as inverters. With the common input connected to a high logic level the MC10195 is a hex buffer, useful for high fanout clock driving and reducing stub lengths on long bus lines.

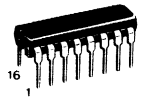
P_D = 200 mW typ/pkg (No Load)
t_{pd} = 2.8 ns typ (B–Q)
t_{pd} = 3.8 ns typ (A–Q)
t_r, t_f = 2.5 ns typ (20%–80%)

HEX INVERTER/BUFFER



L SUFFIX
CERAMIC PACKAGE
CASE 620

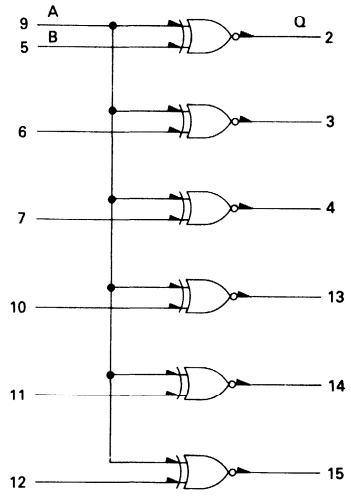
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM

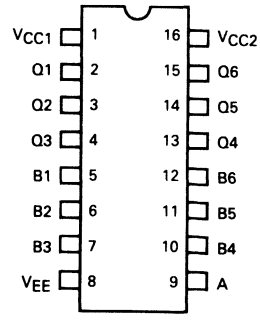


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

Inputs		Output
A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10195 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	54	–	39	49	–	54	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	5	–	425	–	–	265	–	265	μAdc	5	–	–	–	8	1,16
		9	–	460	–	–	290	–	290	μAdc	9	–	–	–	8	1,16
	I_{inL}	5	0.5	–	0.5	–	–	0.3	–	μAdc	–	5	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	5	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,16
Switching Time (50 ohm load)													Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{5+2-}	2	1.1	4.2	1.1	2.8	4.0	1.1	4.4	ns	–	–	5	2	8	1,16
	t_{7-4+}	4	↓	↓	↓	↓	↓	↓	↓		–	–	7	4	↓	↓
	t_{10+13+}	13	↓	↓	↓	↓	↓	↓	↓		–	–	10	13	↓	↓
	t_{11-14-}	14	↓	↓	↓	↓	↓	↓	↓		–	–	11	14	↓	↓
	t_{9-14}	14	1.1	5.2	1.1	3.8	5.0	1.1	5.4				9	14	↓	↓
Rise Time (20% to 80%)	t_{2+}	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0			–	5	2	↓	↓
Fall Time (20% to 80%)	t_{2-}	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0	↓	–	–	5	2	↓	↓

MOTOROLA

MC10197

HEX "AND" GATE

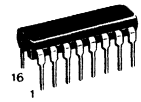
The MC10197 provides a high speed hex AND function with strobe capability.

P_D = 200 mW typ/pkg (No Load)
t_{pd} = 2.8 ns typ (B–Q)
t_{pd} = 3.8 ns typ (A–Q)
t_r, t_f = 2.5 ns typ (20%–80%)

HEX "AND" GATE

L SUFFIX
CERAMIC PACKAGE
CASE 620

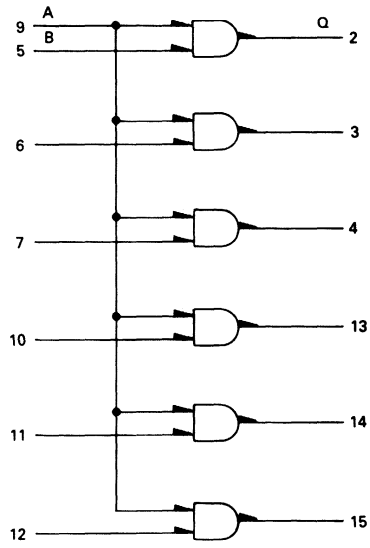
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

3

LOGIC DIAGRAM

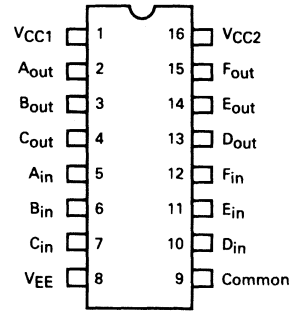


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

Inputs		Output
A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10197 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	54	–	39	49	–	54	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	5	–	425	–	–	265	–	265	μAdc	5	–	–	–	8	1,16
		9	–	460	–	–	290	–	290	μAdc	9	–	–	–	8	1,16
	I_{inL}	5	0.5	–	0.5	–	0.3	–	–	μAdc	–	5	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5,9	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9	–	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9	–	–	5	8	1,16
Switching Time (50 ohm load)												+1.11Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{5+2+}	2	1.1	4.2	1.1	2.8	4.0	1.1	4.4	ns	–	9	5	2	8	1,16
	t_{g+2+}	2	1.1	5.3	1.1	3.5	5.0	1.1	5.5		–	5	9			
Rise Time (20% to 80%)	t_{2+}	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0			9	5			
Fall Time (20% to 80%)	t_{2-}	2	1.1	4.7	1.1	2.5	4.5	1.1	5.0		–	9	5			

MOTOROLA

MC10198

MONOSTABLE MULTIVIBRATOR

MONOSTABLE MULTIVIBRATOR

The MC10198 is a retriggerable monostable multivibrator. Two enable inputs permit triggering on any combination of positive or negative edges as shown in the accompanying table. The trigger input is buffered by Schmitt triggers making it insensitive to input rise and fall times.

The pulse width is controlled by an external capacitor and resistor. The resistor sets a current which is the linear discharge rate of the capacitor. Also, the pulse width can be controlled by an external current source or voltage (see applications information).

For high-speed response with minimum delay, a hi-speed input is also provided. This input bypasses the internal Schmitt triggers and the output responds within 2 nanoseconds typically.

Output logic and threshold levels are standard MECL 10,000. Test conditions are per Table 2. Each "Precondition" referred to in Table 2 is per the sequence of Table 1.

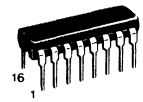
P_D = 415 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ Trigger Input to Q
2.0 ns typ Hi-Speed Input to Q

Min Timing Pulse Width	PW_{Qmin}	10 ns typ[1]
Max Timing Pulse Width	PW_{Qmax}	>10 ns typ[2]
Min Trigger Pulse Width	PW_T	2.0 ns typ
Min Hi-Speed Trigger Pulse Width	PW_{HS}	3.0 ns typ
Enable Setup Time	t_{set}	1.0 ns typ
Enable Hold Time	t_{hold}	1.0 ns typ

[1] C_{Ext} = 0 (Pin 4 open), R_{Ext} = 0 (Pin 6 to V_{EE})
[2] C_{Ext} = 10 µF, R_{Ext} = 2.7 kΩ

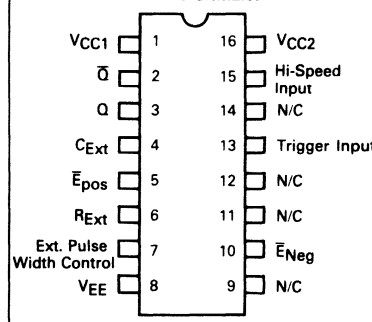
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



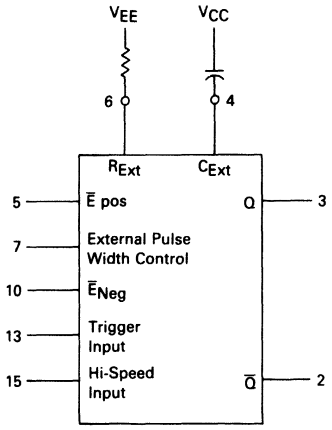
FN SUFFIX
PLCC
CASE 775

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

LOGIC DIAGRAM



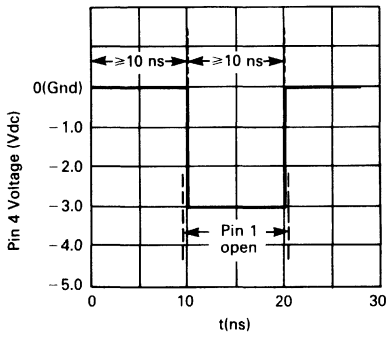
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

INPUT		OUTPUT
$\bar{E}_{Pos}$	$\bar{E}_{Neg}$	
L	L	Triggers on both positive & negative input slopes
L	H	Triggers on positive input slope
H	L	Triggers on negative input slope
H	H	Trigger is disabled

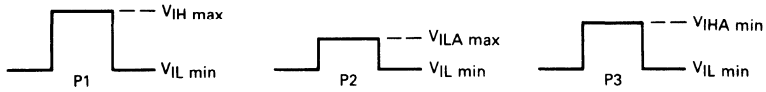
3

TABLE 1 — PRECONDITION SEQUENCE



1. At t = 0 a.) Apply V_{IHmax} to Pin 5 and 10.
   b.) Apply V_{ILmin} to Pin 15.
   c.) Ground Pin 4.
2. At t ≥10 ns a.) Open Pin 1.
   b.) Apply −3.0 Vdc to Pin 4.
   Hold these conditions for ≥10 ns.
3. Return Pin 4 to Ground and perform test as indicated in Table 2.

TABLE 2 — CONDITIONS FOR TESTING OUTPUT LEVELS
(See Table 1 for Precondition Sequence)



Pins 1, 16 = V_{CC} = Ground
Pins 6, 8 = V_{EE} = 5.2 Vdc
Outputs loaded 50 Ω to −2.0 Vdc

Test	P.U.T.	Pin Conditions 5	10	13	15
Precondition					
V_{OH}	2			V_{IL} min	
V_{OH}	3			P1	
Precondition					
V_{OL}	3			V_{IL} min	
V_{OL}	2			P1	
Precondition					
V_{OHA}	2				V_{ILA} max
V_{OHA}	3				V_{IHA} min
Precondition					
V_{OHA}	2			V_{IL} min	
V_{OHA}	3			P3	
Precondition					
V_{OHA}	2			P2	
V_{OHA}	3			P3	
Precondition					
V_{OHA}	2		V_{IH} max	P2	
V_{OHA}	3		V_{IH} max	P3	
Precondition					
V_{OHA}	2		V_{IH} max	P1	
V_{OHA}	3		V_{IH} max	P1	

Test	P.U.T.	Pin Conditions 5	10	13	15
Precondition					
V_{OHA}	2		V_{IHA} min	P1	
V_{OHA}	3		V_{ILA} max	P1	
Precondition					
V_{OLA}	3				V_{ILA} max
V_{OLA}	2				V_{IHA} min
Precondition					
V_{OLA}	2			V_{IL} min	
V_{OLA}	3			V_{IL} min	
Precondition					
V_{OLA}	3			P2	
V_{OLA}	2			P3	
Precondition					
V_{OLA}	3		V_{IH} max	P2	
V_{OLA}	2		V_{IH} max	P3	
Precondition					
V_{OLA}	3	V_{IHA} min	V_{IH} max	P1	
V_{OLA}	2	V_{ILA} max	V_{IH} max	P1	
Precondition					
V_{OLA}	3	V_{IH} max	V_{IHA} min	P1	
V_{OLA}	2	V_{IH} max	V_{ILA} max	P1	

ELECTRICAL CHARACTERISTICS

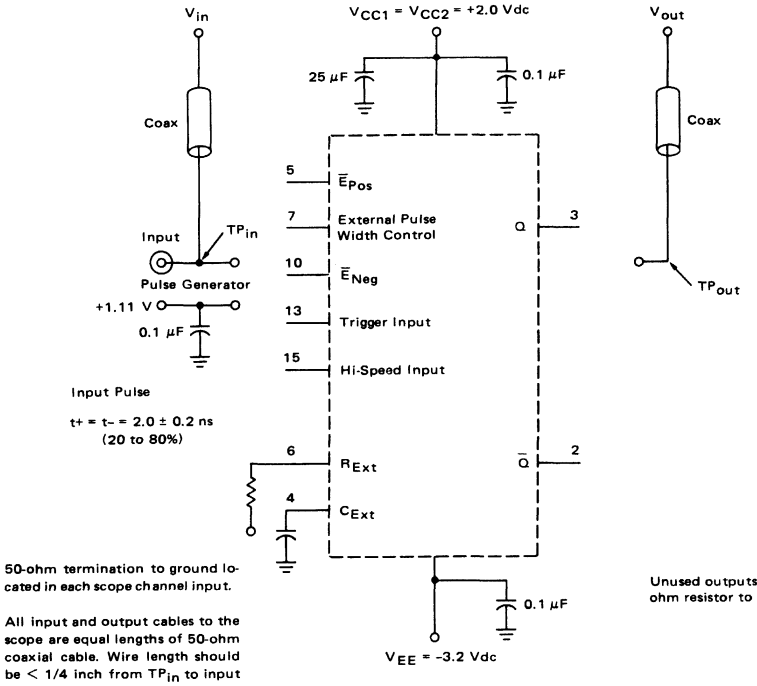
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only selected inputs and outputs. Other inputs and outputs tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10198 TEST LIMITS -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	110	–	80	100	–	110	mAdc	–	–	–	–	6,8	1,4,16
Input Current	I_{inH}	5,10	–	415	–	–	260	–	260	µAdc	5,10	–	–	–	6,8	1,4,16
		13	–	350	–	–	220	–	220		13	–	–	–		
		15	–	560	–	–	350	–	350		15	–	–	–		
	I_{inL}	5	0.5	—	0.5	–	–	0.3	—	µAdc	–	5	–	–		
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	13 ④	13	–	–	6,8	1,4,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc			–	–	6,8	1,4,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	13 ④	–	–	–	6,8	1,4,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc		13	–	–	6,8	1,4,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–		–	15	6,8	1,16,4
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–		15		6,8	1,16,4
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	15	–	6,8	1,16,4
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	15	6,8	1,16,4
Switching Times											1.11 Vdc		Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Trigger Input	t_{T+Q+}	3	2.5	6.5	2.5	4.0	5.5	2.5	6.5	ns	10	–	13	3	6,8	1,16,4
	t_{T-Q+}	3	2.5	6.5	2.5	4.0	5.5	2.5	6.5		5	–	13	3		
Hi Speed Trigger Input	t_{HS+Q+}	3	1.5	3.2	1.5	2.0	2.8	1.5	3.2		–	–	15	3		
Minimum Timing Pulse Width	PW_{Qmin}	3	–	–	–	10.0	–	–	–		–	–	–	②		
Maximum Timing Pulse Width	PW_{Qmax}	3	–	–	–	10	–	–	–	ms	–	–	–	③		
Minimum Trigger Pulse Width	PW_T	3	–	–	–	2.0	–	–	–	ns	–	–	13	3		
Minimum Hi-Speed Trigger Pulse Width	PW_{HS}	3	–	–	–	3.0	–	–	–		–	–	15	3		
Rise Time (20% to 80%)		3	1.5	4.0	1.5	—	3.5	1.5	4.0							
Fall Time (20% to 80%)		3	1.5	4.0	1.5	—	3.5	1.5	4.0							
Enable Setup Time	$t_{setup(E)}$	3	–	–	–	1.0	–	–	–		–	–	5	3		
Enable Hold Time	$t_{hold(E)}$	3	–	–	–	1.0	–	–	–		–	–	5	3		

Notes: ① The monostable is in the timing mode at the time of this test.
② C_{EXT} = 0 (Pin 4 open)
R_{EXT} = 0 (Pin 6 tied to V_{EE})
③ C_{EXT} = 10 µF (Pin 4)
R_{EXT} = 2.7 k (Pin 6)
④ 

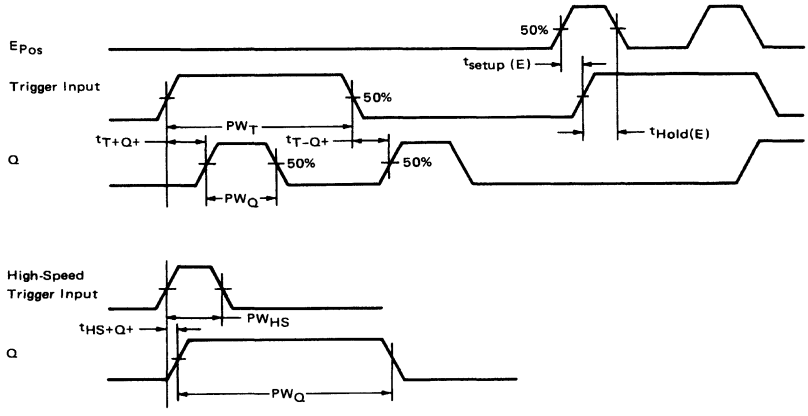
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are tied to a 50-ohm resistor to ground.



APPLICATIONS INFORMATION

Circuit Operation:

1. PULSE WIDTH TIMING — The pulse width is determined by the external resistor and capacitor. The MC10198 also has an internal resistor (nominally 284 ohms) that can be used in series with R_{Ext}. Pin 7, the external pulse width control, is a constant voltage node (−3.60 V nominally). A resistance connected in series from this node to V_{EE} sets a constant timing current I_T. This current determines the discharge rate of the capacitor:

$$I_T = C_{Ext} \frac{\Delta V}{\Delta T}$$

where

ΔT = pulse width
ΔV = 1.9 V change in capacitor voltage

Then:

$$\Delta T = C_{Ext} \frac{1.9\ V}{I_T}$$

If $R_{Ext} + R_{Int}$ are in series to V_{EE}:

$I_T = [(-3.60\ V) - (-5.2\ V)] \div [R_{Ext} + 284\ \Omega]$
$I_T = 1.6\ V/(R_{Ext} + 284)$

The timing equation becomes:

$\Delta T = [(C_{Ext})(1.9\ V)] \div [1.6\ V/(R_{Ext} + 284)]$
$\Delta T = C_{Ext}\ (R_{Ext} + 284)\ 1.19$

where ΔT = Sec
R_{Ext} = Ohms
C_{Ext} = Farads

FIGURE 1 —

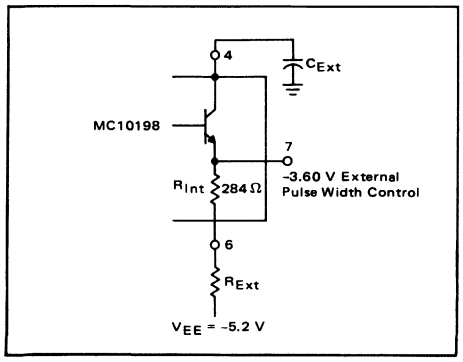


Figure 2 shows typical curves for pulse width versus C_{Ext} and R_{Ext} (total resistance includes R_{Int}). Any low leakage capacitor can be used and R_{Ext} can vary from 0 to 16 k-ohms.

2. TRIGGERING — The $\overline{E}_{Pos}$ and $\overline{E}_{Neg}$ inputs control the trigger input. The MC10198 can be programmed to trigger on the positive edge, negative edge, or both. Also, the trigger input can be totally disabled. The truth table is shown on the first page of the data sheet.

The device is totally retriggerable. However, as duty cycle approaches 100%, pulse width jitter can occur due to the recovery time of the circuit. Recovery time is basically dependent on capacitance C_{Ext}. Figure 3 shows typical recovery time versus capacitance at I_T = 5 mA.

FIGURE 2 — TIMING PULSE WIDTH versus C_{Ext} and R_{Ext}

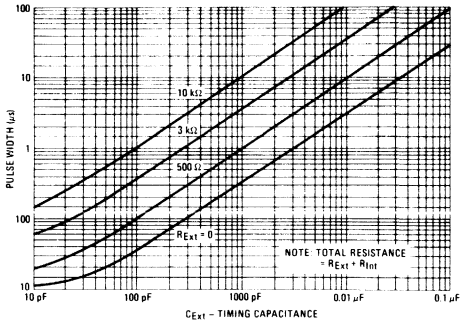
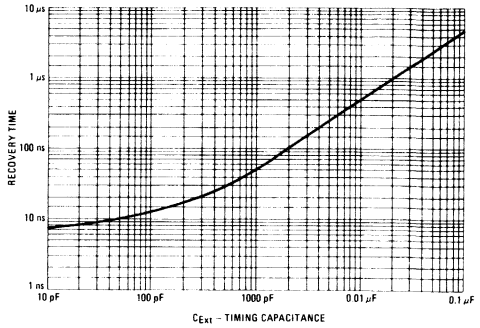


FIGURE 3 — RECOVERY TIME versus C_{Ext} @ I_T = 5 mA

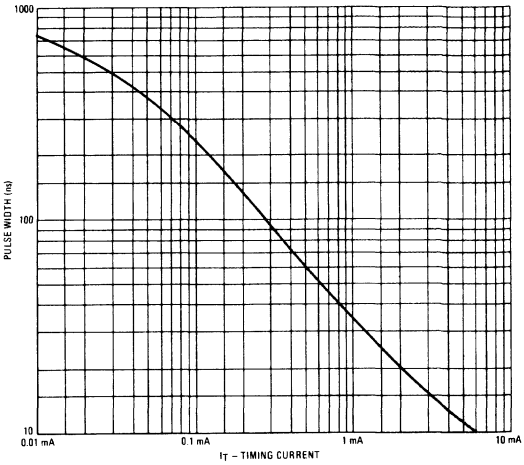


3. HI-SPEED INPUT — This input is used for stretching very narrow pulses with minimum delay between the output pulse and the trigger pulse. The trigger input should be disabled when using the high-speed input. The MC10198 triggers on the rising edge, using this input, and input pulse width should narrow, typically less than 10 nanoseconds.

USAGE RULES:

1. Capacitor lead lengths should be kept very short to minimize ringing due to fast recovery rise times.
2. The $\overline{E}$ inputs should not be tied to ground to establish a high logic level. A resistor divider or diode can be used to establish a −0.7 to −0.9 voltage level.
3. For optimum temperature stability; 0.5 mA is the best timing current I_T. The device is designed to have a constant voltage at the EXTERNAL PULSE WIDTH CONTROL over temperature at this current value.
4. Pulse Width modulation can be attained with the EXTERNAL PULSE WIDTH CONTROL. The timing current can be altered to vary the pulse width. Two schemes are:
   (a) The internal resistor is not used. A dependent current source is used to set the timing current as shown in Figure 4. A graph of pulse width versus timing current (C_{Ext} = 13 pF) is shown in Figure 5.

FIGURE 5 — PULSE WIDTH versus I_T @ C_{Ext} = 13 pF



   (b) A control voltage can also be used to vary the pulse width using an additional resistor (Figure 6). The current (I_T + I_C) is set by the voltage drop across R_{Int} + R_{Ext}. The control current IC modifies I_T and alters the pulse width. Current I_C should never force I_T to zero. R_C typically 1 kΩ.

FIGURE 4 —

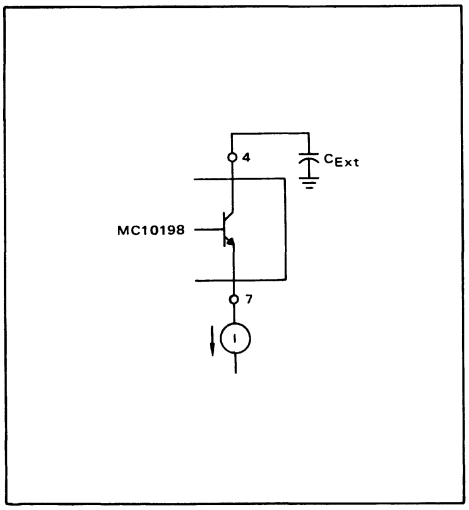
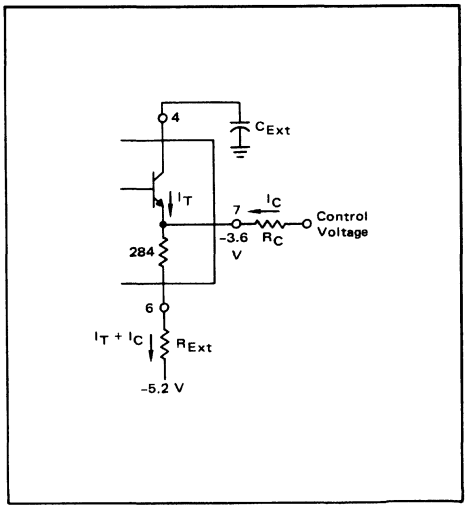
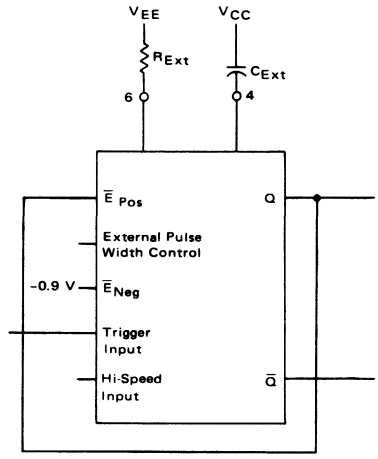


FIGURE 6 —



5. The MC10198 can be made non-retriggerable. The Q output is fed back to disable the trigger input during the triggered state (Logic Diagram). Figure 7 shows a positive triggered configuration; a similar configuration can be made for negative triggering.

FIGURE 7 —



MOTOROLA

MC10210

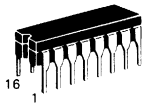
DUAL 3-INPUT 3-OUTPUT "OR" GATE

The MC10210 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR" -ing of several levels of gating for minimization of gate and package count.

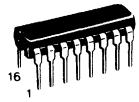
The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10210 particularly useful in clock distribution applications where minimum clock skew is desired.

P_D = 160 mW typ/pkg (No Loads)
t_{pd} = 1.5 ns typ (All Output Loaded)
t_r, t_f = 1.5 ns typ (20%–80%)

DUAL 3-INPUT 3-OUTPUT "OR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

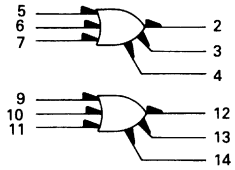


P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

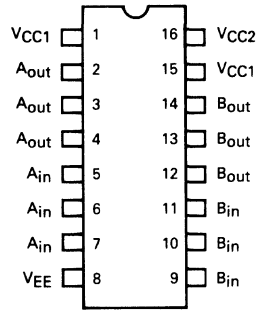
3

LOGIC DIAGRAM



V_{CC1} = Pin 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10210 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	42	–	–	38	–	42	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	650	–	–	410	–	410	µAdc	*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	6	–	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	7	–	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	6	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	7	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2+}	2	1.0	2.6	1.0	1.5	2.5	1.0	2.8	ns	–	–	5	2	8	1,15,16
	t_{5-2-}	2									–	–		2		
	t_{5+3+}	3									–	–		3		
	t_{5-3-}	3									–	–		3		
	t_{5+4+}	4									–	–		4		
	t_{5-4-}	4									–	–		4		
Rise Time (20 to 80%)	t_{2+}	2									–	–		2		
	t_{3+}	3									–	–		3		
	t_{4+}	4									–	–		4		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		
	t_{4-}	4									–	–		4		

*Individually test each input using the pin connections shown.

MOTOROLA

MC10211

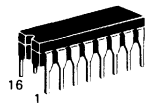
DUAL 3-INPUT 3-OUTPUT "NOR" GATE

The MC10211 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10211 particularly useful in clock distribution applications where minimum clock skew is desired.

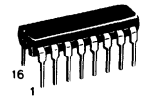
P_D = 160 mW typ/pkg (No Loads)
t_{pd} = 1.5 ns typ (All Output Loaded)
t_r, t_f = 1.5 ns typ (20%–80%)

DUAL 3-INPUT 3-OUTPUT "NOR" GATE



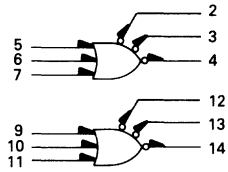
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



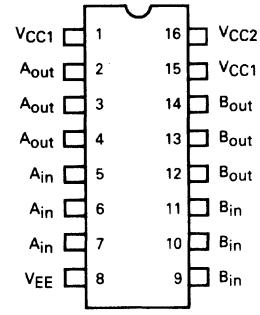
FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM



V_{CC1} = Pin 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10211 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	42	–	30	38	–	42	mAdc	–	–	–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	650	–	–	410	–	410	μAdc	*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	0.5	–	0.5	–	–	0.3	–	μAdc	–	*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	6	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	5	8	1,15,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	6	8	1,15,16
		4	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	–	7	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	6	–	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	7	–	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2-}	2	1.0	2.6	1.0	1.5	2.5	1.0	2.8	ns	–	–	5	2	8	1,15,16
	t_{5-2+}	2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	2	↓	↓
	t_{5+3-}	3									–	–		3		
	t_{5-3+}	3									–	–		3		
	t_{5+4-}	4									–	–		4		
	t_{5-4+}	4									–	–		4		
Rise Time (20 to 80%)	t_{2+}	2									–	–		2		
	t_{3+}	3									–	–		3		
	t_{4+}	4									–	–		4		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		
	t_{4-}	4	↓	↓	↓	↓	↓	↓	↓	↓	–	–	↓	4	↓	↓

*Individually test each input using the pin connections shown.

MOTOROLA

MC10212

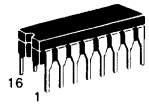
HIGH SPEED DUAL 3-INPUT 3-OUTPUT OR/NOR GATE

The MC10212 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10212 particularly useful in clock distribution applications where minimum clock skew is desired.

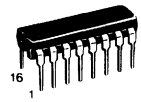
P_D = 160 mW typ/pkg (No Load)
t_{pd} = 1.5 ns typ (All Outputs Loaded)
t_r, t_f = 1.5 ns typ (20%–80%)

HIGH SPEED DUAL 3-INPUT 3-OUTPUT OR/NOR GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

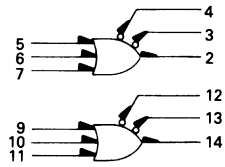
P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

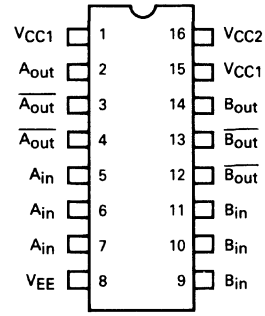
3

LOGIC DIAGRAM



V_{CC1} = Pins 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specification shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gate is tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10212 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	42	–	30	38		42	mAdc			–	–	8	1,15,16
Input Current	I_{inH}	5,6,7	–	650	–	–	410		410	μAdc	5,6,7*	–	–	–	8	1,15,16
	I_{inL}	5,6,7	0.5		0.5	–		0.3		μAdc	–	5,6,7*	–	–	8	1,15,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,15,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
		4	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	–	–	8	1,15,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	–	–	–	8	1,15,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,15,16
		4	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,15,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080		-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,15,16
		3	-1.080		-0.980	–	–	-0.910		Vdc	–	–	–	5	8	1,15,16
		4	-1.080		-0.980	–	–	-0.910	–	Vdc	–	–	–	5	8	1,15,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	5	8	1,15,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,15,16
		4	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,15,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{5+2+}	2	1.0	2.6	1.0	1.5	2.5	1.0	2.8	ns	–	–	5	2	8	1,15,16
	t_{5-2-}	2									–	–		2		
	t_{5+3-}	3									–	–		3		
	t_{5-3+}	3									–	–		3		
	t_{5+4-}	4									–	–		4		
	t_{5-4+}	4									–	–		4		
Rise Time (20 to 80%)	t_{2+}	2									–	–		2		
	t_{3+}	3									–	–		3		
	t_{4+}	4									–	–		4		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		
	t_{4-}	4									–	–		4		

*Individually test each input using the pin connections shown.

MOTOROLA

MC10216

HIGH SPEED TRIPLE LINE RECEIVER

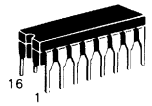
The MC10216 is a high speed triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10216 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

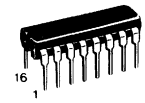
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 1.8 ns typ (Single ended)
= 1.5 ns typ (Differential)
t_r, t_f = 1.5 ns typ (20%–80%)

HIGH SPEED TRIPLE LINE RECEIVER



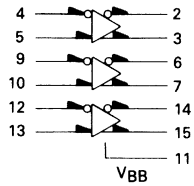
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM

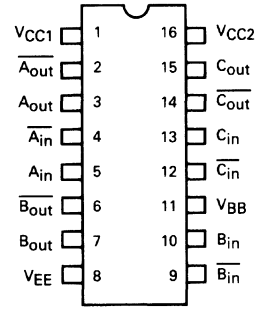


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

*V_{BB} to be used to supply bias to the MC10216 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor.

When the input pin with bubble goes positive, it's respective output pin with bubble goes positive.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	From	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	Pin	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	11	-5.2

Characteristic	Symbol	Pin Under Test	MC10216 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	27	–	20	25	–	27	mAdc	4,9,12	–	–	–	5,10,13	8	1,16
Input Current	I_{inH}	4	–	180	–	–	115	–	115	μAdc	4	9,12	–	–	5,10,13	8	1,16
	I_{CBO}	4	–	1.5	–	–	1.0		1.0	μAdc	–	9,12	–	–	5,10,13	8,4	1,16
		9	–	1.5	–	–	1.0	–	1.0	μAdc	–	4,12	–	–	5,10,13	8,9	1,16
High Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4	9,12	–	–	5,10,13	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	9,12	4	–	–	5,10,13	8	1,16
Low Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	9,12	4	–	–	5,10,13	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	9,12	–	–	5,10,13	8	1,16
High Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9,12	4	–	5,10,13	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	9,12	–	–	4	5,10,13	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9,12	–	4	5,10,13	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	9,12	–	4	–	5,10,13	8	1,16
Reference Voltage	V_{BB}	11	-1.420	-1.280	-1.350	–	-1.230	-1.295	-1.150	Vdc	–	–	–	–	5,10,13	8	1,16
Switching Times (50-ohm Load)													Pulse In	Pulse Out		-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{4+2+}	2	1.0	2.6	1.0	1.8*	2.5	1.0	2.8	ns	–	–	4	2	5,10,13	8	1,16
	t_{4-2-}	2									–	–		2			
	t_{4+3-}	3									–	–		3			
	t_{4-3+}	3									–	–		3			
Rise Time (20% to 80%)	t_{2+}	2				1.5					–	–		2			
	t_{3+}	3									–	–		3			
Fall Time (20% to 80%)	t_{2-}	2									–	–		2			
	t_{3-}	3									–	–		3			

*Delay is 1.5 ns when inputs are driven differentially
Delay is 1.8 ns when inputs are driven single ended

MOTOROLA

MC10231

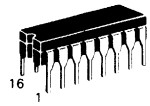
HIGH SPEED DUAL TYPE D MASTER-SLAVE FLIP-FLOP

The MC10231 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{C_E}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

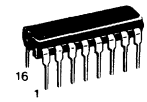
The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master-slave construction.

P_D = 270 mW typ/pkg (No Load)
t_{pd} = 2 ns typ
t_{Tog} = 225 MHz typ
t_r, t_f = 2.0 ns typ (20%–80%)

HIGH SPEED DUAL TYPE D MASTER-SLAVE FLIP-FLOP



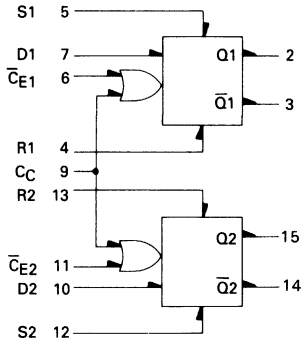
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

CLOCK TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

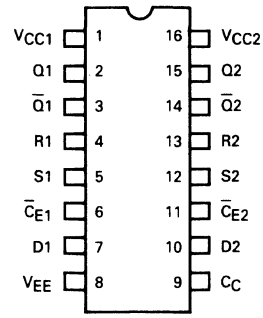
ϕ = Don't Care
$C = \overline{C_E} + C_C$.
A clock H is a clock transition from a low to a high state.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

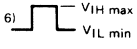
ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table after the thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC10231 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	72	–	52	65	–	72	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	650	–	–	410	–	410	μAdc	4	–	–	–	8	1, 16
		5	–	650	–	–	410	–	410		5	–	–	–		
		6	–	350	–	–	220	–	220		6	–	–	–		
		7	–	350	–	–	220	–	220		7	–	–	–		
		9	–	460	–	–	290	–	290		9	–	–	–		
Input Leakage Current	I_{inL}	4,5,*	–	–	0.5	–	–		–	μAdc	–	*	–	–	8	1, 16
		6,7,9*	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1, 16
		2†	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1, 16
		3†	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1, 16
		2†	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	7	9	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1, 16
		3†	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	7	9	8	1, 16
Switching Times											+1.11 Vdc		Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input Propagation Delay	t_{9+2-}	2	1.5	3.4	1.5	2.0	3.3	1.6	3.7	ns	–	–	9	2	8	1, 16
	t_{6+2+}	2	1.5	3.4	1.5	2.0	3.3	1.6	3.7		7	–	6	2		
Rise Time (20 to 80%)	t_{2+}	2	0.9	3.3	1.0	1.3	3.1	1.0	3.6		7	–	9	2		
Fall Time (20 to 80%)	t_{2-}	2	0.9	3.3	1.0	1.3	3.1	1.0	3.6		–	–	9	2		
Set Input Propagation Delay	t_{5+2+}	2	1.1	3.4	1.1	2.0	3.3	1.2	3.7	ns	–	–	5	2	8	1, 16
	t_{12+15+}	15									6	–	12	15		
	t_{5+3+}	3									–	–	5	3		
	t_{12+14-}	14									9	–	12	14		
Reset Input Propagation Delay	t_{4+2-}	2	1.1	3.4	1.1	2.0	3.3	1.2	3.7	ns	–	–	4	2	8	1, 16
	t_{13+15-}	15									6	–	13	15		
	t_{4+3-}	3									–	–	4	3		
	t_{13+14+}	14									9	–	13	14		
Setup Time	t_{Setup}	7	1.5	–	1.0	–	–	1.5	–	ns	–	–	6,7	2	8	1, 16
Hold Time	t_{Hold}	7	0.9	–	0.75	–	–	0.9	–	ns	–	–	6,7	2	8	1, 16
Toggle Frequency (Max)	f_{Tog}	2	200	–	200	225	–	200	–	MHz	• •	–	6	2	8	1, 16

*Individually test each input; apply $V_{IL\ min}$ to pin under test.

†Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ input (pin 6) 

MECL III

Selector Guide | **Data Sheets** | **4**

MECL III
INTEGRATED CIRCUITS

MC1600 Series
(−30 to +85°C)

Function Selection — (−30 to +85°C)

Function	Device	Case
Gates		
Dual 4-Input OR/NOR	MC1660	620
Quad 2-Input NOR	MC1662	620
Triple 2-Input Exclusive OR	MC1672	620
Flip-Flops		
Master-Slave Type D	MC1670	620
UHF Prescaler Type D	MC1690(1)	620
Multivibrator		
Voltage-Controlled	MC1658	620, 648 751B, 775
Oscillator		
Emitter Coupled	MC1648	632, 646 751, 775
Comparator		
Dual A/D	MC1650/ MC1651	620
Receiver		
Quad-Line	MC1692	620

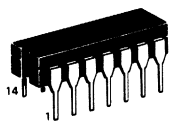
(1) Obsolete use MC12090

4

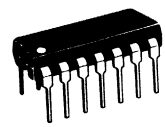
MOTOROLA

MC1648

VOLTAGE-CONTROLLED OSCILLATOR



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751

FN SUFFIX
PLASTIC PACKAGE
CASE 775

VOLTAGE-CONTROLLED OSCILLATOR

The MC1648 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C). FOR MAXIMUM PERFORMANCE $Q_L \geq 100$ AT FREQUENCY OF OPERATION.

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase-Locked Loop shown in Figure 9. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity. (See Figure 2.)

The MC1648 may be operated from a +5.0 Vdc supply or a −5.2 Vdc supply, depending upon system requirements.

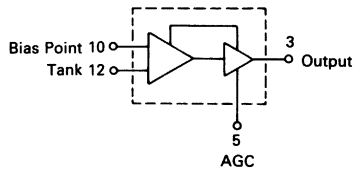
Supply Voltage	Gnd Pins	Supply Pins
+5.0 Vdc	7, 8	1, 14
−5.2 Vdc	1, 14	7, 8

MC1648 PIN CONVERSION DATA
NON-STANDARD

	Tank	V_{CC}	V_{CC}	Output	AGC	V_{EE}	V_{EE}	Bias Point
8 D	1	2	3	4	5	6	7	8
14 L, P	12	14	1	3	5	7	8	10
20 FN	18	20	2	4	8	10	12	14

*Note — All unused pins are not connected.

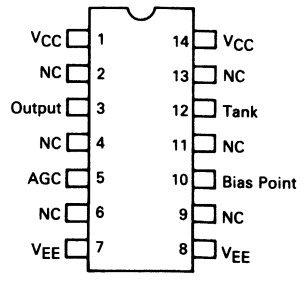
LOGIC DIAGRAM



Input Capacitance = 6.0 pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ
Power Dissipation = 150 mW typ/pkg (+5.0 Vdc Supply)
Maximum Output Frequency = 225 MHz typ

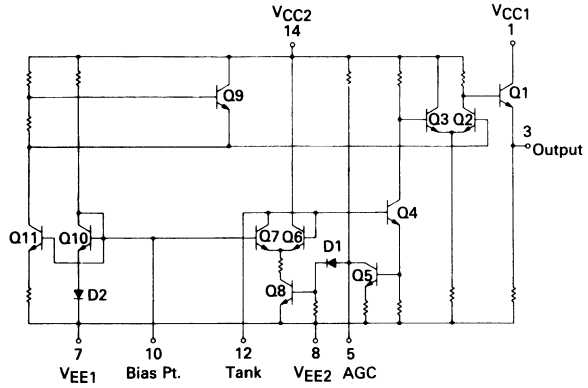
V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{EE} = Pin 7

PIN ASSIGNMENT



4

FIGURE 1 — CIRCUIT SCHEMATIC



@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{CC}	mAdc I_L
MC1648				
−30°C	+2.0	+1.5	5.0	−5.0
+25°C	+1.85	+1.35	5.0	−5.0
+85°C	+1.7	+1.2	5.0	−5.0

Note: SOIC "D" Package guaranteed −30° to +70°C only

ELECTRICAL CHARACTERISTICS

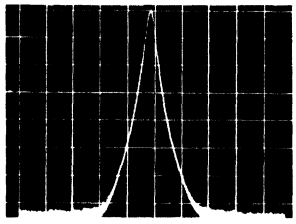
Supply Voltage = +5.0 Volts

Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	Conditions
Power Supply Drain Current	I_E	—	—	—	41	—	—	mAdc	Inputs and outputs open.
Logic "1" Output Voltage	V_{OH}	3.955	4.185	4.04	4.25	4.11	4.36	Vdc	V_{ILmin} to Pin 12, I_L @ Pin 3.
Logic "0" Output Voltage	V_{OL}	3.16	3.4	3.2	3.43	3.22	3.475	Vdc	V_{IHmax} to Pin 12, I_L @ Pin 3.
Bias Voltage	V_{Bias}*	1.6	1.9	1.45	1.75	1.3	1.6	Vdc	V_{ILmin} to Pin 12.

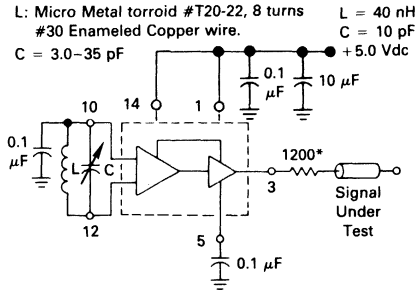
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Peak-to-Peak Tank Voltage	V_{P-P}	—	—	—	—	400	—	—	—	—	mV	See Figure 3.
Output Duty Cycle	Vdc	—	—	—	—	50	—	—	—	—	%	
Oscillation Frequency	f_{max}**	—	225	—	200	225	—	—	225	—	MHz	

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.
**Frequency variation over temperature is a direct function of the ΔC/Δ Temperature and ΔL/Δ Temperature.

FIGURE 2 — SPECTRAL PURITY OF SIGNAL OUTPUT FOR 200 MHz TESTING



B.W. = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div



*The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{EE}	mAdc I_L
MC1648				
−30°C	−3.2	−3.7	−5.2	−5.0
+25°C	−3.35	−3.85	−5.2	−5.0
+85°C	−3.5	−4.0	−5.2	−5.0

Note: SOIC "D" Package guaranteed −30° to +70°C only

ELECTRICAL CHARACTERISTICS

Supply Voltage = −5.2 Volts

Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	Conditions
Power Supply Drain Current	I_E	—	—	—	41	—	—	mAdc	Inputs and outputs open.
Logic "1" Output Voltage	V_{OH}	−1.045	−0.815	−0.96	−0.75	−0.89	−0.64	Vdc	V_{ILmin} to Pin 12, I_L @ Pin 3.
Logic "0" Output Voltage	V_{OL}	−1.89	−1.65	−1.85	−1.62	−1.83	−1.575	Vdc	V_{IHmax} to Pin 12, I_L @ Pin 3.
Bias Voltage	V_{Bias}*	−3.6	−3.3	−3.75	−3.45	−3.9	−3.6	Vdc	V_{ILmin} to Pin 12.

		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Peak-to-Peak Tank Voltage	V_{P-P}	—	—	—	—	400	—	—	—	—	mV	See Figure 3.
Output Duty Cycle	Vdc	—	—	—	—	50	—	—	—	—	%	
Oscillation Frequency	f_{max}**	—	225	—	200	225	—	—	225	—	MHz	

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.
**Frequency variation over temperature is a direct function of the ΔC/Δ Temperature and ΔL/Δ Temperature.

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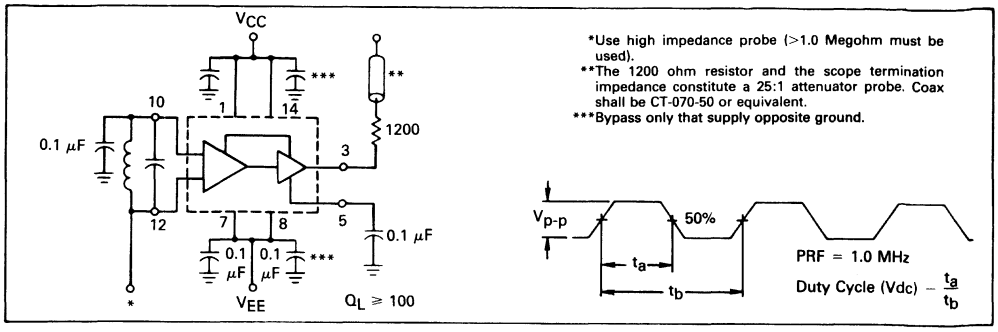
FIGURE 3 — TEST CIRCUIT AND WAVEFORMS



OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the MC1648. The oscillator incorporates positive feedback by coupling the base of transistor Q6 to the collector of Q7. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q6) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, transistor Q4 is used to translate the oscillator signal to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provides a highly buffered output which produces a square wave. Transistors Q9 and Q11 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that the cathode of the varactor diode (D) should be biased at least "2" V_{BE} above V_{EE} (≈1.4 V for positive supply operation).

When the MC1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

FIGURE 4 — THE MC1648 OPERATING IN THE VOLTAGE CONTROLLED MODE

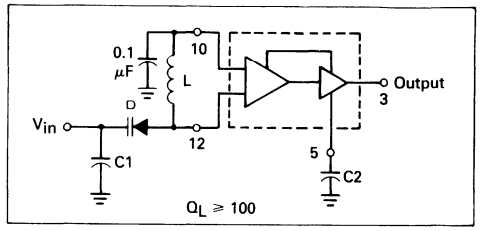
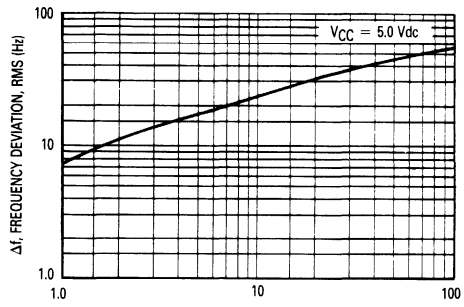
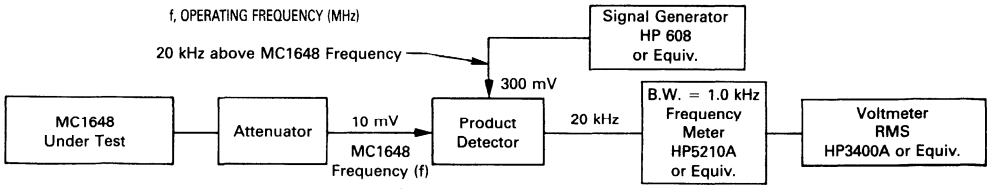


FIGURE 5 — NOISE DEVIATION TEST CIRCUIT AND WAVEFORM



Oscillator Tank Components (Circuit of Figure 4)

f MHz	D	L μH
1.0–10	MV2115	100
10–60	MV2116	2.3
60–100	MV2106	0.15



$$\text{Frequency Deviation} = \frac{\text{(HP5210A output voltage) (Full Scale Frequency)}}{\text{1.0 Volt}}$$

NOTE: Any frequency deviation caused by the signal generator and MC1648 power supply should be determined and minimized prior to testing.

TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE USING EXTERNAL VARACTOR DIODE AND COIL. T_A = 25°C

FIGURE 6

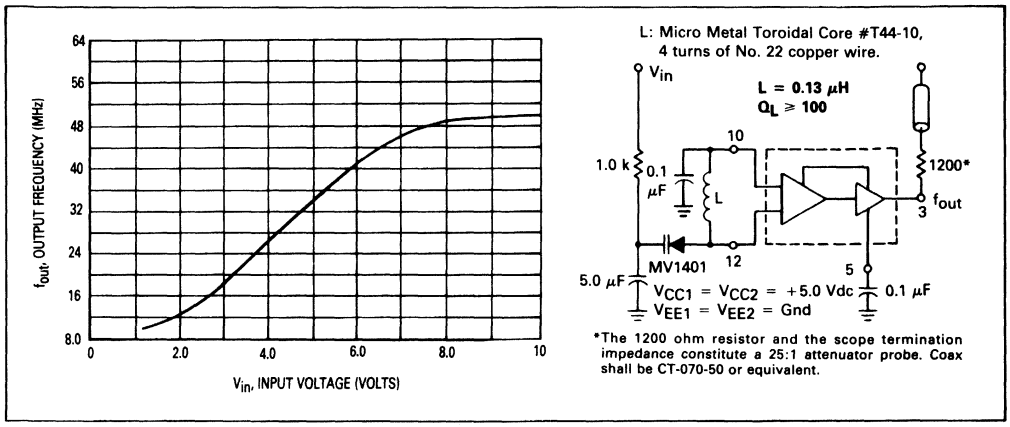


FIGURE 7

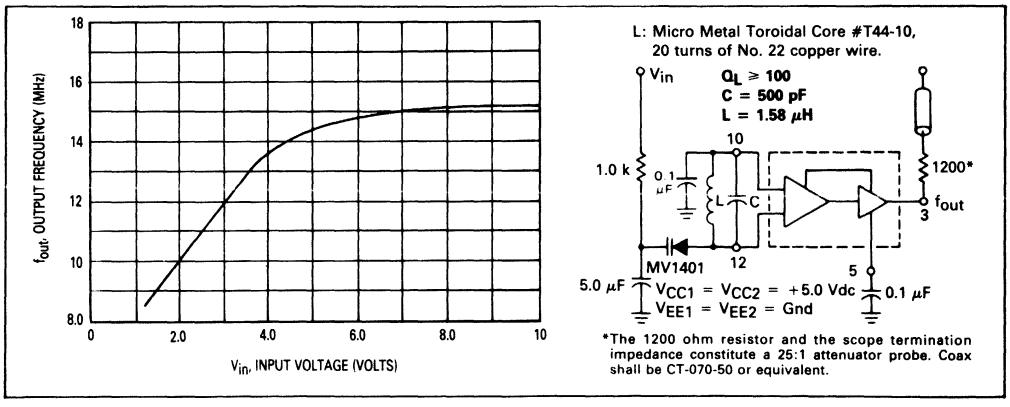
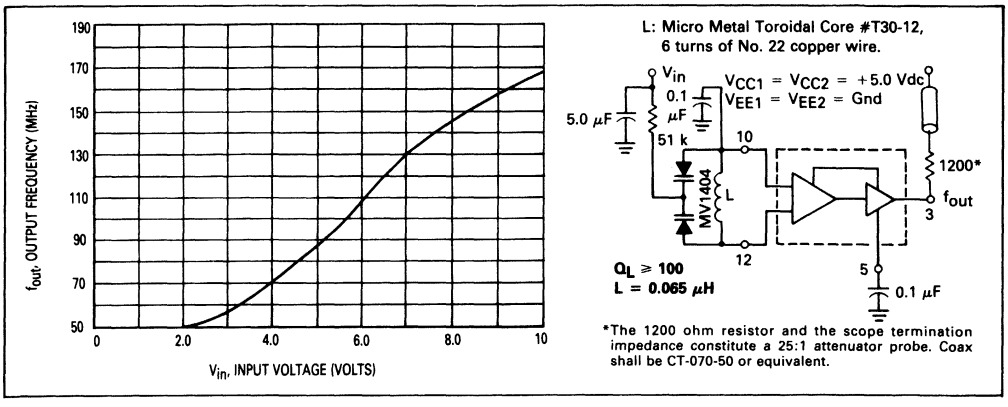


FIGURE 8



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Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7, and 8. Figures 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6.0 pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1.0 kΩ resistor in Figures 6 and 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D(max) + C_S}}{\sqrt{C_D(min) + C_S}}$$

where $f_{min} = \frac{1}{2\pi\sqrt{L(C_D(max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency bypassing is necessary on the power supply pins. (See Figure 2.)

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1.0 MHz and 50 MHz a 0.1 μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At high frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, −5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be desirable to increase the tank circuit peak-to-peak voltage in order to shape the signal at the output of the MC1648. This is accomplished by tying a series resistor (1.0 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a −5.2 volt supply is used). Figure 11 illustrates this principle.

4

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and land-mobile communications, amateur and CB receivers. The system operates from a single +5.0 Vdc supply, and requires no internal translations, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lockup. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

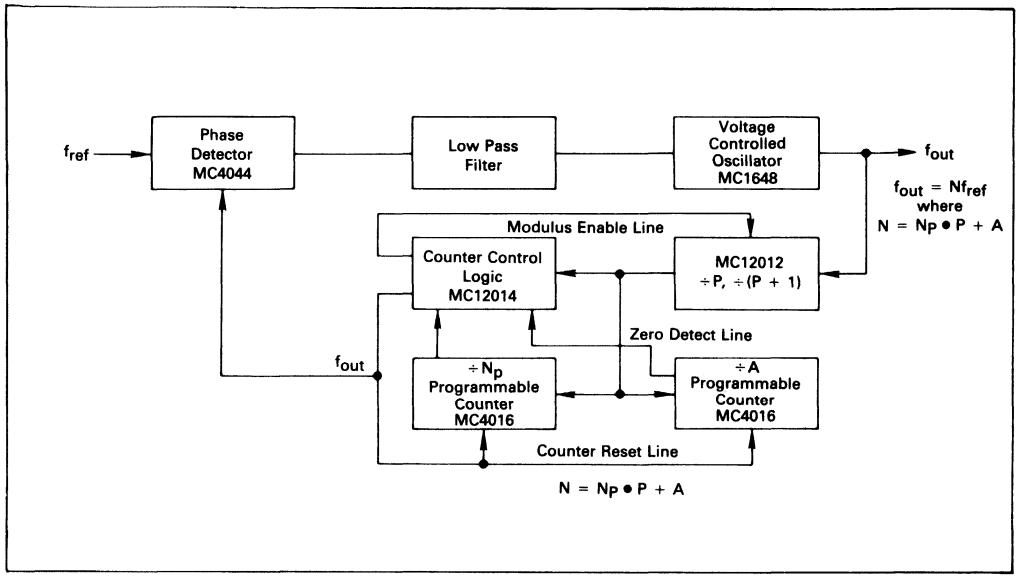
The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{out} = Nf_{ref}$. The channel spacing is equal to frequency (f_{ref}).

For additional information on applications and designs for phase locked-loops and digital frequency synthesizers, see Motorola Brochure BR504/D, Electronic Tuning Address Systems, (ETAS).

Figure 10 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to V_{EE}.

Figure 11 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To extend the useful range of the device (maintain a square wave output

FIGURE 9 — TYPICAL FREQUENCY SYNTHESIZER APPLICATION



above 175 MHz), a resistor is added to the AGC circuit at pin 5 (1.0 k-ohm minimum).

Figure 12 shows the MC1648 operating from +5.0 Vdc and +9.0 Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the MECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figures 13 and 14 for 100 MHz and 10 MHz operation. The total collector load includes R in parallel with Rp of L1 and C1 at resonance. The optimum value for R at 100 MHz is approximately 850 ohms.

FIGURE 10 — METHOD OF OBTAINING A SINE-WAVE OUTPUT

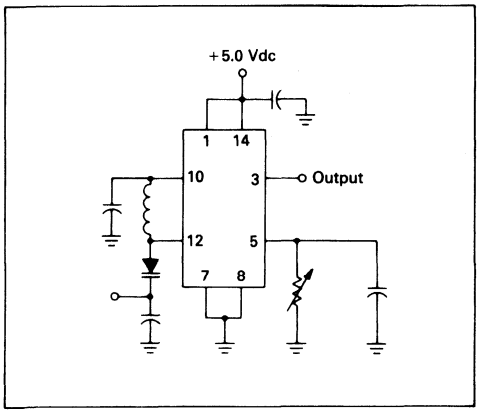


FIGURE 11 — METHOD OF EXTENDING THE USEFUL RANGE OF THE MC1648 (SQUARE WAVE OUTPUT)

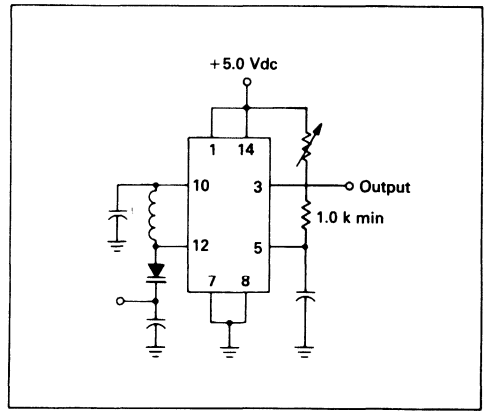
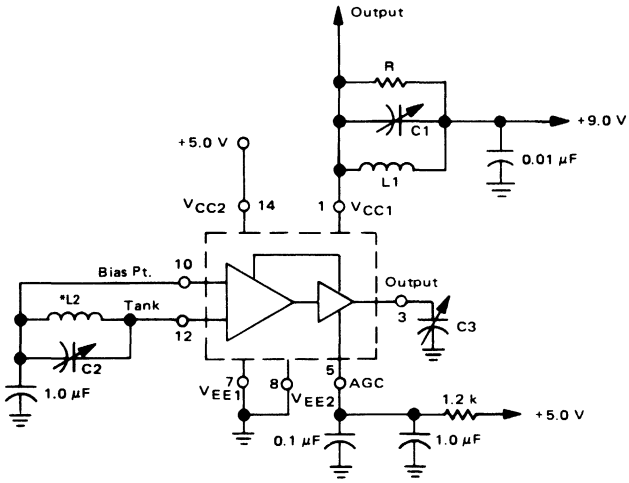


FIGURE 12 — CIRCUIT USED FOR COLLECTOR OUTPUT OPERATION



*$Q_L \geq 100$

4

FIGURE 13 — POWER OUTPUT versus COLLECTOR LOAD

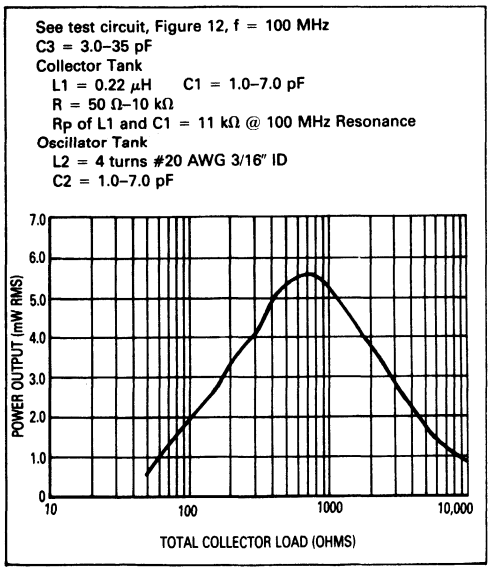
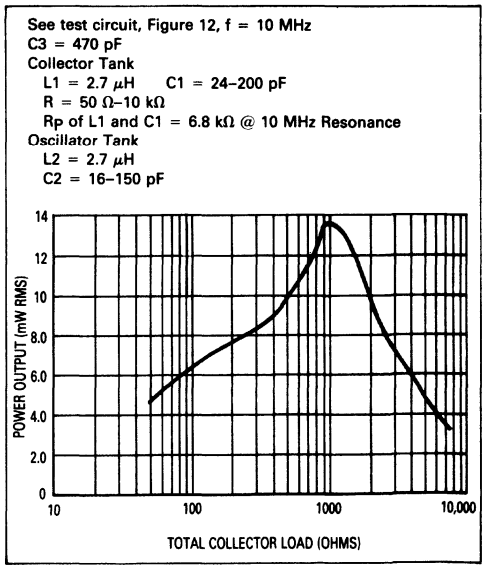


FIGURE 14 — POWER OUTPUT versus COLLECTOR LOAD



MOTOROLA

MC1650
MC1651

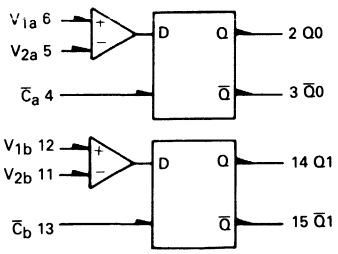
DUAL A/D CONVERTER

The MC1650 and the MC1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The MC1650 provides high impedance Darlington inputs, while the MC1651 is a lower impedance option, with higher input slew rate and higher speed capability.

The clock inputs ($\overline{C}_a$ and $\overline{C}_b$) operate from MECL III or MECL 10,000 digital levels. When $\overline{C}_a$ is at a logic high level, Q0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q}0$ is the logic complement of Q0. When the clock input goes to a low logic level, the outputs are latched in their present state.

Assessment of the performance differences between the MC1650 and the MC1651 may be based upon the relative behaviors shown in Figures 4 and 7.

LOGIC DIAGRAM

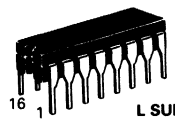


V_{CC} = +5.0 V = Pin 7, 10
V_{EE} = −5.2 V = Pin 8
Gnd = Pin 1, 16

- P_D = 330 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ (MC1650)
  = 3.0 ns typ (MC1651)
- Input Slew Rate = 350 V/μs (MC1650)
  = 500 V/μs (MC1651)
- Differential Input Voltage: 5.0 V (−30°C to +85°C)
- Common Mode Range:
  −3.0 V to +2.5 V (−30°C to +85°C) (MC1651)
  −2.5 V to +3.0 V (−30°C to +85°C) (MC1650)
- Resolution: ≤ 20 mV (−30°C to +85°C)
- Drives 50 Ω lines

Number at end of terminal denotes pin number for L package (Case 620).

DUAL A/D CONVERTER



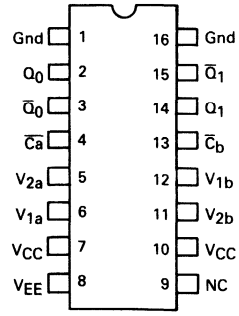
L SUFFIX
CERAMIC PACKAGE
CASE 620

TRUTH TABLE

$\overline{C}$	V_1, V_2	$Q0_{n+1}$	$\overline{Q0}_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	$Q0_n$	$\overline{Q0}_n$

ϕ = Don't Care

PIN ASSIGNMENT



4

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC}[3]	V_{EE}[3]
−30°C	−0.875	−1.89	−1.18	−1.515	+0.02	−0.02	See Note 4				+5.0	−5.2
+25°C	−0.81	−1.85	−1.095	−1.485	+0.02	−0.02					+5.0	−5.2
+85°C	−0.7	−1.83	−1.025	−1.44	+0.02	−0.02					+5.0	−5.2

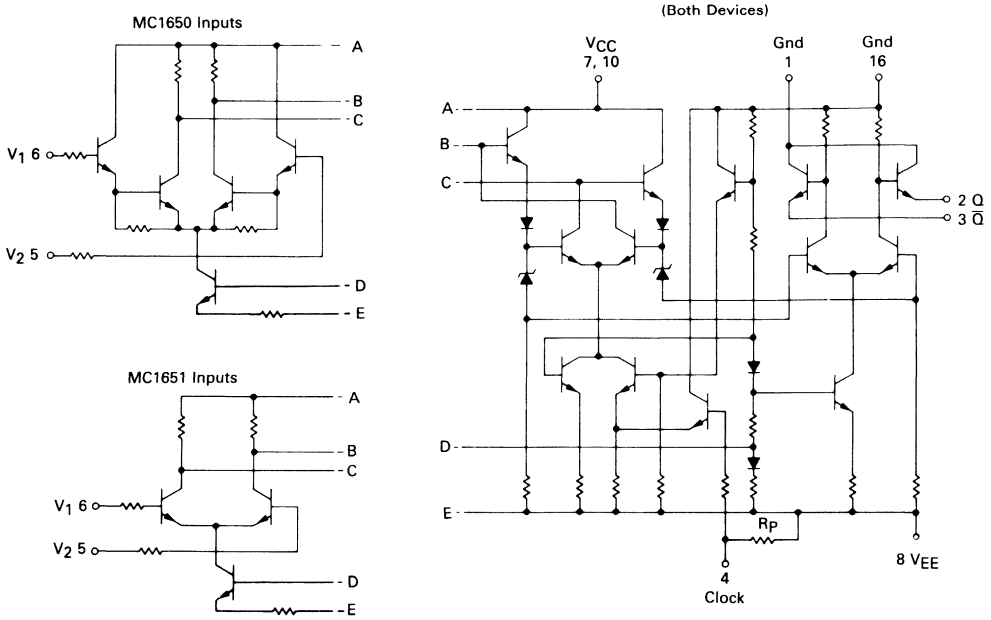
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	Gnd
Power Supply Drain Current								mAdc											
Positive	I_{CC}	—	—	—	25*	—	—		—	4,13	—	—	6,12	—	—	—	—	—	1,5,11,16
Negative	I_E	—	—	—	55*	—	—		4,13	—	—	—	6,12	—	—	—	—	—	1,5,11,16
Input Current	I_{in}							μAdc											
MC1650		—	—	—	10	—	—		4	13	—	—	12	—	6	—	—	—	1,5,11,16
MC1651		—	—	—	40	—	—		—	—	—	—	—	—	—	—	—	—	
Input Leakage Current	I_R							μAdc											
MC1650		—	—	—	7.0	—	—		4	13	—	—	12	—	—	—	6	—	1,5,11,16
MC1651		—	—	—	10	—	—		—	—	—	—	—	—	—	—	—	—	
Clock Input Current	I_{inH}	—	—	—	350	—	—	μAdc	4	13	—	—	6,12	—	—	—	—	—	1,5,11,16
Logic "1" Output Voltage	V_{OH}	−1.045	−0.875	−0.96	−0.81	−0.89	−0.7	Vdc	4,13	—	—	—	6,12	—	—	—	—	—	1,5,11,16
										—	—	—	—	5,11	—	—	—	—	1,6,12,16
										—	—	—	—	—	6,12	5,11	—	—	1,16
										—	—	—	—	—	—	—	5,11	6,12	1,16
										—	—	—	—	6,12	—	—	—	—	1,5,11,16
										—	—	—	5,11	—	—	—	—	—	1,6,12,16
										—	—	—	—	—	5,11	6,12	—	—	1,16
										—	—	—	—	—	—	—	6,12	5,11	1,16
Logic "0" Output Voltage	V_{OL}	−1.89	−1.65	−1.85	−1.62	−1.83	−1.575	Vdc	4,13	—	—	—	—	6,12	—	—	—	—	1,5,11,16
										—	—	—	5,11	—	—	—	—	—	1,6,12,16
										—	—	—	—	—	5,11	6,12	—	—	1,16
										—	—	—	—	—	—	—	6,12	5,11	1,16
										—	—	—	6,12	—	—	—	—	—	1,5,11,16
										—	—	—	—	5,11	—	—	—	—	1,6,12,16
										—	—	—	—	—	6,12	5,11	—	—	1,16
										—	—	—	—	—	—	—	5,11	6,12	1,16
Logic "1" Threshold Voltage[2]	V_{OHA}	−1.065	—	−0.98	—	−0.91	—	Vdc	—	13	4	—	6	—	—	—	—	—	1,5,16
									—		—	4	—	6	—	—	—	—	
									—		4	—	—	6	—	—	—	—	
									—		—	4	6	—	—	—	—	—	
Logic "0" Threshold Voltage[2]	V_{OLA}	—	−1.63	—	−1.6	—	−1.555	Vdc	—	13	4	—	6	—	—	—	—	—	1,5,16
									—		—	4	—	6	—	—	—	—	
									—		4	—	—	6	—	—	—	—	
									—		—	4	6	—	—	—	—	—	

NOTES: 1. All data is for 1/2 MC1650 or MC1651, except data marked (*) which refers to the entire package.
2. These tests done in order indicated. See Figure 5.
3. Maximum Power Supply Voltages (beyond which device life may be impaired):
$|V_{EE}| + |V_{CC}| \geq 12$ Vdc
4.

All Temperatures	V_{A3}	V_{A4}	V_{A5}	V_{A6}
MC1650	+3.0	+2.98	−2.5	−2.48
MC1651	+2.5	+2.48	−3.0	−2.98

CIRCUIT SCHEMATIC
1/2 of Device Shown



4

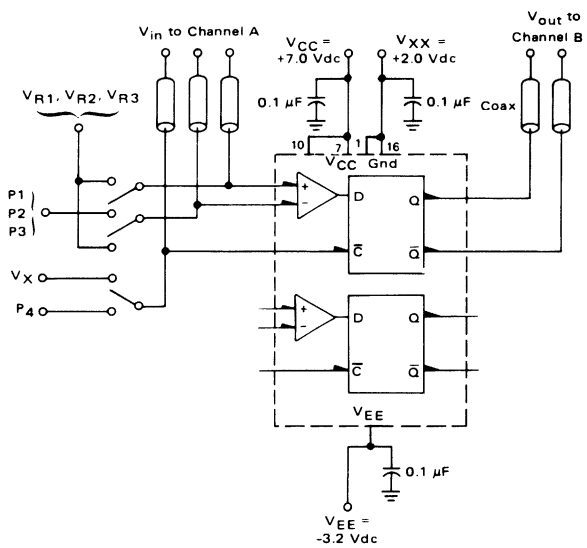
@ Test Temperature	SWITCHING TEST VOLTAGE VALUES (Volts)						
	V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC}[1]	V_{EE}[1]
−30°C	+2.0	See Note 4		+1.04	+2.0	+7.0	−3.2
+25°C	+2.0			+1.11	+2.0	+7.0	−3.2
+85°C	+2.0			+1.19	+2.0	+7.0	−3.2

Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	Conditions (See Figures 1–3)
Switching Times Propagation Delay (50% to 50%) V-Input	t_{pd}	2.0	5.0	2.0	5.0	2.0	5.7	ns	V_{R1} to V_2, V_X to Clock, P_1 to V_1, or, V_{R2} to V_2, V_X to Clock, P_2 to V_1, or, V_{R3} to V_2, V_X to Clock, P_3 to V_1.
Clock[2]		2.0	4.7	2.0	4.7	2.0	5.2		V_{R1} to V_2, P_1 to V_1 and P_4 to Clock, or, V_{R1} to V_1, P_1 to V_2 and P_4 to Clock.
Clock Enable[3]	t_{setup}	—	—	2.5	—	—	—	ns	V_{R1} to V_2, P_1 to V_1, P_4 to Clock
Clock Aperture[3]	t_{ap}	—	—	1.5	—	—	—	ns	
Rise Time (10% to 90%)	t^+	1.0	3.5	1.0	3.5	1.0	3.8	ns	V_R to V_2, V_X to Clock, P_1 to V_1.
Fall Time (10% to 90%)	t^-	1.0	3.0	1.0	3.0	1.0	3.3	ns	

NOTES: 1. Maximum Power Supply Voltages (beyond which device life may be impaired:
$|V_{CC}| + |V_{EE}| \geq 12$ Vdc.
2. Unused clock inputs may be tied to ground.
3. See Figure 3.
4.

All Temperatures	V_{R2}	V_{R3}
MC1650	+4.9	−0.4
MC1651	+4.4	−0.9

FIGURE 1 — SWITCHING TIME TEST CIRCUIT @ 25°C



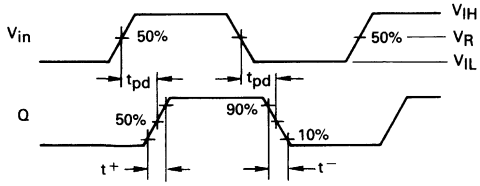
Note: All power supply and logic levels are shown shifted 2.0 volts positive.
50 ohm termination to ground located in each scope channel input.
All input and output cables to the scope are equal lengths of 50 ohm coaxial cable.

4

FIGURE 2 — SWITCHING AND PROPAGATION WAVEFORMS @ 25°C

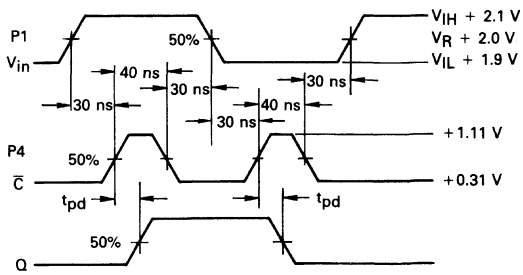
The pulse levels shown are used to check ac parameters over the full common-mode range.

V — INPUT TO OUTPUT



Test pulses: t_+, t_- = 1.5 ± 0.2 ns (10% to 90%)
f = 5.0 MHz
50% Duty Cycle

CLOCK TO OUTPUT

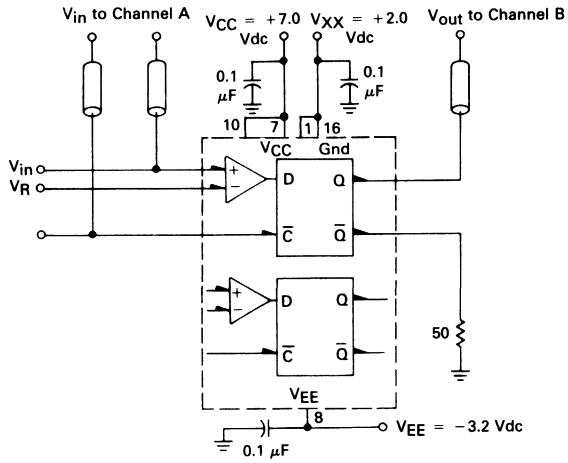


P4: t_+, t_- = 1.5 ± 0.2 ns.

TEST PULSE LEVELS

	P1		P2		P3	
	MC1650	MC1651	MC1650	MC1651	MC1650	MC1651
V_{IH}	+2.1 V	+2.1 V	+5.0 V	+4.5 V	−0.3 V	−0.8 V
V_R	+2.0 V	+2.0 V	+4.9 V	+4.4 V	−0.4 V	−0.9 V
V_{IL}	+1.9 V	+1.9 V	+4.8 V	+4.3 V	−0.5 V	−1.0 V

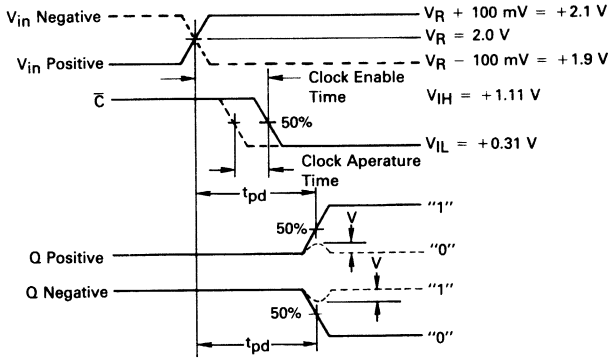
FIGURE 3 — CLOCK ENABLE AND APERTURE TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50 ohm termination to ground located in each scope channel input.
All input and output cables to the scope are equal lengths of 50 ohm coaxial cable.

4

ANALOG SIGNAL POSITIVE AND NEGATIVE SLEW CASE



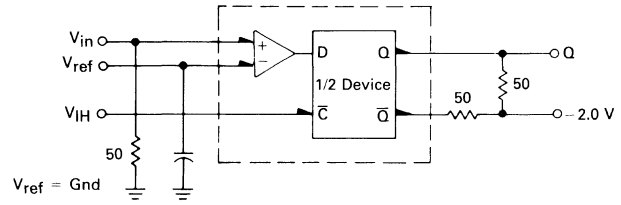
——— Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200 ps.

– – – – – – Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

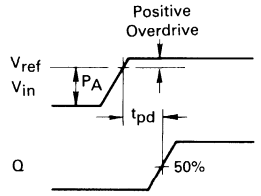
Note: All power supply and logic levels are shown shifted 2.0 volts positive.

FIGURE 4 — PROPAGATION DELAY (t_{pd}) versus INPUT PULSE AMPLITUDE AND CONSTANT OVERDRIVE

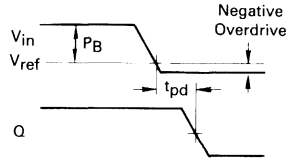
TEST CIRCUIT



POSITIVE PULSE DIAGRAM

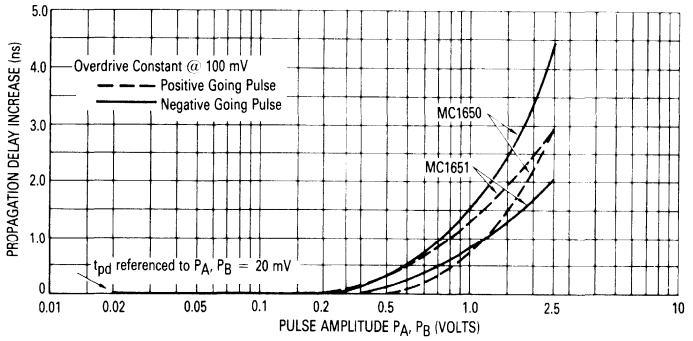


NEGATIVE PULSE DIAGRAM



Input Switching time is constant at 1.5 ns (10% to 90%).

PROPAGATION DELAY versus PULSE AMPLITUDE



PROPAGATION DELAY versus OVERDRIVE

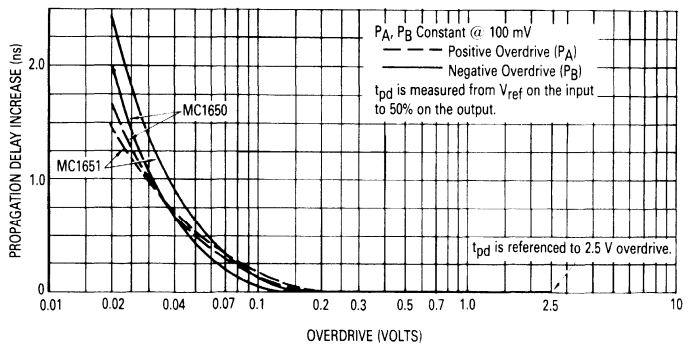


FIGURE 5 — LOGIC THRESHOLD TESTS (WAVEFORM SEQUENCE DIAGRAM)

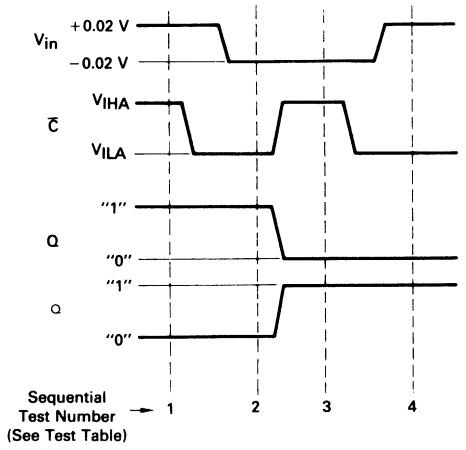
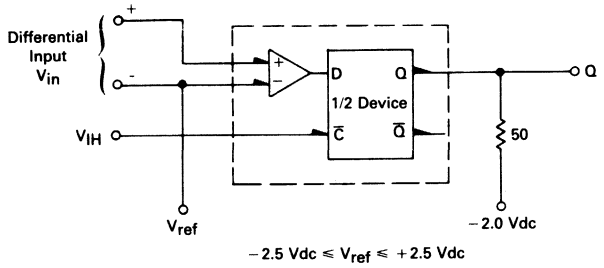


FIGURE 6 — TRANSFER CHARACTERISTICS (Q versus V_{in})

TEST CONFIGURATION



$-2.5\ Vdc \leq V_{ref} \leq +2.5\ Vdc$

TYPICAL TRANSFER CURVES

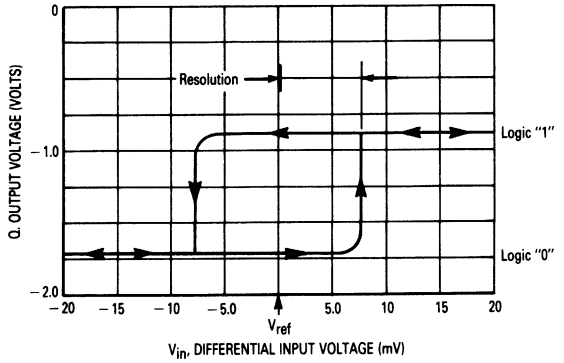
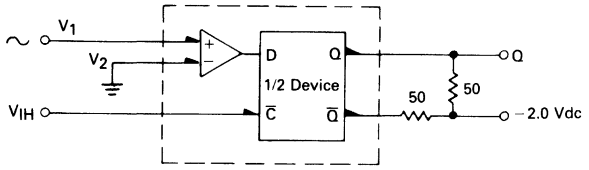
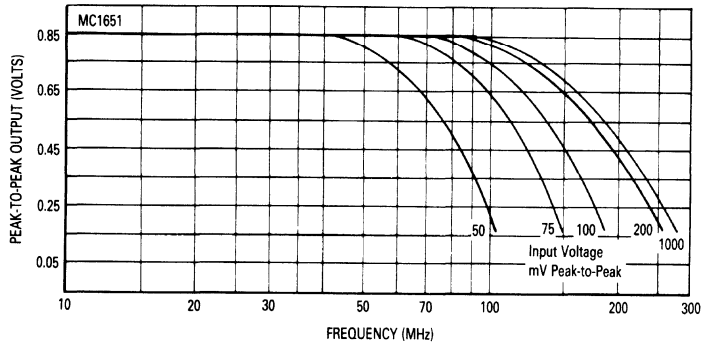


FIGURE 7 — OUTPUT VOLTAGE SWING versus FREQUENCY

(A) TEST CIRCUIT



(B) TYPICAL OUTPUT LOGIC SWING versus FREQUENCY



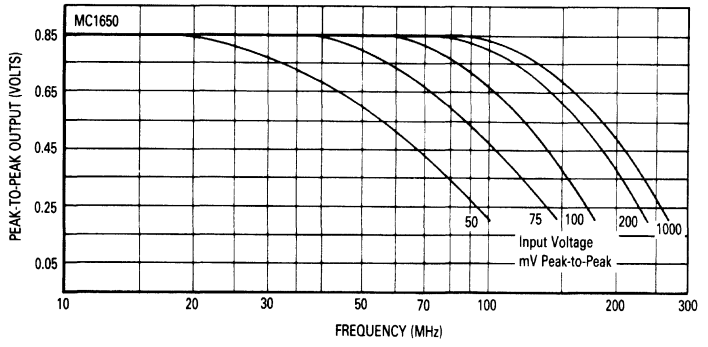


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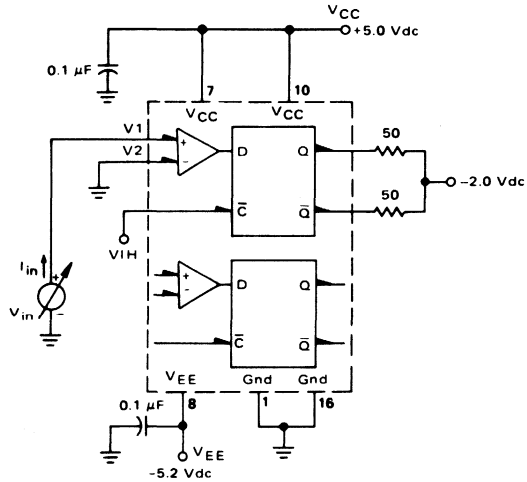
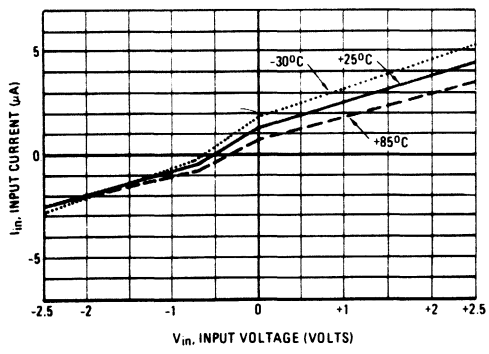
FIGURE 8 — INPUT CURRENT versus INPUT VOLTAGE

TEST CIRCUIT

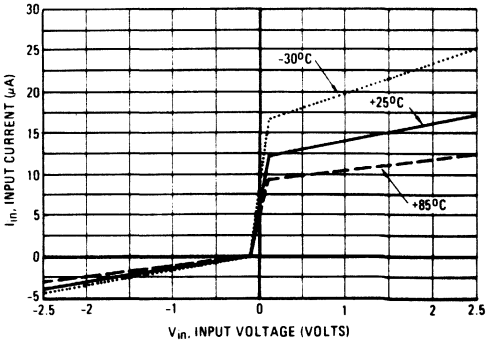


4

Typical MC1650 (Complementary Input Grounded)



Typical MC1651 (Complementary Input Grounded)



MOTOROLA

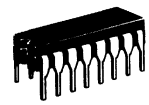
MC1658

VOLTAGE-CONTROLLED MULTIVIBRATOR

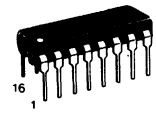
The MC1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with MECL III and MECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.

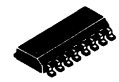
VOLTAGE-CONTROLLED MULTIVIBRATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

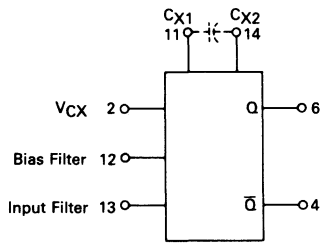


D SUFFIX
PLASTIC PACKAGE
CASE 751B

FN SUFFIX
PLASTIC PACKAGE
CASE 775

4

LOGIC DIAGRAM



V_{CC} = Pin 1
V_{CC2} = Pin 5
V_{EE} = Pin 8

PIN ASSIGNMENT

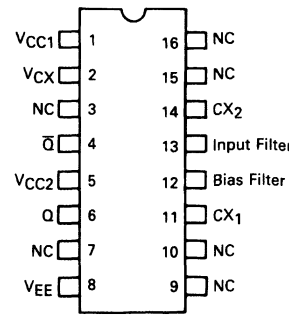
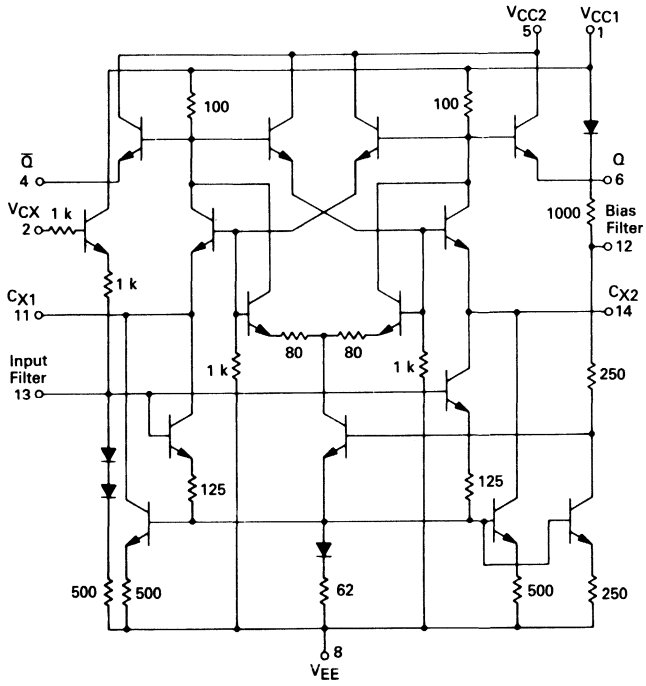


FIGURE 1 — CIRCUIT SCHEMATIC



@ Test Temperature	TEST VOLTAGE VALUES Vdc ±1% V_{IH}	V_{IL}	V_3	V_{IHA}
−30°C	0	−2.0	−1.0	+2.0
+25°C	0	−2.0	−1.0	+2.0
+85°C	0	−2.0	−1.0	+2.0

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V V_{CC} = 0 V (GND)

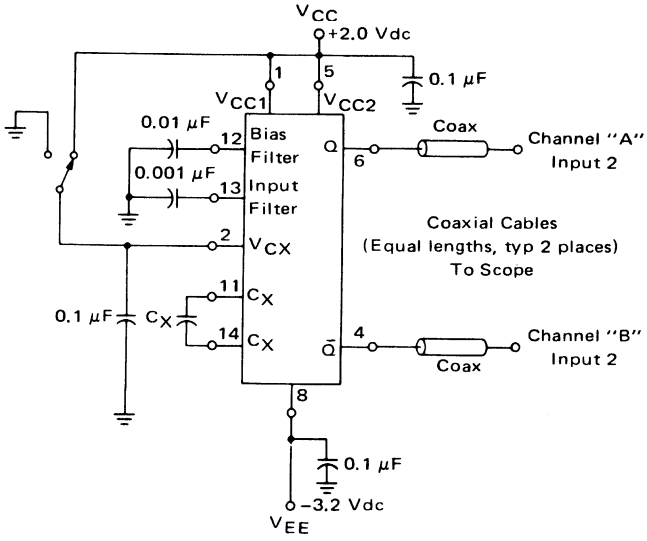
Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	Conditions
Power Supply Drain Current	I_E	—	—	—	32	—	—	mAdc	V_{IH} to V_{CX} Limit applies for 1 or 2
Input Current	I_{inH}	—	—	—	350	—	—	μAdc	V_{IH} to V_{CX}[1]
"Q" High Output Voltage	V_{OH}	−1.045	−0.875	−0.96	−0.81	−0.89	−0.7	Vdc	V_3 to V_{CX}. Limits apply for 1 or 2
"Q̄" Low Output Voltage	V_{OL}	−1.89	−1.65	−1.85	−1.62	−1.83	−1.575	Vdc	

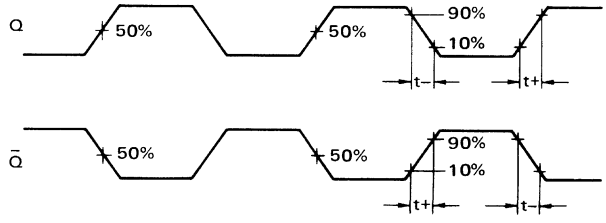
AC CHARACTERISTICS (V_{EE} = −3.2 V V_{CC} = +2.0 V)

	Symbol	Min	Max	Min	Typ	Max	Min	Max	Unit	Conditions (See Figure 2)
Rise Time (10% to 90%)	t^+	—	2.7	—	1.6	2.7	—	3.0	ns	V_{IHA} to V_{CX}, CX1[4] from pin 11 to pin 14.
Fall Time (10% to 90%)	t^-	—	2.7	—	1.4	2.7	—	3.0	ns	
Oscillator Frequency	f_{osc1}	130	—	130	155	175	110	—	MHz	
	f_{osc2}	—	—	78	100	120	—	—	MHz	V_{IHA} to V_{CX}, CX2[5] from pin 11 to pin 14.
Tuning Ratio Test	TR[3]	—	—	3.1	4.5	—	—	—	—	CX2[5] from pin 11 to pin 14.

NOTES: 1. Germanium diode (0.4 drop) forward biased from 11 to 14 (11 → 14).
2. Germanium diode (0.4 drop) forward biased from 14 to 11 (11 ← 14).
3. $TR = \frac{\text{Output frequency at } V_{CX} = \text{Gnd}}{\text{Output frequency at } V_{CX} = -2.0\text{ V}}$
4. C_{X1} = 5.0 pF connected from pin 11 to pin 14.
5. C_{X2} = 10 pF connected from pin 11 to pin 14.

FIGURE 2 — AC TEST CIRCUIT AND WAVEFORMS





50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Note: All power supply and logic levels are shown shifted 2.0 volts positive.

4

FIGURE 3 — OUTPUT FREQUENCY versus CAPACITANCE FOR VARIOUS VALUES OF INPUT VOLTAGE

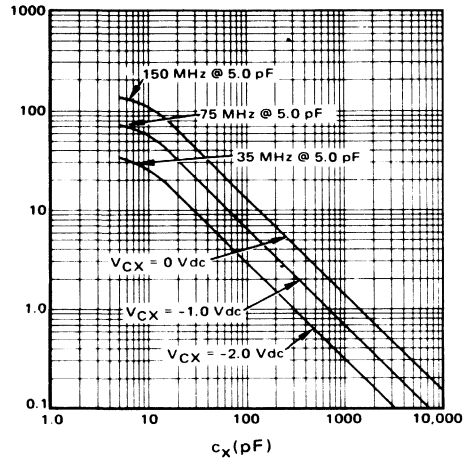


FIGURE 4 — RMS NOISE DEVIATION versus OPERATING FREQUENCY

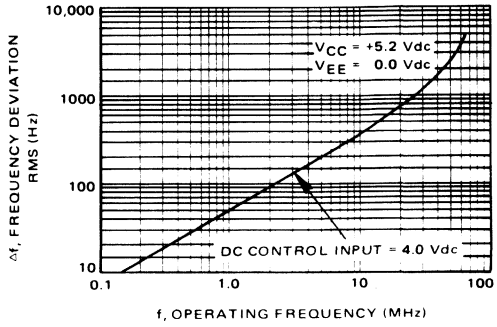


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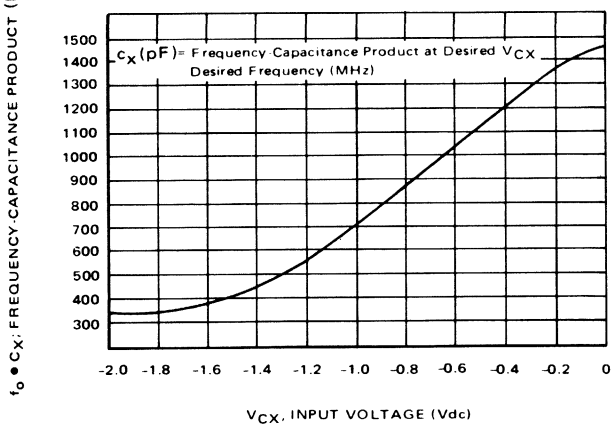
FIGURE 5 — FREQUENCY CAPACITANCE PRODUCT versus CONTROL VOLTAGE (V_{CX})

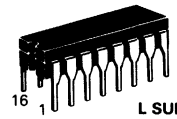


V_{EE} = −5.2 V, V_{CC} = 0 V.
FOR USE AT V_{EE} = 0 V, V_{CC} = +5 V (V_{CXP} = +5 V − V_{CX})
V_{CXP} = POSITIVE INPUT VOLTAGE.

MOTOROLA

MC1660

DUAL 4-INPUT OR/NOR GATE

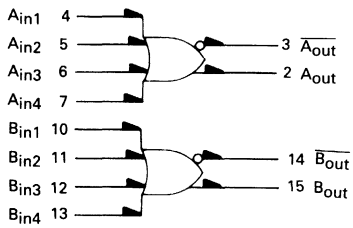


L SUFFIX
CERAMIC PACKAGE
CASE 620

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	—	—	—	28	—	—	mAdc
Input Current	I_{inH}	—	—	—	350	—	—	μAdc
Switching Times								ns
Propagation Delay	t^{+-}	0.6	1.8	0.6	1.7	0.6	1.9	
	t^{-+}	0.6	1.6	0.6	1.5	0.6	1.7	
Rise Time, Fall Time (10% to 90%)	t^+, t^-	0.6	2.2	0.6	2.1	0.6	2.3	ns

LOGIC DIAGRAM



$out = in1 + in2 + in3 + in4$

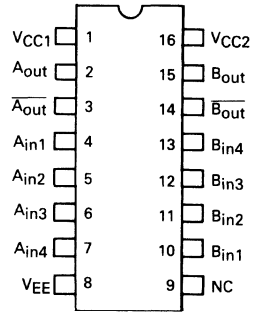
$\overline{out} = \overline{in1 + in2 + in3 + in4}$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510 ohm load)
= 1.1 ns typ (50 ohm load)

P_D = 120 mW typ/pkg (No load)
Full Load Current, I_L = −25 mAdc max

PIN ASSIGNMENT



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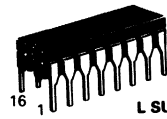
MOTOROLA

MC1662

QUAD 2-INPUT NOR GATE



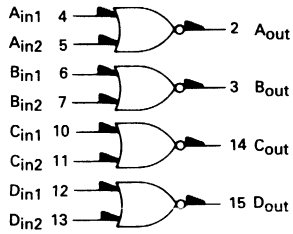
16 1

L SUFFIX
CERAMIC PACKAGE
CASE 620

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—	56	—	—	mAdc
Input Current	I_{inH}	—	—	—	350	—	—	μAdc
Switching Times Propagation Delay	t^{-+} t^{+-}	0.6 0.6	1.6 1.8	0.6 0.6	1.5 1.7	0.6 0.6	1.7 1.9	ns
Rise Time, Fall Time (10% to 90%)	t^+, t^-	0.6	2.2	0.6	2.1	0.6	2.3	ns

LOGIC DIAGRAM



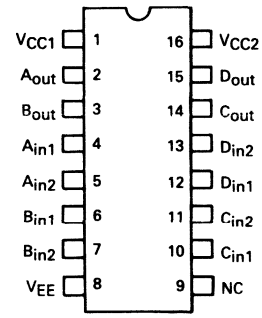
$out = \overline{in1 + in2}$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510 ohm load)
= 1.1 ns typ (50 ohm load)

P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = −25 mAdc max

PIN ASSIGNMENT



4

MOTOROLA

MC1670

MASTER-SLAVE FLIP-FLOP

Master slave construction renders the MC1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the "Master" portion of the flip-flop. The data present in the "Master" is transferred to the "Slave" when clock inputs (C1 "OR" C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 "OR" C2 is in the high state, the "Master" (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Power Dissipation = 220 mW typ (No Load)
f_{Tog} = 350 MHz typ

TRUTH TABLE

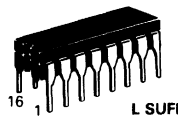
R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	⌐	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	⌐	H
L	L	H	H	Q_n

ϕ = Don't Care
ND = Not Defined
C = C1 + C2

ELECTRICAL CHARACTERISTICS

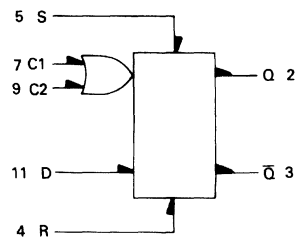
Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	—	—	—	48	—	—	mAdc
Input Current	I_{inH}							μAdc
Set, Reset		—	—	—	550	—	—	
Clock		—	—	—	250	—	—	
Data		—	—	—	270	—	—	
Switching Times								ns
Propagation Delay	t_{pd}	1.0	2.7	1.1	2.5	1.1	2.9	
Rise Time (10% to 90%)	t^+	0.9	2.7	1.0	2.5	1.0	2.9	ns
Fall Time (10% to 90%)	t^-	0.5	2.1	0.6	1.9	0.6	2.3	ns
Setup Time	$t_{S"1"}$	—	—	0.4	—	—	—	ns
	$t_{S"0"}$	—	—	0.5	—	—	—	
Hold Time	$t_{H"1"}$	—	—	0.3	—	—	—	ns
	$t_{H"0"}$	—	—	0.5	—	—	—	
Toggle Frequency	f_{Tog}	270	—	300	—	270	—	MHz

MASTER-SLAVE FLIP-FLOP



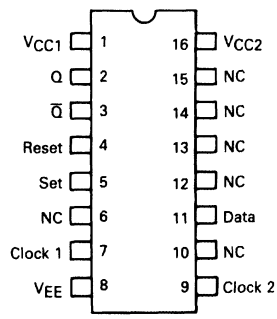
L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



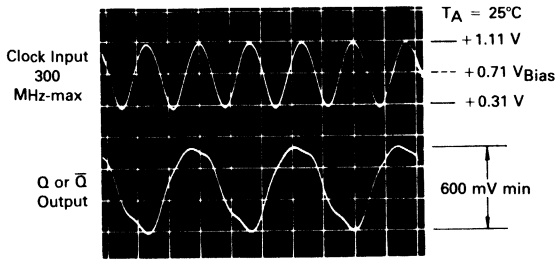
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN ASSIGNMENT



4

FIGURE 1 — TOGGLE FREQUENCY WAVEFORMS



The maximum toggle frequency of the MC1670 has been exceeded when either:

1. The output peak-to-peak voltage swing falls below 600 millivolts,
   OR
2. The device ceases to toggle (divide by two).

FIGURE 2 — MAXIMUM TOGGLE FREQUENCY (TYPICAL)

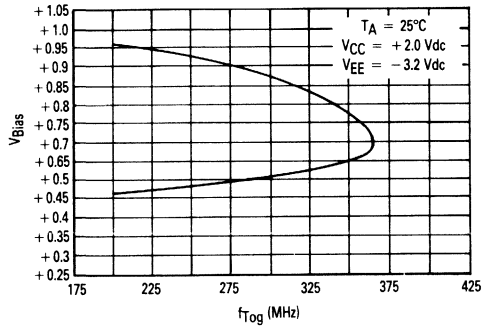
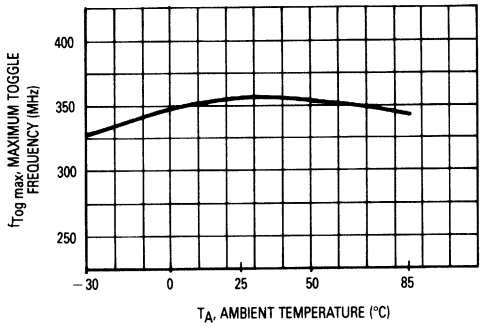


Figure 2 illustrates the variation in toggle frequency with the dc offset voltage (V_{Bias}) of the input clock signal.

Figures 4 and 5 illustrate minimum clock pulse width recommended for reliable operation of the MC1670.

4

FIGURE 3 — TYPICAL MAXIMUM TOGGLE FREQUENCY versus TEMPERATURE



Temperature	−30°C	+25°C	+85°C
V_{Bias}	+0.66 Vdc	+0.71 Vdc	+0.765 Vdc

Note: All power supply and logic levels are shown shifted 2.0 volts positive.

FIGURE 4 — MINIMUM "DOWN TIME" TO CLOCK
OUTPUT LOAD = 50 Ω

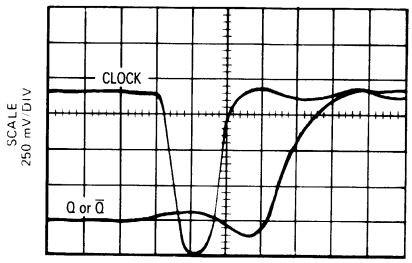
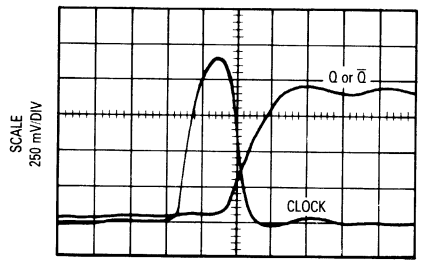


FIGURE 5 — MINIMUM "UP TIME" TO CLOCK
OUTPUT LOAD = 50 Ω

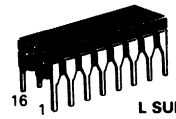


4

MOTOROLA

MC1672

TRIPLE 2-INPUT EXCLUSIVE-OR GATE

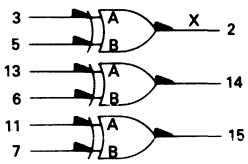


L SUFFIX
CERAMIC PACKAGE
CASE 620

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current		I_E	—	—	—	55	—	—	mAdc
Input Current									μAdc
	A Inputs	I_{inH}	—	—	—	350	—	—	
	B Inputs	I_{inH}	—	—	—	270	—	—	
Switching Times									ns
Propagation Delay	A Inputs	t^{++},t^{-+}	—	2.1	—	1.9	—	2.4	
		t^{+-},t^{--}	—	2.2	—	2.0	—	2.5	
	B Inputs	t^{++},t^{-+}	—	2.6	—	2.4	—	2.9	
		t^{+-},t^{--}	—	2.6	—	2.4	—	2.9	
Rise Time (10% to 90%)		t^{+}	—	2.7	—	2.5	—	2.9	ns
Fall Time (10% to 90%)		t^{-}	—	2.4	—	2.2	—	2.6	ns

LOGIC DIAGRAM



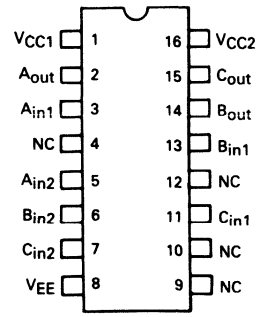
$X = A \bullet \overline{B} + \overline{A} \bullet B$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 1.1 ns typ (510 ohm load)
= 1.3 ns typ (50 ohm load)
P_D = 220 mW typ/pkg
Full Load Current, I_L = −25 mAdc max

Number at end of terminal denotes pin number for L package.

PIN ASSIGNMENT

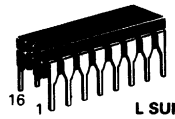


4

MOTOROLA

MC1690
OBSOLETE
USE MC12090

UHF PRESCALER
TYPE D FLIP-FLOP

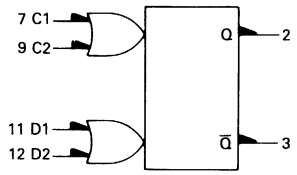


L SUFFIX
CERAMIC PACKAGE
CASE 620

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	—	—	—	—	59	—	—	mAdc
Input Current	I_{inH}								μAdc
Pins 7, 9		—	—	—	—	250	—	—	
Pins 11, 12		—	—	—	—	270	—	—	
Switching Times				Min	Typ	Max			ns
Propagation Delay	t_{pd}	—	—	—	1.5	—	—	—	
Rise Time, Fall Time (10% to 90%)	t^+, t^-	—	—	—	1.3	—	—	—	ns
Setup Time	t_{setup}	—	—	—	0.3	—	—	—	ns
Hold Time	t_{hold}	—	—	—	0.3	—	—	—	
Toggle Frequency	f_{Tog}	500	—	500	540	—	500	—	MHz

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

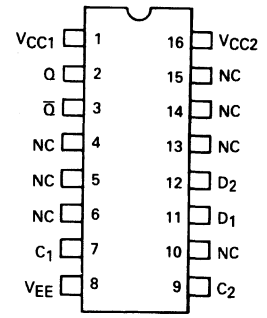
P_D = 200 mW typ/pkg (No Load)
f_{Tog} = 500 MHz min

TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	ϕ	Q_n
⎍	L	L
⎍	H	H

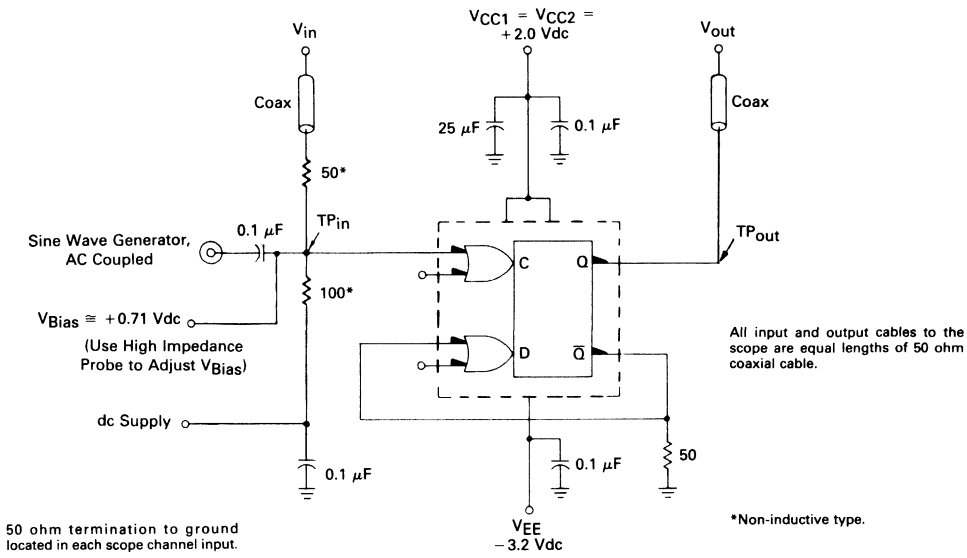
C = C1 + C2
D = D1 + D2
ϕ = Don't Care

PIN ASSIGNMENT



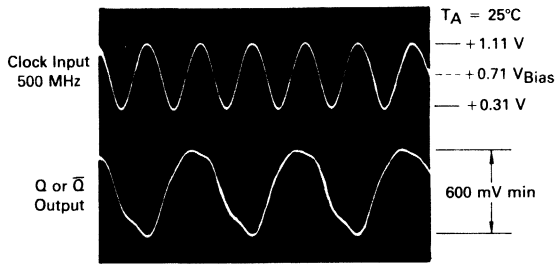
4

FIGURE 1 — TOGGLE FREQUENCY TEST CIRCUIT



4

FIGURE 2 — TOGGLE FREQUENCY WAVEFORMS



The maximum toggle frequency of the MC1690 has been exceeded when either:

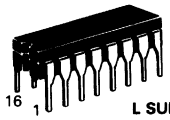
1. The output peak-to-peak voltage swing falls below 600 millivolts,
   OR
2. The device ceases to toggle (divide-by-two).

Note: All power supply and logic levels are shown shifted 2.0 volts positive.

MOTOROLA

MC1692

QUAD LINE RECEIVER



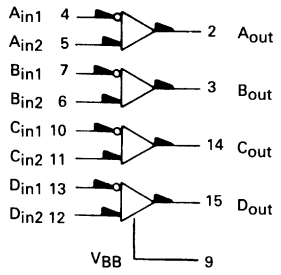
16 1

L SUFFIX
CERAMIC PACKAGE
CASE 620

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—	50	—	—	mAdc
Input Current	I_{in}	—	—	—	250	—	—	μAdc
Input Leakage Current	I_R	—	—	—	100	—	—	μAdc
Reference Voltage	V_{BB}	−1.375	−1.275	−1.35	−1.25	−1.3	−1.2	Vdc
Switching Times Propagation Delay	t^{-+}	0.6	1.6	0.6	1.5	0.6	1.7	ns
	t^{+-}	0.6	1.8	0.6	1.7	0.6	1.9	
Rise Time, Fall Time (10% to 90%)	t^+, t^-	0.6	2.2	0.6	2.1	0.6	2.3	ns

LOGIC DIAGRAM

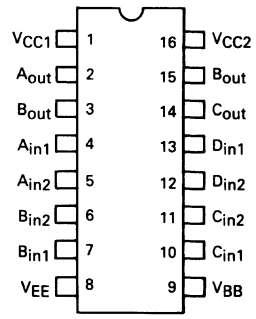


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510 ohm load)
= 1.1 ns typ (50 ohm load)

P_D = 220 mW typ/pkg (No Load)
Full Load Current, I_L = −25 mAdc max

PIN ASSIGNMENT



4

APPLICATION INFORMATION

The MC1692 quad line receiver is used primarily to receive data from balanced twisted pair lines, as indicated in Figure 1. The line is driven with a MC1660 OR/NOR gate. The MC1660 is terminated with 50 ohm resistors to −2.0 volts. At the end of the twisted pair a 100 ohm termination resistor is placed across the differential line receiver inputs of the MC1692. Illustrated in Figure 2 is the sending and receiving waveforms at a data rate of 400 megabits per second over an 18 foot twisted pair cable. The waveform picture of Figure 3 shows a 5.0 nanosecond pulse being propagated down the 18 foot line. The delay time for the line is 1.68 ns/foot.

The MC1692 may also be applied as a high frequency schmitt trigger as illustrated in Figure 4. This circuit has been used in excess of 200 MHz. The MC1692 when loaded into 50 ohms will produce an output rising edge of about 1.5 nanoseconds.

FIGURE 1 — LINE DRIVER/RECEIVER

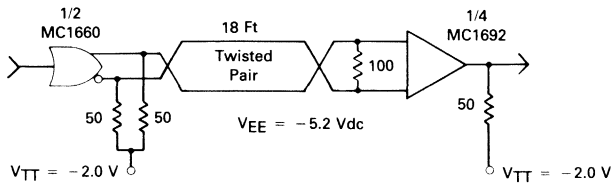


FIGURE 2 — 400 MBS WAVEFORMS

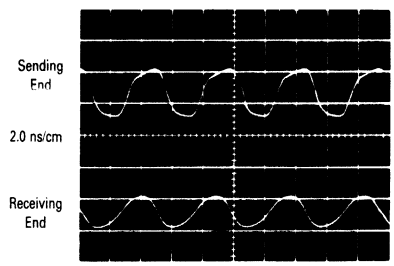


FIGURE 3 — PULSE PROPAGATION WAVEFORMS

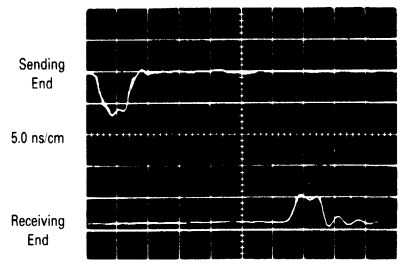
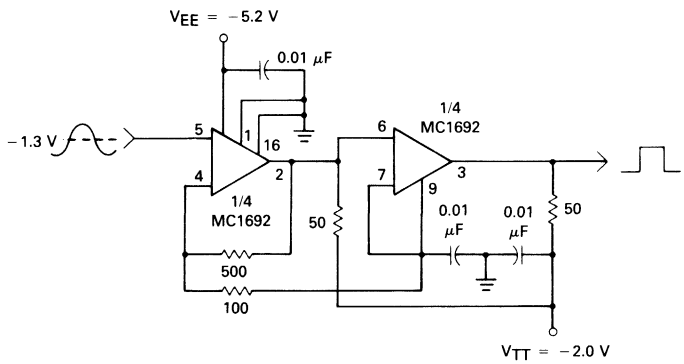


FIGURE 4 — 200 MHz SCHMITT TRIGGER



MECL Memories

Selector Guide | **Data Sheets** | **5**

MECL Memories
INTEGRATED CIRCUITS

Device	Organization (Word x Bit)	Access Time	Pins	Case
ECL 10K, 10H				
MC10H145	16 x 4	6	16	620, 648, 775
MCM10145	16 x 4	15	16	620
MCM10146	1024 x 1	29	16	620

Device	Organization (Word x Bit)	Access Time	Pins	Case
PROMS				
MCM10149*25	256 + 4	25	16	620

5

MOTOROLA

MCM10145

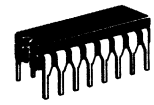
64-BIT REGISTER FILE (RAM)

The MCM10145 is a 64-Bit RAM organized as a 16 x 4 array. This organization and the high speed make the MCM10145 particularly useful in register file or small scratch pad applications. Fully decoded inputs, together with a chip enable, provide expansion of memory capacity. The Write Enable input, when low, allows data to be entered; when high, disables the data inputs. The Chip Select input when low, allows full functional operation of the device; when high, all outputs go to a low logic state. The Chip Select, together with open emitter outputs allow full wire-ORing and data bussing capability. On-chip input pulldown resistors allow unused inputs to remain open.

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 4.5 ns
- Operating Temperature Range = 0° to +75°C
- 50 kΩ Pulldown Resistors on All Inputs
- Fully Compatible with MECL 10,000
- Pin-for-Pin Compatible with the F10145

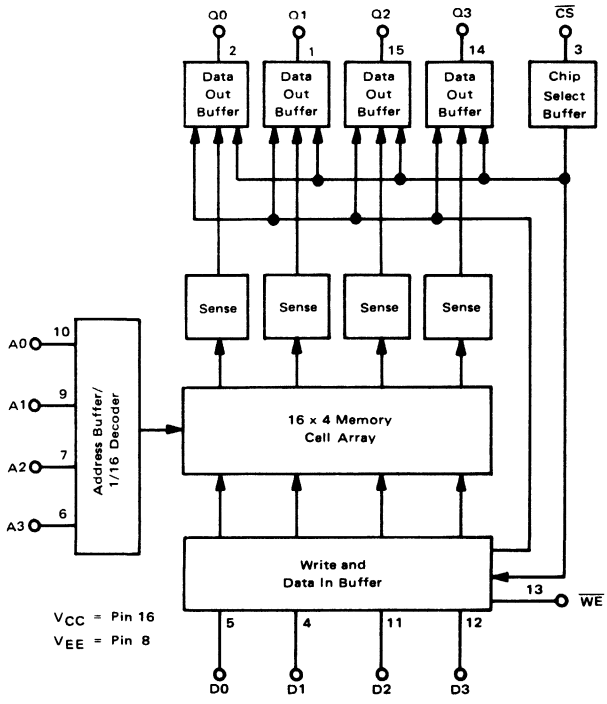
MECL

64-BIT REGISTER FILE (RAM)

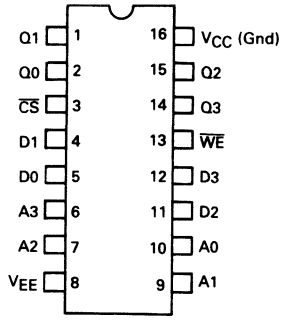


L SUFFIX
CERAMIC PACKAGE
CASE 620

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

$\overline{CS}$	Chip Select Input
A0 thru A3	Address Inputs
D0 thru D3	Data Inputs
Q0 thru Q3	Data Outputs
$\overline{WE}$	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

5

FUNCTIONAL DESCRIPTION:

The MCM10145 is a 16 word x 4-bit RAM. Bit selection is achieved by means of a 4-bit address A0 thru A3.

The active-low chip select allows memory expansion up to 32 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_n is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at Q_n.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current – Continuous – Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

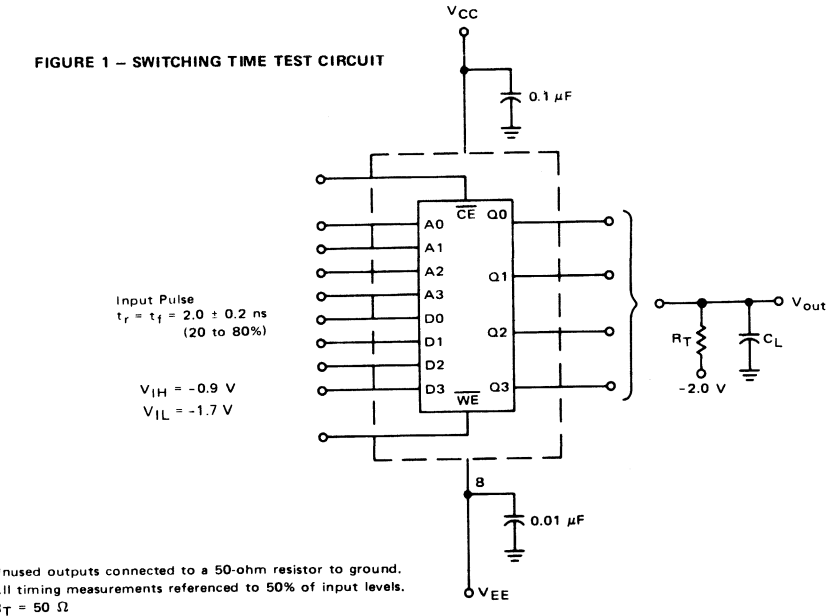
DC Characteristics	Symbol	MCM10145 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	130	–	125	–	120	mAdc	Typ I_{EE} @ 25°C = 90 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	µAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	µAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = −5.2 Vdc ±5°; Output Load see Figure 1; see Note 2.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.5	8.0	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	5.0	8.0	ns	output. See Note 1.
Address Access Time	t_{AA}	4.0	10	15	ns	
Write Mode						
Write Pulse Width	t_W	8.0	–	–	ns	t_{WSA} = 5 ns
Data Setup Time Prior to Write	t_{WSD}	0	-6.0	–	ns	Measured at 50% of input to 50% of
Data Hold Time After Write	t_{WHD}	3.0	0	–	ns	output.
Address Setup Time Prior to Write	t_{WSA}	5.0	1.0	–	ns	t_W = 8 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	1.0	-3.0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	0	-5.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	0	-6.0	–	ns	
Write Disable Time	t_{WS}	2.0	5.0	8.0	ns	
Write Recovery Time	t_{WR}	2.0	5.0	8.0	ns	
Chip Enable Strobe Mode						
Data Setup Prior to Chip Select	t_{CSD}	0	-6.0	–	ns	Guaranteed but not tested on standard
Write Enable Setup Prior to Chip Select	t_{CSW}	0	-3.0	–	ns	product. See Figure 5.
Address Setup Prior to Chip Select	t_{CSA}	0	-3.0	–	ns	
Data Hold Time After Chip Select	t_{CHD}	2.0	-1.0	–	ns	
Write Enable Hold Time After Chip Select	t_{CHW}	0	-6.0	–	ns	
Address Hold Time After Chip Select	t_{CHA}	4.0	-1.0	–	ns	
Chip Select Minimum Pulse Width	t_{CS}	18	12	–	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Address to Output	t_r, t_f	1.5	3.0	7.0	ns	
$\overline{CS}$ to Output	t_r, t_f	1.5	3.0	5.0	ns	
Capacitance						
Input Capacitance	C_{in}	–	4.0	6.0	pF	
Output Capacitance	C_{out}	–	5.0	8.0	pF	

Notes:
1. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
2. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



Unused outputs connected to a 50-ohm resistor to ground.
All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (Including Jig and Stray Capacitance)
Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.

5

FIGURE 2 – CHIP SELECT ACCESS TIME

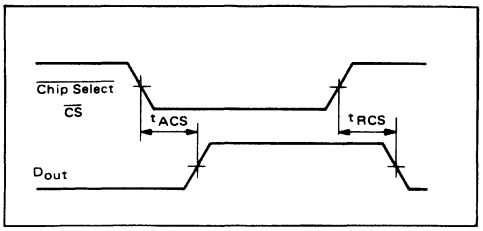


FIGURE 3 – ADDRESS ACCESS TIME

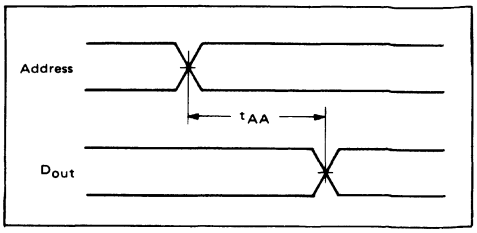


FIGURE 4 – WRITE MODE

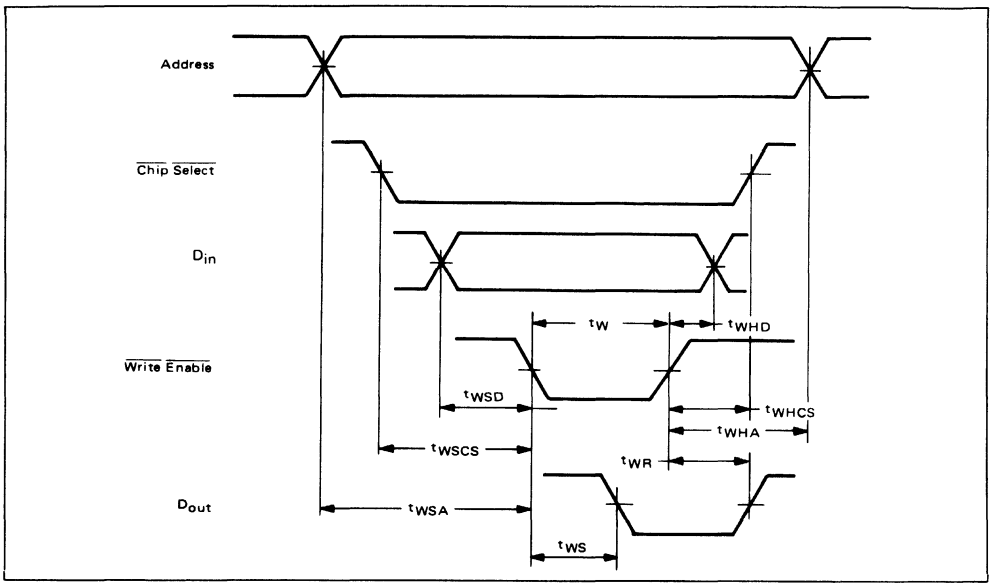
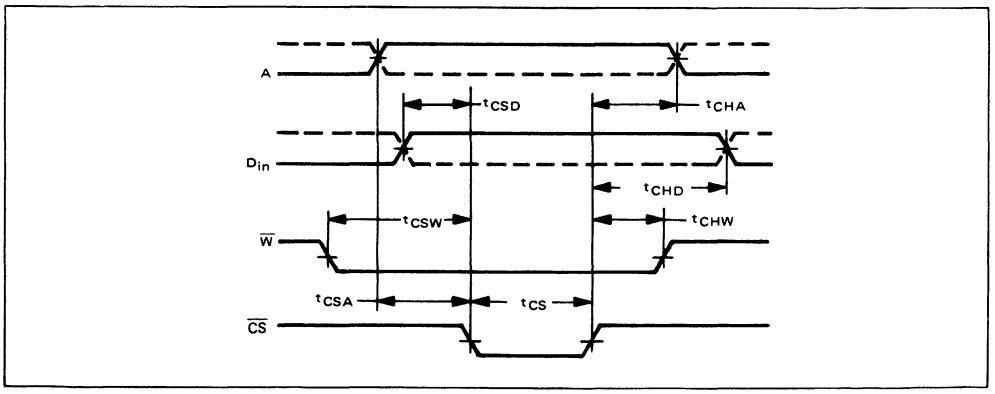


FIGURE 5 – CHIP ENABLE STROBE MODE



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MOTOROLA

MCM10146

1024 x 1-BIT RANDOM ACCESS MEMORY

The MCM10146 is a 1024-bit Read/Write Random Access Memory organized 1024 words by 1 bit. Data is selected or stored by means of a 10-bit address (A0 through A9) decoded on the chip. The chip is designed with a separate data in line, a non-inverting data output, and an active-low chip select.

This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

- Fully Compatible with MECL 10,000
- Temperature Range of 0° to 75°C (see note 1)
- Emitter-Follower Output Permits Full Wire-ORing (see note 3)
- Power Dissipation Decreases with Increasing Temperature
- Typical Address Access of 24 ns
- Typical Chip Select Access of 4.0 ns

PIN DESIGNATION

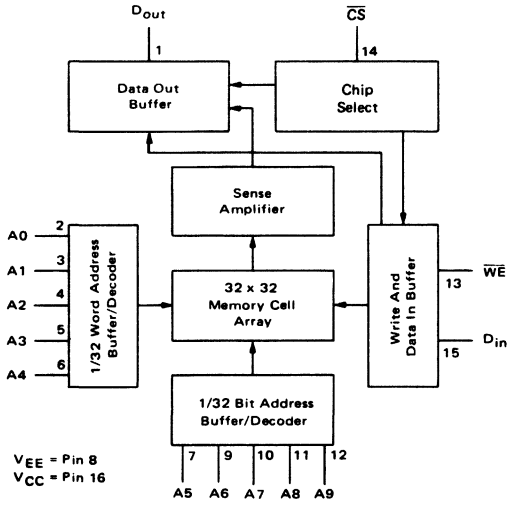
CS	Chip Select Input
A0 to A9	Address Inputs
D_{in}	Data Inputs
D_{out}	Data Output
WE	Write Enable Input

MECL

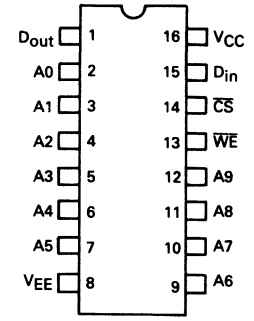
1024 X 1-BIT RANDOM ACCESS MEMORY

L SUFFIX
CERAMIC PACKAGE
CASE 620

BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

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FUNCTIONAL DESCRIPTION:

This device is a 1024 x 1-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

The operating mode of the RAM (CS input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at D_{out}. (See Truth Table)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

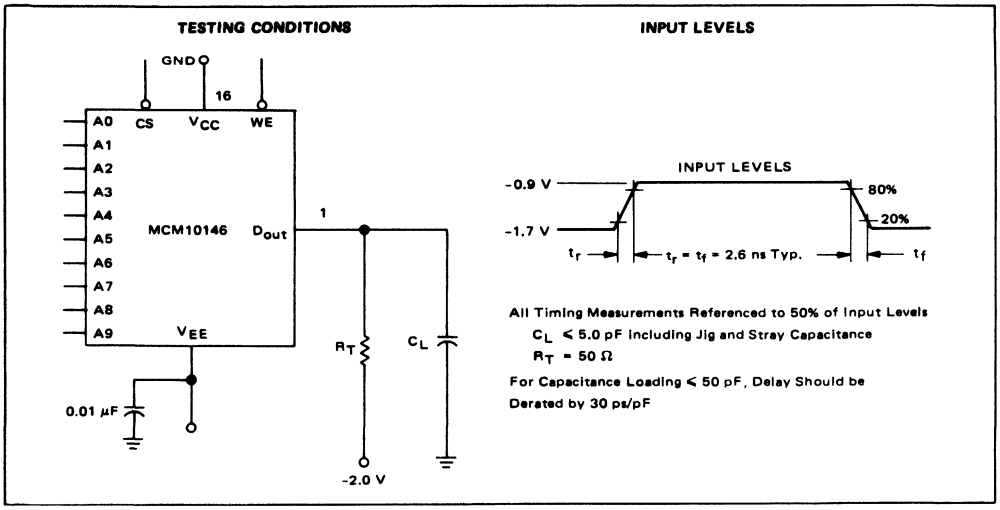
	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

		MCM10146 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}		150		145		125	mAdc	Typ I_{EE} @ 25°C = 100 mA All outputs and inputs open. Measure pin 8.
Input Current High	I_{inH}	—	220	—	220	—	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	—	-0.980	—	-0.920	—	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	—	-1.645	—	-1.630	—	-1.605	Vdc	

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS



Guaranteed with V_{EE} = -5.2 Vdc ± 5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10146 Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.0	7.0	ns	Measured at 50% of input to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	4.0	7.0	ns	See Note 2.
Address Access Time	t_{AA}	8.0	24	29	ns	
Write Mode						See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	25	20	–	ns	t_{WSA} = 8.0 ns. Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	5.0	0	–	ns	
Data Hold Time After Write	t_{WHD}	5.0	0	–	ns	
Address Setup Time Prior to Write	t_{WSA}	8.0	0	–	ns	t_W = 25 ns
Address Hold Time After Write	t_{WHA}	2.0	0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	5.0	0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	5.0	0	–	ns	
Write Disable Time	t_{WS}	2.8	5.0	7.0	ns	
Write Recovery Time	t_{WR}	2.8	5.0	7.0	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	2.5	4.0	ns	When driven from $\overline{CS}$ or $\overline{WE}$ inputs.
Output Rise and Fall Time	t_r, t_f	1.5	4.0	8.0	ns	When driven from Address inputs.
Capacitance						Measured with a pulse technique.
Input Lead Capacitance	C_{in}	–	4.0	5.0	pF	
Output Lead Capacitance	C_{out}	–	7.0	8.0	pF	

Notes:

(1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.

(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

(4) Typical limits are at V_{EE} = -5.2 Vdc, T_A = 25°C and standard loading.

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FIGURE 2 – CHIP SELECT ACCESS TIME

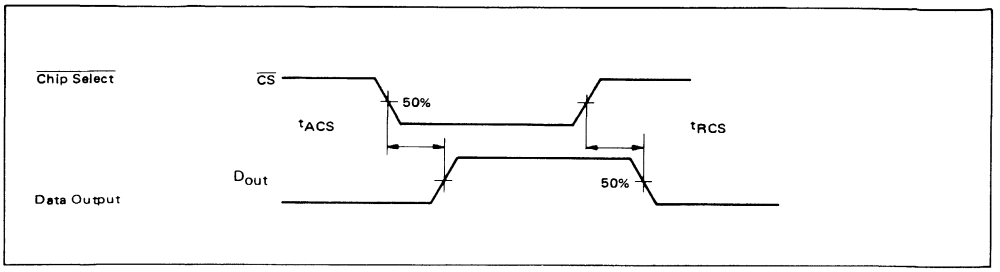


FIGURE 3 – ADDRESS ACCESS TIME

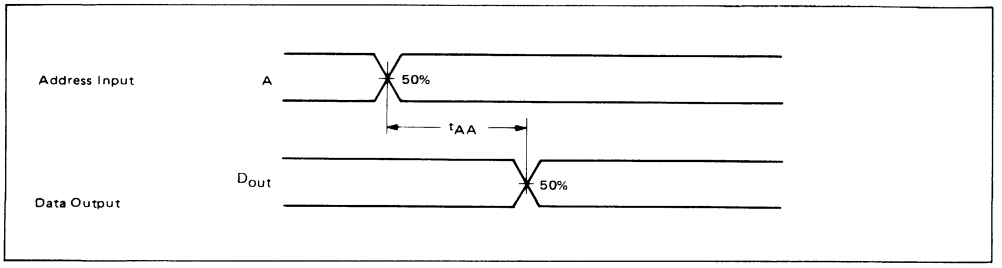
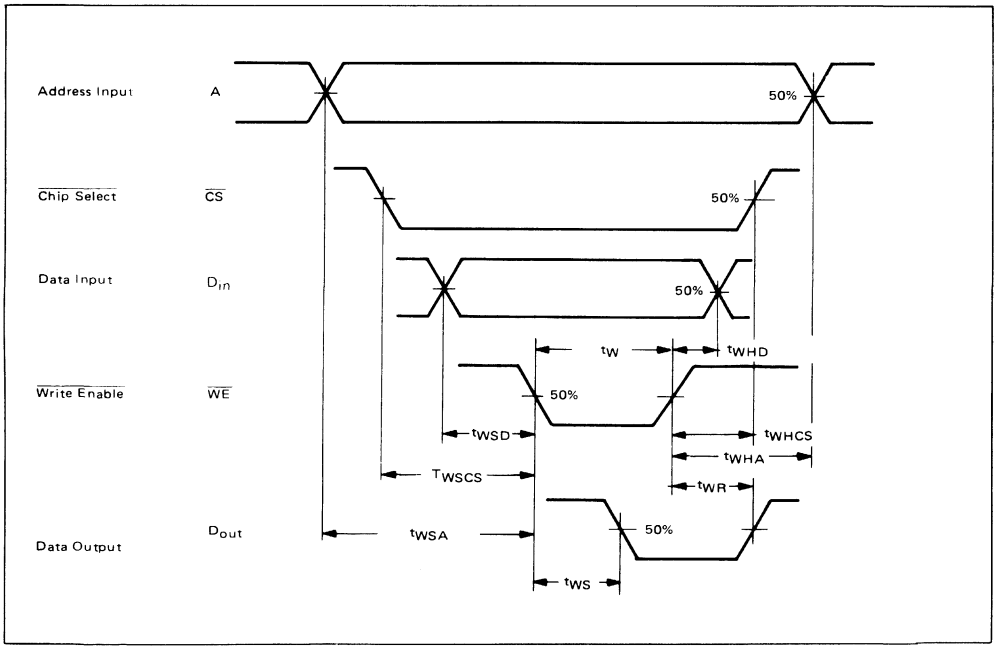


FIGURE 4 – WRITE STROBE MODE



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MOTOROLA

MCM10149*25

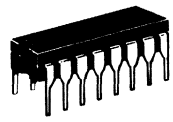
256 x 4-BIT PROGRAMMABLE READ-ONLY MEMORY

This device is a 256-word x 4-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

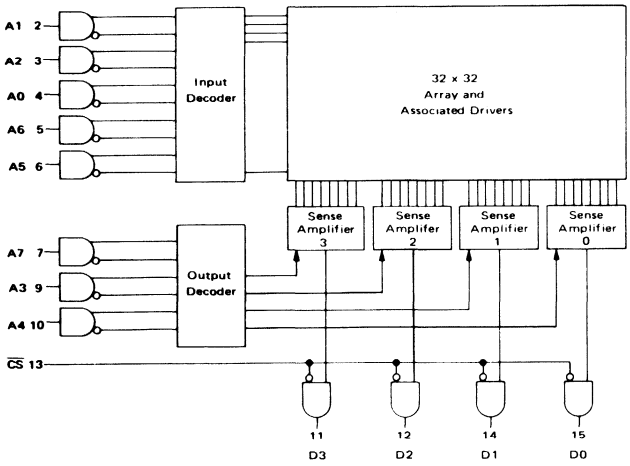
- Typical Address Access Time of 20 ns
- Typical Chip Select Access Time of 8.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (540 mW typ @ 25°C) Decreases with Increasing Temperature

MECL

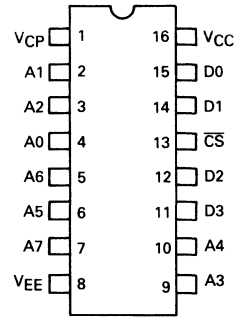
1024-BIT PROGRAMMABLE READ-ONLY MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620



PIN ASSIGNMENT



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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	0°C		+25°C		+75°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	155	–	150	–	145	mAdc
Input Current High	I_{inH}	–	265	–	265	–	265	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

Forcing Function	Parameter	0°C	25°C①	75°C①
V_{IHmax} =	V_{OHmax}	−0.840	−0.810	−0.720
	V_{OHmin}	−1.000	−0.960	−0.900
	V_{OHAmin}	−1.020	−0.980	−0.920
V_{IHAmin}		−1.130	−1.105	−1.045
V_{ILAmax}		−1.490	−1.475	−1.450
	V_{OLAmax}	−1.645	−1.630	−1.605
	V_{OLmax}	−1.665	−1.650	−1.625
V_{ILmin} =	V_{OLmin}	−1.870	−1.850	−1.830
V_{ILmin}	I_{NLmin}	0.5	0.5	0.3

NOTES: ① 0–75°C temperature range, 50Ω to -2.0V.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10149*25 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		Unit	Conditions
		Min	Max		
Read Mode				ns	Measured from 50% of input to 50% of output. See Note 1.
Chip Select Access Time	t_{ACS}	2.0	10		
Chip Select Recovery Time	t_{RCS}	2.0	10		
Address Access Time	t_{AA}	7.0	25		
Rise and Fall Time	t_r, t_f	1.5	7.0	ns	Measured between 20% and 80% points.
Capacitance				pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	5.0		
Output Capacitance	C_{out}	—	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10149;
$C_L \leq 5.0$ pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.
4. $V_{CP} = V_{CC}$ = Gnd for normal operation.

*To be determined; contact your Motorola representative for up-to-date information.

PROGRAMMING THE MCM10149 †

During programming of the MCM 10149, input pins 7, 9, and 10 are addressed with standard MECL 10K logic levels. However, during programming input pins 2, 3, 4, 5, and 6 are addressed with $0 V \leq V_{IH} \leq +0.25$ V and $V_{EE} \leq V_{IL} \leq -3.0$ V. It should be stressed that this deviation from standard input levels is required only during the programming mode. During normal operation, standard MECL 10,000 input levels must be used.

With these requirements met, and with $V_{CP} = V_{CC} =$ 0 V and $V_{EE} = -5.2$ V ± 5%, the address is set up. After a minimum of 100 ns delay, V_{CP} (pin 1) is ramped up to + 12 V ± 0.5 V (total voltage V_{CP} to V_{EE} is now 17.2 V, + 12 V − [− 5.2 V]). The rise time of this V_{CP} voltage pulse should be in the 1 − 10 μs range, while its pulse width (t_{W1}) should be greater than 100 μs but less than 1 ms. The V_{CP} supply current at + 12 V will be approximately 525 mA while current drain from V_{CC} will be approximately 175 mA. A current limit should therefore be

set on both of these supplies. The current limit on the V_{CP} supply should be set at 700 mA while the V_{CC} supply should be limited to 250 mA. It should be noted that the V_{EE} supply must be capable of sinking the combined current of the V_{CC} and V_{CP} supplies while maintaining a voltage of -5.2 V ± 5%.

Coincident with, or at some delay after the V_{CP} pulse has reached its 100% level, the desired bit to be fused can be selected. This is done by taking the corresponding output pin to a voltage of +2.85 V ± 5%. It is to be noted that only one bit is to be fused at a time. The other three unselected outputs should remain terminated through their 50 ohm load resistor to -2.0 V. Current into the selected output is 5.0 mA maximum.

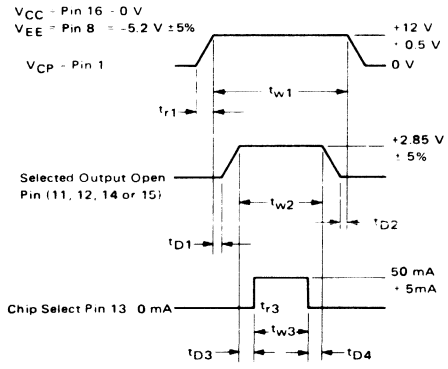
After the bit select pulse has been applied to the appropriate output, the fusing current is sourced out of the chip select pin 13. The 0% to 100% rise time of this current pulse should be 250 ns max. Its pulse width should be greater than 100 μs. Pulse magnitude is 50 mA ± 5.0 mA. The voltage clamp on this current source is to be -6.0 V.

After the fusing current source has returned 0 mA, the bit select pulse is returned to its initial level, i.e., the output is returned through its load to -2.0 V. Thereafter, V_{CP} is returned to 0 V. Strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} has returned to 0 V. The remaining bits are programmed in a similar fashion.

† NOTE: For devices that program incorrectly, return serialized units with individual truth tables. Noncompliance voids warranty.

PROGRAMMING SPECIFICATIONS

The following timing diagrams and fusing information represent programming specifications for the MCM10149.



The timing diagram is shown for programming one bit. Note that only one bit is blown at a time. All addressing must be done 100 ns prior to the beginning of the V_{CP} pulse, i.e., V_{CP} = 0 V. Likewise, strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} returns to 0 V.

Note that the fusing current is defined as a positive current out of the chip select, pin 13. A programming duty cycle of ≤ 15% is to be observed.

Definitions and values of timing symbols are as follows.

Symbol	Definition	Value
t_{r1}	Rise Time, Programming Voltage	≥ 1 μs
t_{w1}	Pulse Width, Programming Voltage	≥ 100 μs < 1 ms
t_{D1}	Delay Time, Programming Voltage Pulse to Bit Select Pulse	≥ 0
t_{w2}	Pulse Width, Bit Select	≥ 100 μs
t_{D2}	Delay Time, Bit Select Pulse to Programming Voltage Pulse	≥ 0
t_{D3}	Delay Time, Bit Select Pulse to Programming Current Pulse	≥ 1 μs
t_{r3}	Rise Time, Programming Current Pulse	250 ns max
t_{w3}	Pulse Width, Programming Current Pulse	≥ 100 μs
t_{D4}	Delay Time, Programming Current Pulse to Bit Select Pulse	≥ 1 μs

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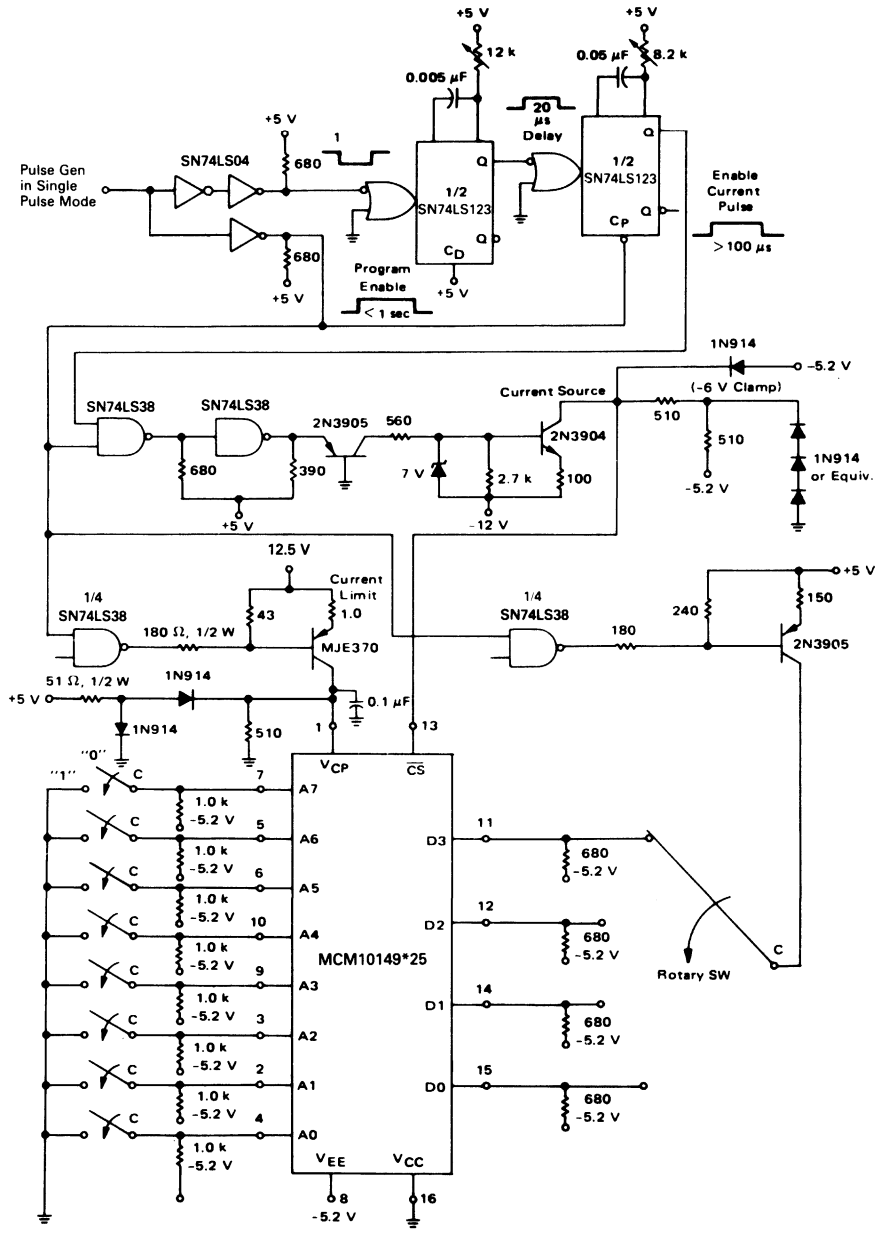
MANUAL PROGRAMMING CIRCUIT



Phase-Locked Loop

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PHASE-LOCKED LOOP
INTEGRATED CIRCUITS

Motorola offers the designer an array of devices to perform phase-locked loop functions, such as prescalers, phase detectors, and oscillators.

Description	Pins	Device	Temp	DIP'S	SM
Control Function					
Counter Control Logic	16	MC12014	0 to +75°C	P,L	
Counter					
Dual Voltage-Controlled Multivibrator	14	MC4024	0 to +75°C	P,L	
Dual Voltage-Controlled Multivibrator	14	MC4324	−55° to +125°C	P,L	
Programmable Modulo-N Counters (N = 0–9)	16	MC4016	0 to +75°C	P,L	
Programmable Modulo-N Counters (N = 0–9)	16	MC4018	0 to +75°C	P,L	
Programmable Modulo-N Counters (N = 0–9)	16	MC4316	−55° to +125°C	P,L	
Detector					
Analog Mixer	14	MC12002	−30° to +85°C	P,L	
Phase-Frequency Detector	14	MC4044	0 to +75°C	P,L	
Phase-Frequency Detector	14	MC4344	−55° to +125°C	P,L	
Phase-Frequency Detector	14	MC12040	0 to +75°C	P,L	FN
Oscillator					
130 MHz Voltage-Controlled Multivibrator	20	MC12101	0 to +75°C	P	FN
200 MHz Voltage-Controlled Multivibrator	20	MC12100	0 to +75°C	P	FN
Crystal Oscillator	16	MC12061	0 to +75°C	P,L	
Low Power Voltage-Controlled Oscillator	8	MC12148	−40° to +85°C		D,SD
Voltage-Controlled Multivibrator	16	MC1658	−30° to +85°C	P,L	D,FN
Voltage-Controlled Oscillator	14	MC1648	−30° to +85°C	P,L	D,FN
Prescaler					
1.1 GHz ÷256 Prescaler	8	MC12074	0 to +70°C	P	D
1.1 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	MC12028A	−40° to +85°C	P	D
1.1 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	MC12028B	−40° to +85°C	P	D
1.1 GHz ÷64 Prescaler	8	MC12073	0 to +70°C	P	D
1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	MC12022A	−40° to +85°C	P	D
1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	MC12022B	−40° to +85°C	P	D
1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	MC12022SLA	−40° to +85°C	P	D
1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	MC12022SLB	−40° to +85°C	P	D
1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	MC12022TSA	−40° to +85°C	P	D
1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	MC12022TSB	−40° to +85°C	P	D
1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler with Stand-By Mode	8	MC12036A	−40° to +85°C	P	D
1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler with Stand-By Mode	8	MC12036B	−40° to +85°C	P	D
1.1 GHz ÷64/65, ÷128/129 Low Power Dual Modulus Prescaler	8	MC12052A	−40° to +85°C	P	D
1.1 GHz ÷64/65, ÷128/129 Low Power Dual Modulus Prescaler	8	MC12052B	−40° to +85°C	P	D
1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	MC12022LVA	−40° to +85°C	P	D
1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	MC12022LVB	−40° to +85°C	P	D
1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	MC12022TVA	−40° to +85°C	P	D
1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	MC12022TVB	−40° to +85°C	P	D
1.3 GHz ÷256 Prescaler	8	MC12076	0 to +85°C	P	D
1.3 GHz ÷256 Prescaler	8	MC12078	0 to +85°C	P	D
2.0 GHz ÷32/33, ÷64/65, Dual Modulus Prescaler	8	MC12034A	−40° to +85°C	P	D
2.0 GHz ÷32/33, ÷64/65, Dual Modulus Prescaler	8	MC12034B	−40° to +85°C	P	D
2.0 GHz ÷32/33, ÷64/65 Low Voltage Dual Modulus Prescaler	8	MC12033A	−40° to +85°C	P	D
2.0 GHz ÷32/33, ÷64/65 Low Voltage Dual Modulus Prescaler	8	MC12033B	−40° to +85°C	P	D
2.0 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	MC12032A	−40° to +85°C	P	D
2.0 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	MC12032B	−40° to +85°C	P	D
2.0 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	MC12031A	−40° to +85°C	P	D
2.0 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	MC12031B	−40° to +85°C	P	D
225 MHz ÷20/21 Dual Modulus Prescaler	8	MC12019	−40° to +85°C	P,L	D
225 MHz ÷32/33 Dual Modulus Prescaler	8	MC12015	−40° to +85°C	P,L	D
225 MHz ÷40/41 Dual Modulus Prescaler	8	MC12016	−40° to +85°C	P,L	D
225 MHz ÷64 Prescaler	8	MC12023	0 to +70°C	P	D
225 MHz ÷64/65 Dual Modulus Prescaler	8	MC12017	−40° to +85°C	P,L	D
480 MHz ÷5/6 Dual Modulus Prescaler	16	MC12009	−30° to +85°C	P,L	
520 MHz ÷128/129 Dual Modulus Prescaler	8	MC12018	−40° to +85°C	P,L	D
520 MHz ÷64/65 Dual Modulus Prescaler	8	MC12025	−40° to +85°C	P	D
550 MHz ÷10/11 Dual Modulus Prescaler	16	MC12013	−30° to +85°C	P,L	
550 MHz ÷8/9 Dual Modulus Prescaler	16	MC12011	−30° to +85°C	P,L	
750 MHz ÷2 UHF Prescaler	16	MC12090	0 to +75°C	P,L	

MOTOROLA

MC4316
MC4016
MC4018

PROGRAMMABLE MODULO-N COUNTERS

The monolithic devices are programmable, cascadable, modulo-N-counters. The MC4316/4016 can be programmed to divide by any number (N) from 0 thru 9, the MC4018 from 0 thru 15.

The parallel enable ($\overline{PE}$) input enables the parallel data inputs D0 thru D3. All zeros are entered into the counter by applying a logic "0" level to the master reset ($\overline{MR}$) and $\overline{PE}$ inputs. This causes the counter to stop counting (count = 0). All data inputs are independent of the logic level of the Clock.

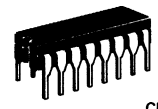
Modulo-N counters are useful in frequency synthesizers, in phase-locked loops, and in other applications where a simple method for frequency division is needed.

All Types:

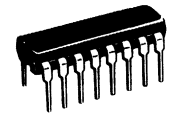
Input Loading Factor:
Clock, $\overline{PE}$ = 2
D0, D1, D2, D3, Gate = 1
$\overline{MR}$ = 4
Output Loading Factor = 8

Total Power Dissipation = 250 mW typ/pkg
Propagation Delay Time:
Clock to Q3 = 50 ns typ
Clock to Bus = 35 ns typ

PROGRAMMABLE MODULO-N COUNTERS



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

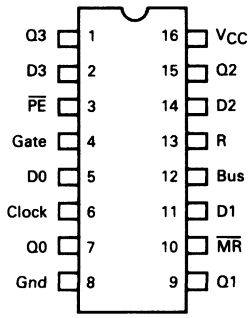
PIN ASSIGNMENT

MC4316/4016

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC4316/4016
MC4018

V_{CC} = Pin 16
Gnd = Pin 8

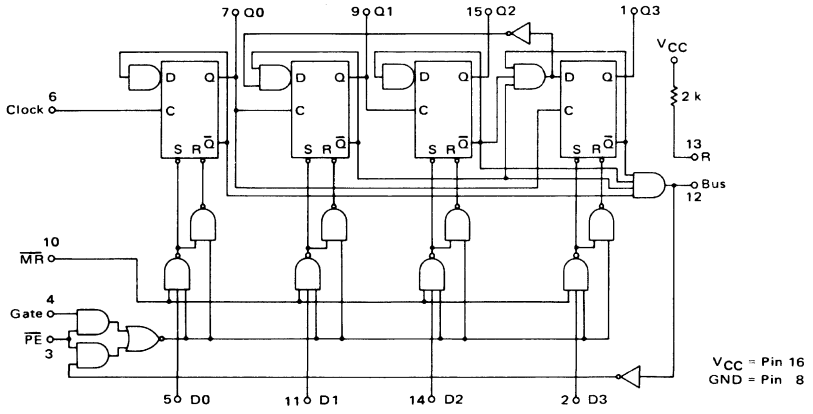


MC4018

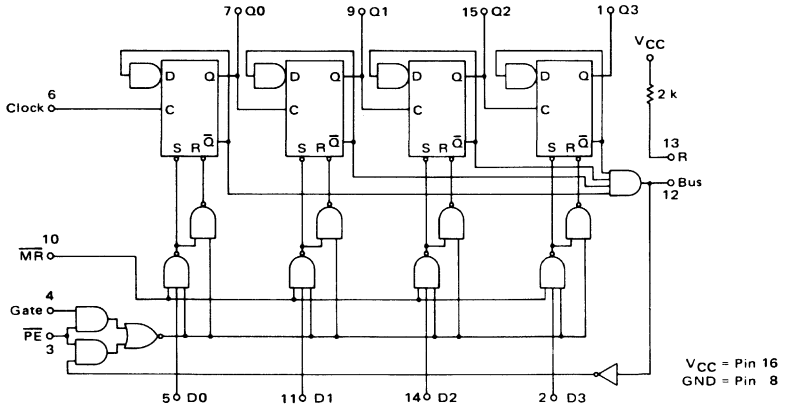
COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

LOGIC DIAGRAMS

MC4316/4016



MC4018



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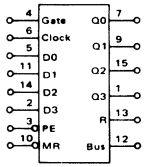
ELECTRICAL CHARACTERISTICS

Tests are shown for one output only.
Others are tested in the same manner.

MC4316/4016
MC4018

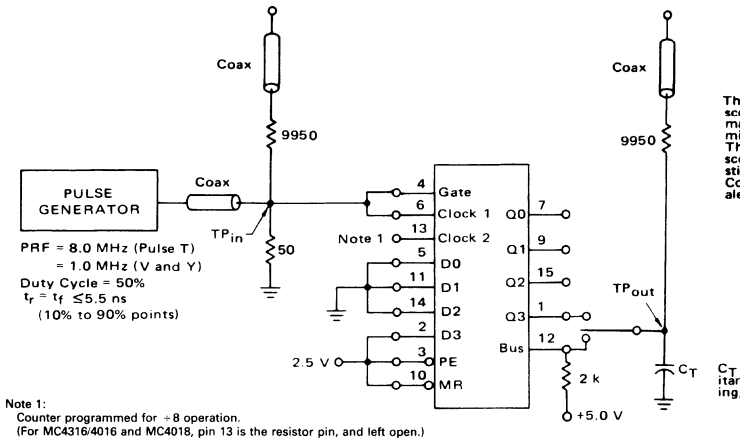


	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OL3}	I_{OH}	I_{IC}	Volts V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{CC}	V_{CCL}	V_{CCH}
MC4316	-55°C	12.8	13.8	9.6	-1.6	–	0.4	2.4	5.5	0.8	2.0	5.0	4.5	5.5
	+25°C	12.8	13.8	9.6	-1.6	-10	0.4	2.4	5.5	0.8	2.0	5.0	4.5	5.5
	+125°C	12.8	13.8	9.6	-1.6	–	0.4	2.4	5.5	0.8	2.0	5.0	4.5	5.5
MC4016/4018	0°C	12.8	13.8	9.6	-1.6	–	0.4	2.5	5.5	0.8	2.0	5.0	4.75	5.25
	+25°C	12.8	13.8	9.6	-1.6	-10	0.4	2.5	5.5	0.8	2.0	5.0	4.75	5.25
	+75°C	12.8	13.8	9.6	-1.6	–	0.4	2.5	5.5	0.8	2.0	5.0	4.75	5.25

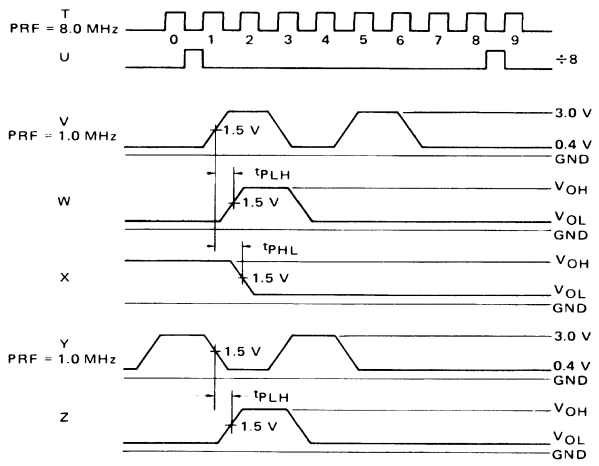
Characteristic	Symbol	Pin Under Test	MC4316 -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4016/4018 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW I_{OL1}	I_{OL2}	I_{OL3}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																													
Forward Current	I_{IL1}	2	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	mAdc						2	10	–					16	3,8
		3	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2							3	4	–						8,12
		4	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6							4	3	–						8
		5	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6							5	10	–						3,8
		6	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2							6		–						8
		10	–	-6.4	–	-6.4	–	-6.4	–	-6.4	–	-6.4	–	-6.4							10	2,5,11,14	–						3,8
		11	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6							11	10	–						
		14	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6							14	10	–						
	I_{IL2}	2	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	mAdc						2	10	–					16	3,8
		3	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8							3	4	–						8,12
		4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4							4	3	–						8
		5	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4							5	10	–						3,8
		6*	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8							6		–						8
		10	–	-5.6	–	-5.6	–	-5.6	–	-5.6	–	-5.6	–	-5.6							10	2,5,11,14	–						3,8
		11	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4							11	10	–						
		14	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4							14	10	–						
Leakage Current	I_{IH}	2	–	40	–	40	–	40	–	40	–	40	–	40	μAdc							2	–					16	8,10
		3	–	80	–	80	–	80	–	80	–	80	–	80								3	–						4,8
		4	–	40	–	40	–	40	–	40	–	40	–	40								4	–						3,8
		5	–	40	–	40	–	40	–	40	–	40	–	40								5	–						8,10
		6	–	80	–	80	–	80	–	80	–	80	–	80								6	–						8
		10	–	160	–	160	–	160	–	160	–	160	–	160								10	–						2,5,8,11,14
		11	–	40	–	40	–	40	–	40	–	40	–	40								11	–						8,10
		14	–	40	–	40	–	40	–	40	–	40	–	40								14	–						8,10
	I_{IHH}	2	1.0	–	1.0	–	1.0	–	1.0	–	1.0	–	1.0	–	mAdc								2					16	8,10
		3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓									3						4,8
		4	–	–	–	–	–	–	–	–	–	–	–	–									4						3,8
		5																					5						8,10
		6																					6						8
		10																					10						2,5,8,11,14
		11																					11						8,10
		14																					14						8,10
Clamp Voltage	V_{IC}	2**	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	2	–	–	–	–	–	16	–	8
Output																													
Output Voltage	V_{OL}	1	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4		0.4	Vdc	1	–	–	–	–	–	–	–	2,3,5,11,14	–	16	–	8
		1	–	0.4	–	0.4		0.4		0.4		0.4		0.4	↓	–	1	–	–	–	–	–	–	2,3,5,11,14	–	16	16	↓
		12	–	0.5	–	0.5		0.5		0.5		0.5		0.5		–	–	12	–	–	–	–	–	3	2,5,11,14	16		
	V_{OH}	1	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	–	–	1	–	–	–	3	2,5,11,14	16		8
Short-Circuit Current	I_{OS}	1	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	–	–	3	2,5,11,14	–	–	–	16	–	–	1,8
		13#	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	mAdc	–	–	–	–	–			–	–	–	16	–	–	8,13
Power Requirements (Total Device)																													
Power Supply Drain	I_{CC}	16	–	–	–	65	–	–	–	–	–	65	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	16	–	–	8

**Test all inputs in the same manner.
#Test applies only to the MC4316/4016 and MC4018.

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



Note 1:
Counter programmed for ÷8 operation.
(For MC4316/4016 and MC4018, pin 13 is the resistor pin, and left open.)



SWITCHING TIME TEST PROCEDURES (T_A = 25°C)

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				OUTPUT		LIMITS		
		Clock Pin 6	Gate Pin 4	D0, D1, D2 Pins 5,11,14	D3, $\overline{PE}$, $\overline{MR}$ Pins 2,3,10	Bus Pin 12	Q3 Pin 1	Min	Max	Unit
Toggle Frequency (Check before measuring propagation delay.)	f_{tog}	T	T	Gnd	2.5 V	–	U	8.0	–	MHz
Propagation Delay Clock to Bus	t_{PLH}	V	V	Gnd	2.5 V	W	–	–	65	ns
Propagation Delay Gate to Q3	t_{PLH}	Y	Y	Gnd	2.5 V	–	Z	–	35	ns
Propagation Delay Clock 1 to Q3 MC4316/4016 MC4018	t_{PHL}	V	V	Gnd	2.5 V	–	X	– –	45 78	ns ns

OPERATING CHARACTERISTICS

MC4316/4016, MC4018

Operation of both counters is essentially the same. The MC4316/4016 has a maximum modulus of ten while the MC4018 is capable of dividing by up to sixteen. Minor differences in the programming procedure will be covered in the discussion of cascaded stages.

Suitable connections for operating a single stage are shown in Figure 1, as well as appropriate waveforms. The desired modulus is applied to the data inputs D0, D1, D2, and D3 in binary (MC4018) or binary coded decimal (MC4016) positive logic format. If a number greater than nine (BCD 1001) is applied to the MC4016, it treats the most significant bit position as a zero; if for example, binary fourteen (1110) were applied to an MC4016, the counter would divide by six. BCD eight is programmed in Figure 1. As $\overline{PE}$ is taken low the states on the parallel inputs are transferred to their respective outputs. Subsequent positive transitions of the input clock will decrement the counter until the all zero state is detected by the bus gate. The resulting positive transition of the bus line is internally inverted and fed back to the preset gating circuitry but does not yet preset the counter since the gateclock input is still high. As the clock returns to the low state the counter is set to the programmed state, taking the bus line low. The net result is one positive pulse on the bus line for every N clock pulses. The output pulse width is approximately equal to one clock pulse high time.

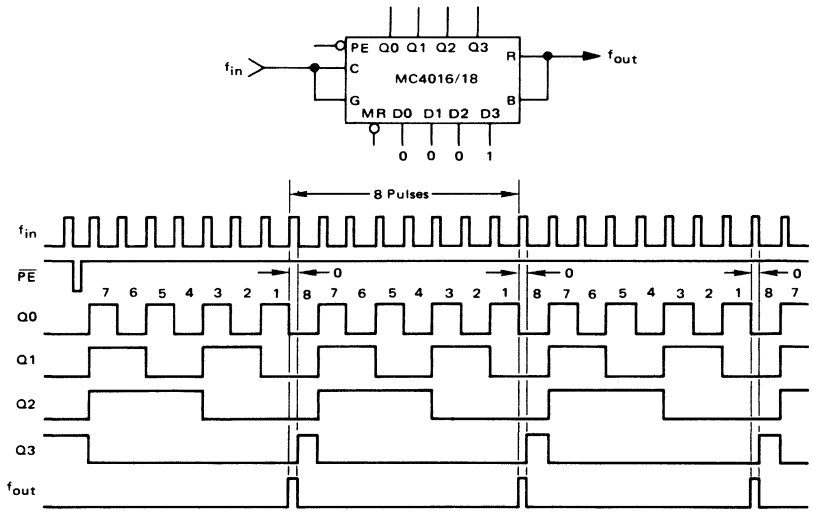
Operation will continue in this fashion until the data on the programmable inputs is changed. Since the preset circuitry is inhibited except when the counter is in the zero state, preset data may be changed while clocking is occurring. If it is necessary to enter a new number before the counter has reached zero this can be done by momentarily taking $\overline{PE}$ low. Countdown will continue from the new number on the next positive clock transition.

The counters can be made to divide by 10 (MC4016) or 16 (MC4018) by inhibiting the preset logic. This may be done by either holding the gate input high or by holding the bus line low.

The normal connections for cascading stages are indicated in Figure 2, with the appropriate waveforms. Note that the gate input of each stage is connected to the clock; all bus outputs are tied to one of the internal pullup resistors, R. The total modulus for cascaded MC4016s is determined from $N_T = N_0 + 10N_1 + 100N_2 + \ldots$; N_T for MC4018s is given by $N_T = N_0 + 16N_1 + 256N_2 + \ldots$ Stated another way, the BCD equivalent of each decimal digit is applied to respective MC4016 stages while the data inputs of the MC4018 stages are treated as part of one long binary number. The difference in programming is illustrated in Figure 2 where $N_T = 245$ is coded for both counter types.

Cascaded operation can be further clarified by referring to the timing diagram of Figure 2. For the MC4016, counting begins with the first positive clock transition after the data has been set in. After the five clock pulses, the least-significant stage has been counted down to zero. The bus line does not go high at this time since the three bus terminals are wire-ORed and the other two stages are not in the zero state. Since no reset occurs, the next positive

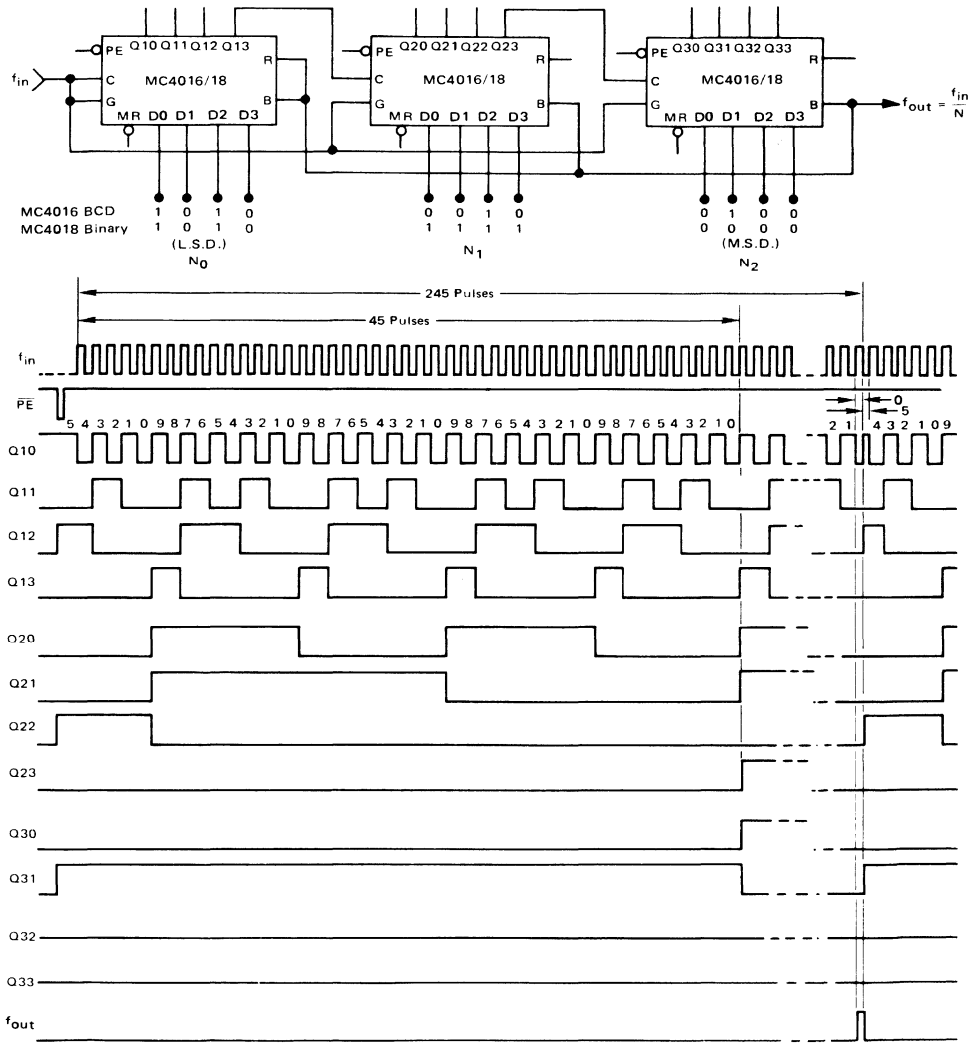
FIGURE 1 — SINGLE-STAGE OPERATION



OPERATING CHARACTERISTICS: MC4316/4016, MC4018

clock edge advances the least significant stage to the nine (1001) state, causing the second stage to be decremented. The process continues in this manner with the least significant stage now dividing by ten. The second stage eventually counts down to zero and also reverts to dividing by ten. Each pulse out of the second stage decrements the third until it reaches zero. At this time the bus line goes high; it remains high until the clock goes low, causing all three stages to be reset to the programmed count again.

FIGURE 2 — CASCADED OPERATION



APPLICATIONS INFORMATION

A typical system application for programmable counters is illustrated in the frequency synthesizer shown in Figure 4. There the counter provides a means of digitally selecting some integral multiple of a stable reference frequency. The circuit phase locks the output, f_{VCO}, of a voltage controlled oscillator to a reference frequency, f_{ref}.[1] Circuit operation is such that $f_{VCO} = Nf_{ref}$, where N is the divider ratio of the feedback counter.

In many synthesizer applications the VCO is operated at VHF frequencies too high for direct division by TTL counters. In these cases the VCO output is usually prescaled by using a suitable fixed divide-by-M ECL circuit as shown in Figure 5. For this configuration, $f_{VCO} = NMf_{ref}$, where N is variable (programmable) and M is fixed. Design of the optimum loop filter requires that the input reference frequency be as high as possible where

FIGURE 4 — MTTL PHASE-LOCKED LOOP

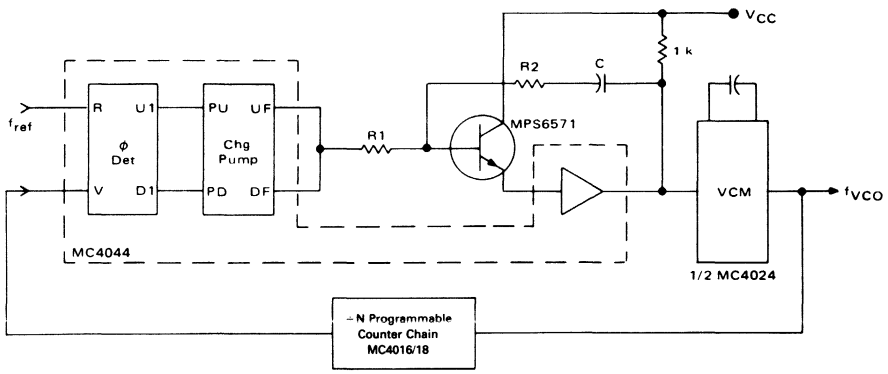
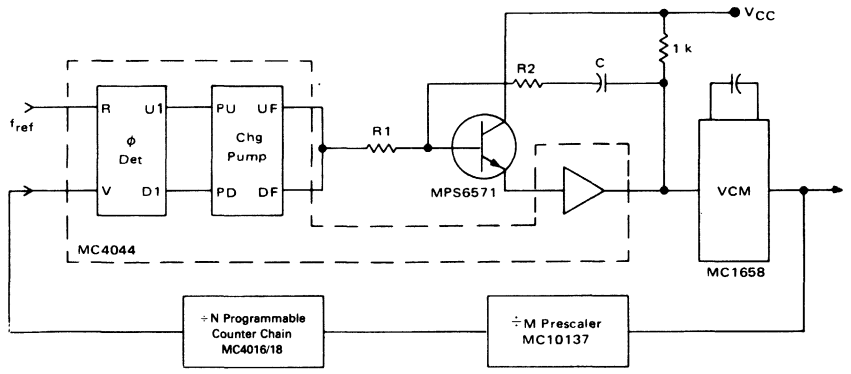


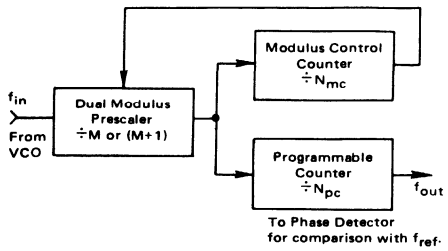
FIGURE 5 — MTTL-MECL PHASE-LOCKED LOOP



1 See Motorola Application Note AN-535 and the MC4344/4044 Data Sheet for detailed explanation of overall circuit operation.

6

FIGURE 6 — FEEDBACK COUNTERS WITH DUAL MODULUS PRESCALER



the upper limit is established by the required channel spacing. Since $f_{VCO} = Nf_{ref}$ in the non-prescaled case, if N is changed by one, the VCO output changes by f_{ref}, or the synthesizer channel spacing is just equal to f_{ref}. When the prescaler is used as in Figure 5, $f_{VCO} = NMf_{ref}$, and a change of one in N results in the VCO changing by Mf_{ref}, i.e., if f_{ref} is set equal to the minimum permissible channel spacing as is desirable, then only every M channels in a given band can be selected. One solution is to set f_{ref} = channel spacing/M but this leads to more stringent loop filter requirements.

An alternate approach that avoids this problem is provided by the counter configuration shown in Figure 6.[2] It too uses a prescaler ahead of a programmable counter, however the modulus of the prescaler is now controlled by a third counter, causing it to alternate between M and M + 1. Operation is best explained by assuming that all three counters have been set for the beginning of a cycle: the prescaler for division by (M + 1), the modulus control counter for division by N_{mc}, and the programmable counter for division by N_{pc}. The prescaler will divide by (M + 1) until the modulus control counter has counted down to zero; at this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle. For this configuration,

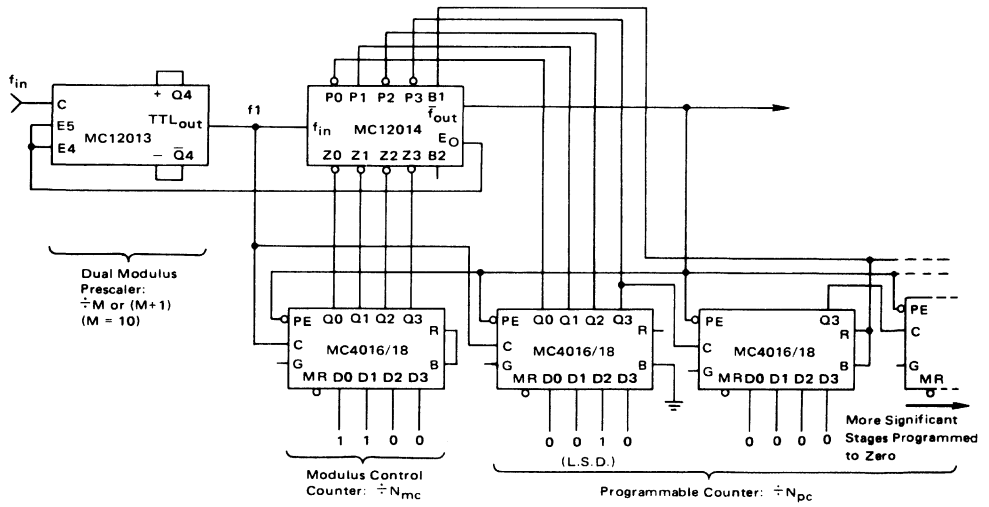
$$f_{out} = \frac{f_{in}}{MN_{pc} + N_{mc}}$$

In terms of the synthesizer application, $f_{VCO} = (MN_{pc} + N_{mc}) f_{ref}$ and channels can be selected every f_{ref} by letting N_{pc} and N_{mc} take on suitable integer values, including zero.

A simplified example of this technique is shown in Figure 7. The MC12013 Dual Modulus Prescaler divides by either 10 or 11 when connected as shown in Figure 7. If the E3 and E4 Enable inputs are high at the start of a prescaler cycle, division by 10 results; if the Enable inputs are low at the beginning of the cycle, division by 11 results. The zero detection circuitry of the MC12014 Counter Control Logic is connected to monitor the outputs of the modulus control counter; this provides a suitable enable signal at E0 as the modulus control counter reaches its terminal (zero) count. The remainder of the MC12014 is connected to extend the operating frequency of the programmable counter chain.

A specific example of this technique is shown in Figure 8. There the feedback divider circuitry required for generating frequencies between 144 MHz and 178 MHz with 30 kHz channel spacing is shown.[2]

FIGURE 7 — FREQUENCY DIVISION: $f_O = f_{in}/MN_{pc} + N_{mc}$



2. This application is discussed in greater detail in the MC12014 Counter Control Logic data sheet.

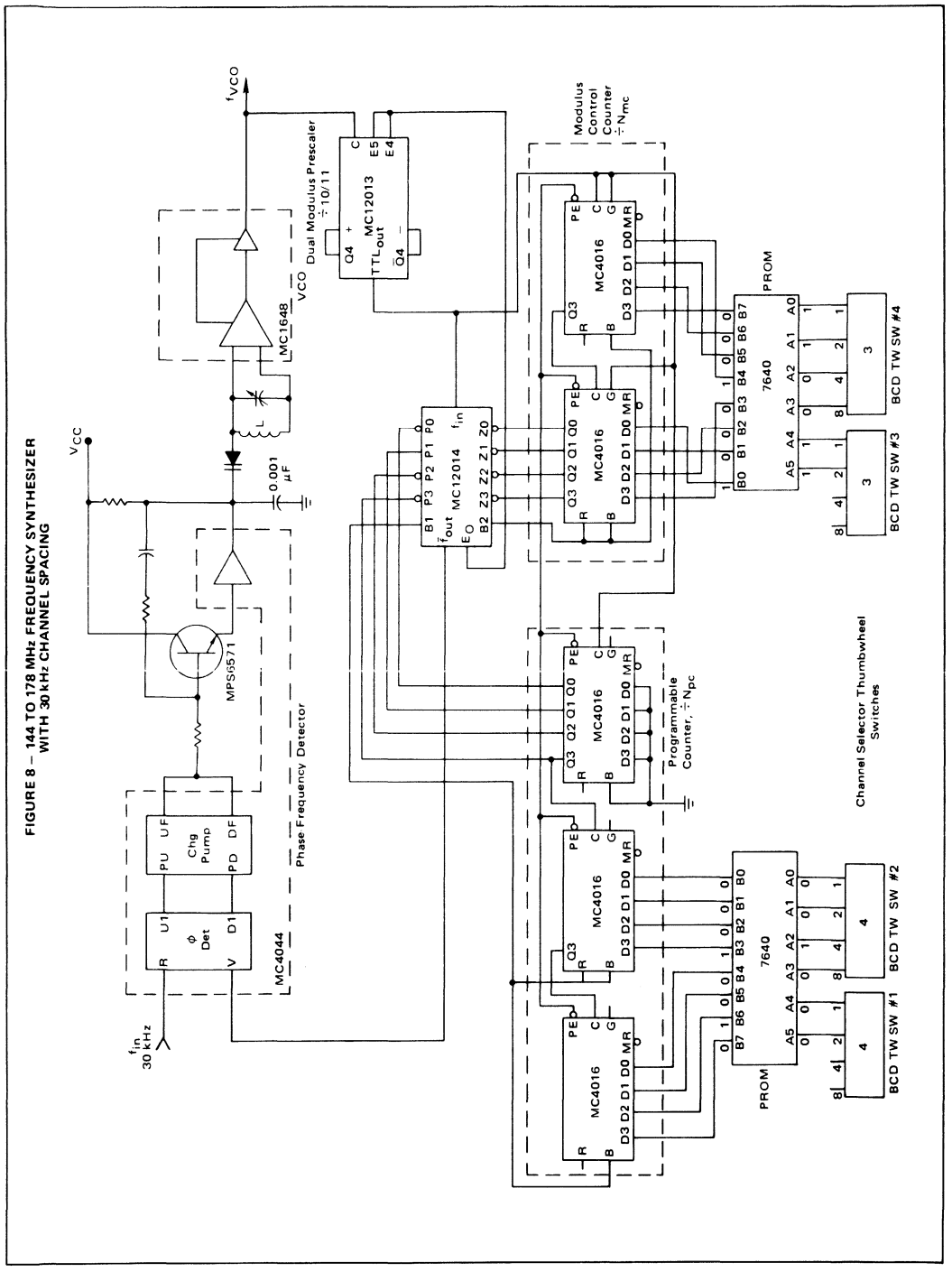


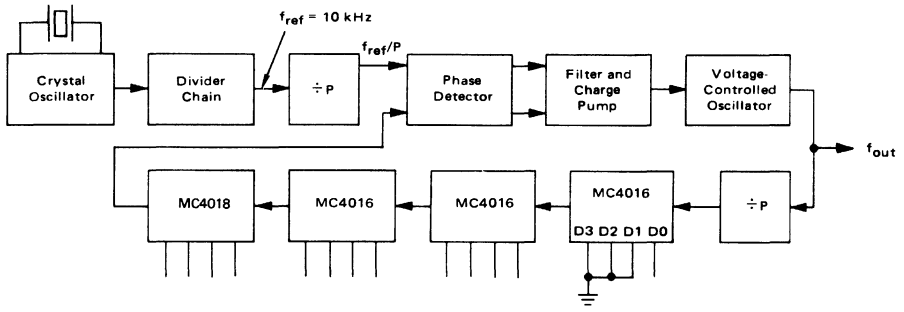
FIGURE 8 – 144 TO 178 MHz FREQUENCY SYNTHESIZER WITH 30 kHz CHANNEL SPACING

Figure 9 shows a frequency synthesizer system for the aircraft band of 108 to 136 MHz with a channel spacing of 50 kHz. For a system of this type it is desirable to use direct-reading thumbwheel switches for channel selection. To implement this system with these constraints, it is necessary to calculate the required reference frequency (f_{ref}). Figure 9 requires a reference frequency of 10 kHz and N4 must be programmed to only 0 and 5.

For any phase-locked loop system it is desirable to maintain as high a reference frequency as possible while meeting the system requirements. The higher the reference frequency, the higher the number of sampling pulses received by the phase detector per unit time. This results in (1) easier filtering of the control voltage, (2) faster lock-up time, and (3) less noise in the output spectrum. The higher reference frequency is also desirable because the reference frequency appears as sidebands on the output frequency and the farther the sidebands are away from the output the better the system. Another advantage of the higher reference frequency is the smaller divide ratio required in the programmable counter chain. This is advantageous when calculating realizable resistors for the filter.

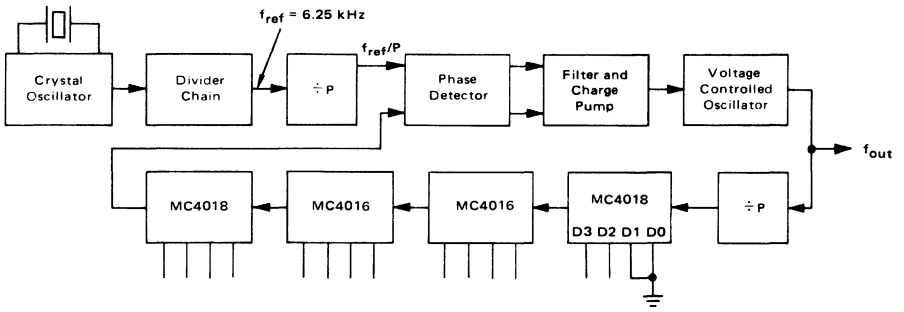
Figure 10 shows the implementation of the aircraft band synthesizer with 25 kHz channel spacing (the 25 kHz spacing has been proposed to the FCC). Figure 10 shows the system using an MC4018 as the first counter, and has a reference frequency of 6.25 kHz to obtain the direct programming.

FIGURE 9 — 108 TO 136 MHz FREQUENCY SYNTHESIZER WITH 50 kHz CHANNEL SPACING



$N = 1000N_1 + 100N_2 + 10N_3 + N_4$

FIGURE 10 — 108 TO 136 MHz FREQUENCY SYNTHESIZER WITH 25 kHz CHANNEL SPACING



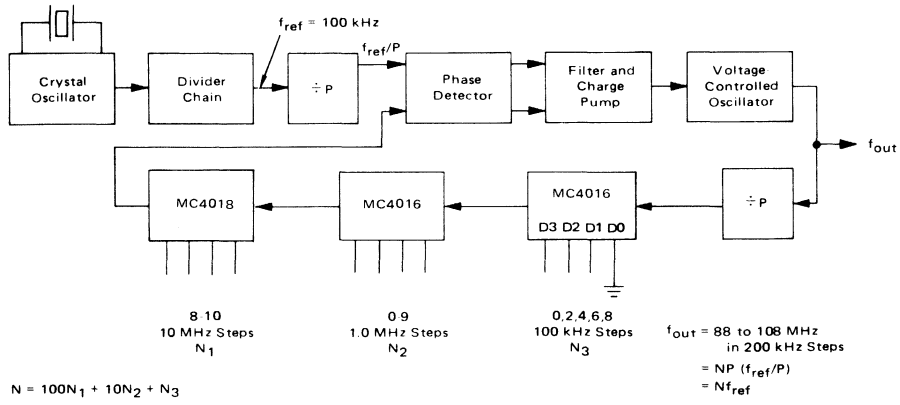
$N = 1600N_1 + 160N_2 + 16N_3 + N_4$

6

Figure 11 shows the FM band implemented with the MC4016 and has a 100 kHz reference frequency.

The MC4316/4016 covers phase-locked loop applications where the channel spacing is 1 x 10^n Hz. The MC4018 is used when the most significant digit is between 9 and 15.

FIGURE 11 — 88 TO 108 MHz FREQUENCY SYNTHESIZER WITH 200 kHz CHANNEL SPACING



6

MOTOROLA

MC4324
MC4024

DUAL VOLTAGE-CONTROLLED MULTIVIBRATOR

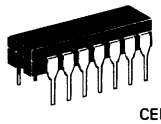
The MC4324/4024 consists of two independent voltage-controlled miltivibrators with output buffers. Variation of the output frequency over a 3.5-to-1 range is guaranteed with an input dc control voltage of 1.0 to 5.0 voltage.

Operating frequency is specified at 25 MHz at 25°C. Operation to 15 MHz is possible over the specified temperature range. For higher frequency requirements, see the MC1648 (200 MHz) or the MC1658 (125 MHz) data sheet.

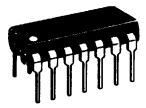
This device was designed specifically for use in phase-locked loops for digital frequency control. It can also be used in other applications requiring a voltage-controlled frequency, or as a stable fixed frequency oscillator (3.0 MHz to 15 MHz) by replacing the external control capacitor with a series mode crystal.

Maximum Operating Frequency = 25 MHz Guaranteed @ 25°C
Power Dissipation = 150 mW typ/pkg
Output Loading Factor = 7

DUAL VOLTAGE-CONTROLLED MULTIVIBRATOR



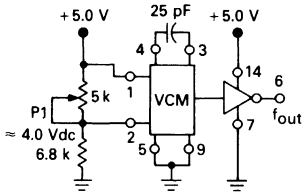
L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC4024 only)

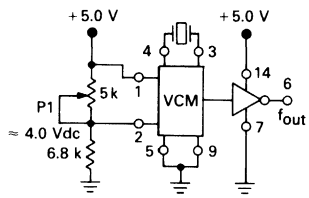
TYPICAL APPLICATIONS

FIGURE 1 — ASTABLE MULTIVIBRATOR



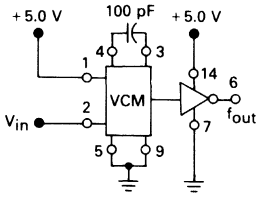
f_{out} = 10 MHz

FIGURE 2 — CRYSTAL CONTROLLED MULTIVIBRATOR



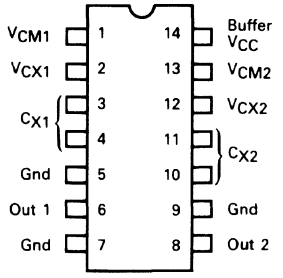
Crystal frequency can be pulled slightly by adjusting P1.

FIGURE 3 — VOLTAGE-CONTROLLED MULTIVIBRATOR



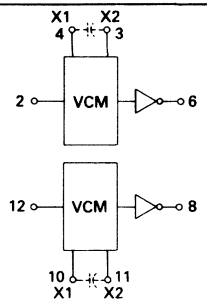
V_{in} = 2.5 V to 5.5 V
f_{out} = 1.0 MHz min, 5.0 MHz max

PIN ASSIGNMENT



6

ELECTRICAL CHARACTERISTICS

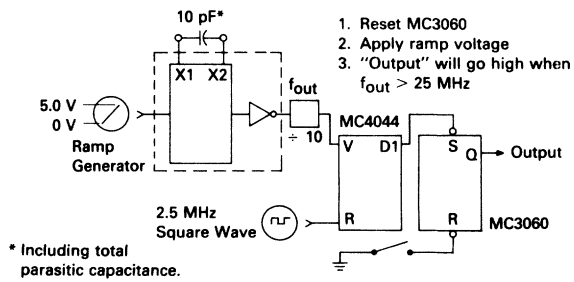


V_{CC}: VCM = 1, 13
Output Buffer = 14
Gnd: VCM = 5, 9
Output Buffer = 7
External Capacitor for
Frequency Range Determination

Test Temperature		TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OH}	Volts V_{IH}	V_{CC}	V_{CCL}	V_{CCH}
MC4324	−55°C	9.8	11.2	−1.6	5.0	5.0	4.5	5.5
	+25°C	9.8	11.2	−1.6	5.0	5.0	4.5	5.5
	+125°C	9.8	11.2	−1.6	5.0	5.0	4.5	5.5
MC4024	0°C	9.8	11.2	−1.6	5.0	5.0	4.75	5.25
	+25°C	9.8	11.2	−1.6	5.0	5.0	4.75	5.25
	+75°C	9.8	11.2	−1.6	5.0	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4324 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4024 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	V_{IH}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																							
Forward Current	I_{in}	2	—	100	—	100	—	100	—	100	—	100	—	100	μAdc	—	—	—	2	—	—	14	5,7,9
		12	—	100	—	100	—	100	—	100	—	100	—	100	μAdc	—	—	—	12	—	—	14	5,7,9
Output																							
Output Voltage	V_{OL}	6	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	Vdc	6	—	—	2	—	1,4,14	—	5,7,9
		8	—	↓	—	↓	—	↓	—	↓	—	↓	—	↓	↓	8	—	—	12	—	10,13,14	—	↓
		6	—	↓	—	↓	—	↓	—	↓	—	↓	—	↓	↓	—	6	—	2	—	—	1,4,14	↓
		8	—	↓	—	↓	—	↓	—	↓	—	↓	—	↓	↓	—	8	—	12	—	—	10,13,14	↓
	V_{OH}	6	2.4	—	2.4	—	2.4	—	2.5	—	2.5	—	2.5	—	Vdc	—	—	6	2	—	1,3,14	—	5,7,9
		8	2.4	—	2.4	—	2.4	—	2.5	—	2.5	—	2.5	—	Vdc	—	—	8	12	—	11,13,14	—	5,7,9
Short-Circuit Current	I_{OS}	6	−20	−65	−20	−65	−20	−65	−20	−65	−20	−65	−20	−65	mAdc	—	—	—	2	1,3,14	—	—	5,6,7,9
		8	−20	−65	−20	−65	−20	−65	−20	−65	−20	−65	−20	−65	mAdc	—	—	—	12	11,13,14	—	—	5,7,8,9
Power Requirements (Total Device)																							
Power Supply Drain	I_{CC}	1,3,14	—	—	—	37	—	—	—	—	—	37	—	—	mAdc	—	—	—	2,4,10,12	1,13,14	—	—	5,7,9

FIGURE 4 — AC TEST CIRCUIT AND WAVEFORMS



1. Reset MC3060
2. Apply ramp voltage
3. "Output" will go high when $f_{out} > 25$ MHz

* Including total parasitic capacitance.

(V_{CC} = 5.0 Vdc, T_A = 25°C)

TEST	SYMBOL	CONDITIONS	VALUE Min	VALUE Typ
Maximum Operating Frequency	F_{max}	C_X = 10 pF, V_{in} = 5.0 Vdc Frequency Ratio = 3.5:1	25 MHz	30 MHz
Ratio of Frequency of Oscillation Over Specified Input Voltage Range	$\frac{F_{high}}{F_{low}}$	C_X = 100 pF, V_{in} high = 5.0 Vdc, V_{in} low = 1.0 Vdc	3.5:1.0	4.5:1.0

FIGURE 5 — FREQUENCY-CAPACITANCE PRODUCT

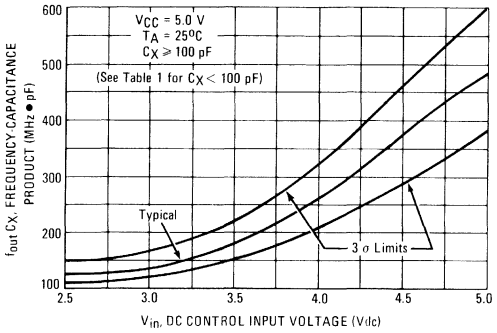


FIGURE 6 — FREQUENCY-VOLTAGE GAIN CHARACTERISTICS

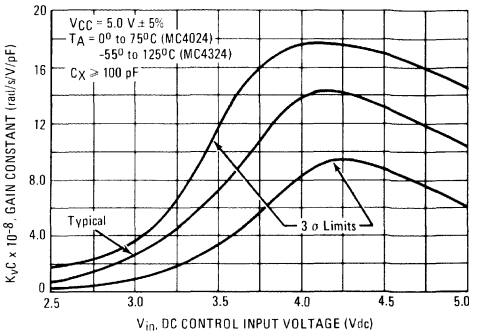


FIGURE 7 — TYPICAL FREQUENCY DEVIATION versus SUPPLY VOLTAGE

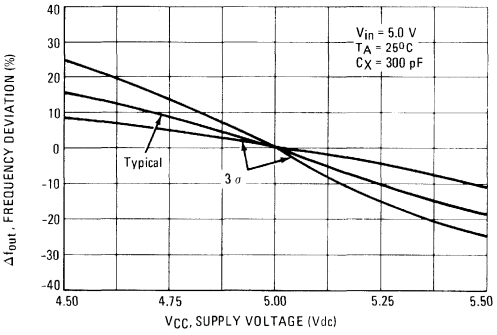


FIGURE 8 — TYPICAL FREQUENCY DEVIATION versus SUPPLY VOLTAGE

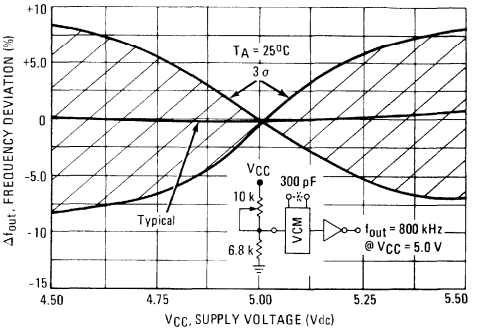


FIGURE 9 — FREQUENCY DEVIATION versus AMBIENT TEMPERATURE

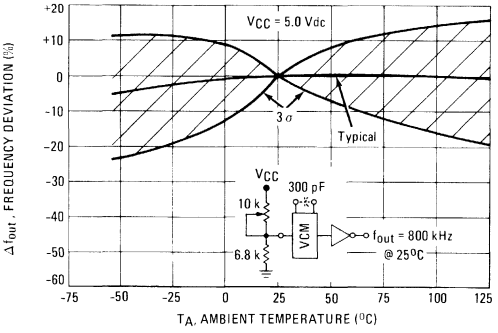
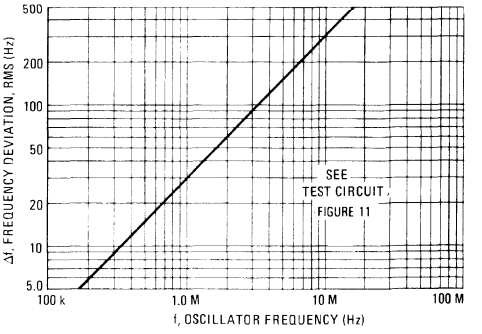
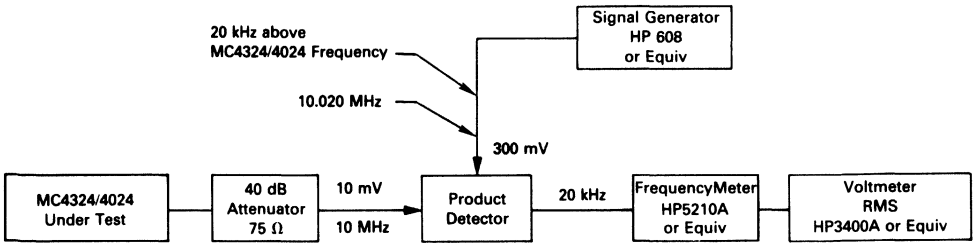


FIGURE 10 — RMS NOISE DEVIATION versus OSCILLATOR FREQUENCY



NOTE: Curves labeled as 3 σ limits denote that 99.7% of the devices tested fell within these limits.

FIGURE 11 — NOISE DEVIATION TEST CIRCUIT



$$\text{Frequency Deviation} = \frac{\text{(HP5210A output voltage) (Full Scale Frequency)}}{\text{1.0 Volt}}$$

NOTE: Frequency deviation values of either the signal generator or power supply should be determined prior to testing.

APPLICATIONS INFORMATION

Suggested Design Practices

Three power supply and three ground connections are provided in this circuit (each multivibrator has separate power supply and ground connections, and the output buffers have common power supply and ground pins). This provides isolation between VCM's and minimizes the effect of output buffer transients on the multivibrators in critical applications. The separation of power supply and ground lines also provides the capability of disabling one VCM by disconnecting its V_{CC} pin. However, all ground lines must always be connected to insure substrate grounding and proper isolation.

General design rules are:

1. Ground pins 5, 7, and 9 for all applications, including those where only one VCM is used.
2. Use capacitors with less than 50 nA leakage at plus and minus 3.0 volts. Capacitance values of 15 pF or greater are acceptable.
3. When operated in the free running mode, the minimum voltage applied to the DC Control input should be 60% of V_{CC} for good stability. The maximum voltage at this input should be V_{CC} + 0.5 volt.
4. When used in a phase-locked loop, the filter design should have a minimum DC Control input voltage of 1.0 volt and a maximum voltage of V_{CC} + 0.5 volt. The maximum restriction may be waived if the output impedance of the driving device is such that it will not source more than 10 mA at a voltage of V_{CC} + 0.5 volt.
5. The power supply for this device should be bypassed with a good quality RF-type capacitor of 500 to 1000 pF. Bypass capacitor lead lengths should be kept as short as possible. For best results, power supply voltage should be maintained as close to +5.0 V as possible. Under no conditions should the design require operation with a power supply voltage outside the range of 5.0 volts ± 10%.

External Control Capacitor (C_X) Determination (See Table 1)

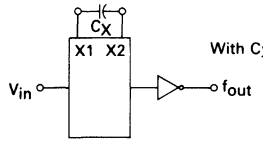
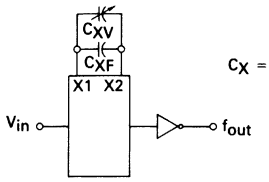
The operating frequency range of this multivibrator is controlled by the value of an external capacitor that is connected between X1 and X2. A tuning ratio of 3.5-to-1 and a maximum frequency of 25 MHz are guaranteed under ideal conditions (V_{CC} = 5.0 volts. T_A = 25°C). Under actual operating conditions, variations in supply voltage, ambient temperature, and internal component tolerances limit the tuning ratio (see Figures 7 thru 12). An improvement in tuning ratio can be achieved by providing a variable tuning capacitor to facilitate initial alignment of the circuit.

Figures 5 through 9 show typical and suggested design limit information for important VCM characteristics. The suggested design limits are based on operation over the specified temperature range with a supply voltage of 5.0 volts ± 5% unless otherwise noted. They include a safety factor of three times the estimated standard deviation.

Figures 5 and 6 provide data for any external control capacitor value greater than 100 pF. With smaller capacitor values, the curves are effectively moved downward. For example, a typical curve of frequency versus control voltage would be very nearly identical to the lower suggested design limit of Figure 5 if a 15 pF capacitor is used. To use Figure 5 divide on the ordinate by the capacitor

6

TABLE 1 — EXTERNAL CONTROL CAPACITOR VALUE DETERMINATION

CONFIGURATION	T_A	V_{CC}	VALUES OF K				
			K1	K2	K3	K4	K5
 With $C_X = \frac{K1}{f_{OH}} - 5$, $f_{OL} \leq \frac{K2}{C_X}$	25°C ±3°C	5.0 V	385	150	600	110	1.0
		5.0 V ±5%	325	175	680	125	1.14
		5.0 V ±10%	290	190	750	140	1.25
 $C_X = C_{XV} + C_{XF}$	0°C to 75°C	5.0 V	335	165	660	120	1.10
		5.0 V ±5%	280	190	750	140	1.25
		5.0 V ±10%	250	200	840	150	1.40
Choose C_{XF} and C_{XV} such that C_X can be adjusted to: $\frac{K1}{f_{OH}} - 5 \leq C_X \leq \frac{K3}{f_{OH}} - 5$ With $V_{in} = V_{CC} = 5.0$ V, adjust C_X to obtain: $f_{out} = K5\ (f_{OH})$ Then: $f_{OL} \leq \frac{K4}{K1} f_{OH}$	−55°C to 125°C	5.0 V	300	175	690	125	1.15
		5.0 V ±5%	260	200	780	145	1.30
		5.0 V ±10%	230	210	860	155	1.45

Definitions: f_{OH} = Output frequency with $V_{in} = V_{CC}$
f_{OL} = Output frequency with $V_{in} = 2.5$ V
(Frequencies in MHz, C_X in pF)

value in picofarads to obtain output frequency in megahertz. In Figure 6 the ordinate axis is multiplied by the capacitor value in picofarads to obtain the gain constant (K_V) in radians/second/volt.

Frequency Stability

When the MC4324/4024 is used as a fixed-frequency oscillator (V_{in} constant), the output frequency wll vary slightly because of internal noise. This variation is indicated by Figure 10 for the circuit of Figure 11. These variations are relatively independent (< 10%) of changes in temperature and supply voltage.

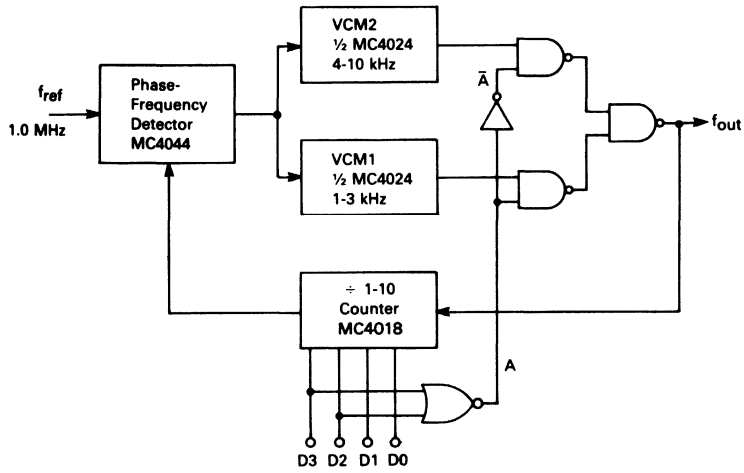
10-to-1 Frequency Synthesizer

A frequency synthesizer covering a 10-to-1 range is shown in Figure 14.Three packages are required to complete the loop: The MC4344/4044 phase-frequency detector, the MC4324/4024 dual voltage-controlled multivibrator, and the MC4318/4018 programmable counter. Two VCM's (one package) are used to obtain the required frequency range. Each VCM is capable of operating over a 3-to-1 range, thus VCM1 is used for the lower portion of the times ten range and VCM2 covers the upper end. The proper divide ratio is set into the programmable counter and the VCM for that frequency is selected by control gates. The other VCM is left to be free running since its output is gated out of the feedback path.

Normally with a single VCM the loop gain would vary over a 10-to-1 range due to the range of the counter ratios. This affects the bandwidth, lockup time, and damping ratio severely. Utilizing two VCM's reduces this change in loop gain rom 10-to-1 to 3-to-1 as a result of the different sensitivities of the two VCM's due to the different frequency ranges. This change of VCM sensitivity (3-to-1) is of such a direction of compensate for loop gain variations due to the programmable counter.

The overall concept of multi-VCM operation can be expanded for ranges greater than 10-to-1. Four VCM's (two packages) could be used to cover a 100-to-1 range.

FIGURE 12 — 10-TO-1 FREQUENCY SYNTHESIZER



÷N	Input D3	D2	D1	D0	A	VCM1 kHz	VCM2 kHz	f_{out} kHz
1	0	0	0	1	1	1	X	1
2	0	0	1	0	1	2	X	2
3	0	0	1	1	1	3	X	3
4	0	1	0	0	0	X	4	4
5	0	1	0	1	0	X	5	5
6	0	1	1	0	0	X	6	6
7	0	1	1	1	0	X	7	7
8	1	0	0	0	0	X	8	8
9	1	0	0	1	0	X	9	9
10	1	0	1	0	0	X	10	10

MOTOROLA

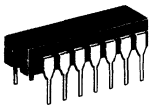
MC4344
MC4044

PHASE-FREQUENCY DETECTOR

The MC4344/4044 consists of two digital phase detectors, a charge pump, and an amplifier. In combination with a voltage controlled multivibrator (such as the MC4324/4024 or MC1648), it is useful in a broad range of phase-locked loop applications. The circuit accepts TTL waveforms at the R and V inputs and generates an error voltage that is proportional to the frequency and/or phase difference of the input signals. Phase detector #1 is intended for use in systems requiring zero frequency and phase difference at lock. Phase detector #2 is used if quadrature lock is desired. Phase detector #2 can also be used to indicate that the main loop, utilizing phase detector #1, is out of lock.

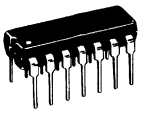
Operating Frequency = 8 MHz typ
Input Loading Factor: R, V = 3
Output Loading Factor (Pin 8) = 10
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time = 9.0 ns typ
(thru phase detector)

PHASE-FREQUENCY DETECTOR

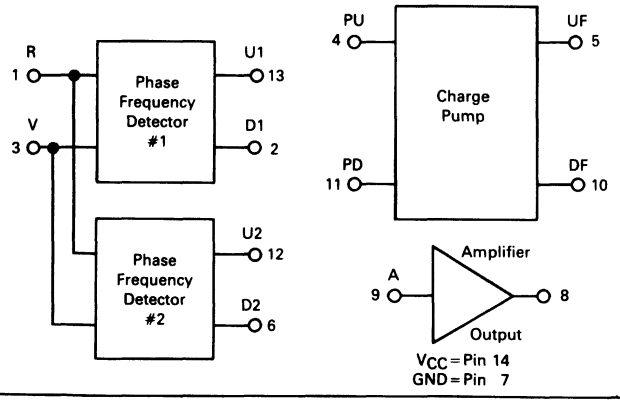


L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

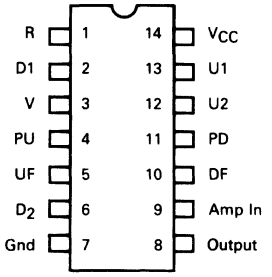
P SUFFIX
PLASTIC PACKAGE
CASE 646
MC4044 only



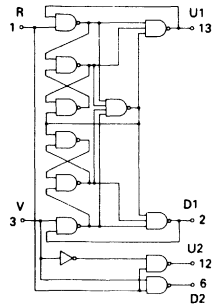
LOGIC DIAGRAM



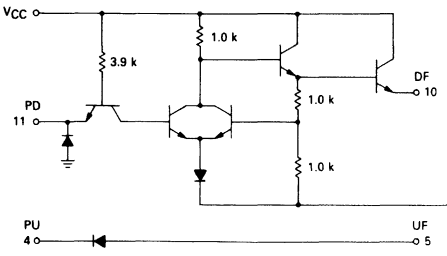
PIN ASSIGNMENT



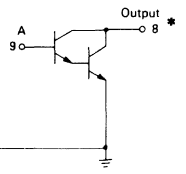
PHASE DETECTOR



CHARGE PUMP



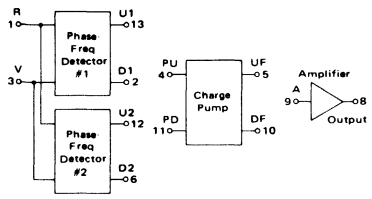
AMPLIFIER



*V_{MAX} not to exceed 8.0 Vdc.

6

ELECTRICAL CHARACTERISTICS



INPUT STATE	INPUT R	INPUT V	OUTPUT U1	OUTPUT D1	OUTPUT U2	OUTPUT D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	0	1	1	1
8	1	0	0	1	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not show all possible modes of operation. It is useful for dc testing.

1. X indicates output state unknown.
2. U1 and D1 outputs are sequential; i.e., they must be sequenced in order shown.
3. U2 and D2 outputs are combinational; i.e., they need only inputs shown to obtain outputs.

Characteristic	Symbol	Pin Under Test	MC4344 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4044 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW I_{OL}	I_{OH1}	I_{OH2}	I_{in}	I_{IC}	I_A	V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{out}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																															
Forward Current	I_{IL}	1	-	-4.8	-	-4.8	-	-4.8	-	-4.8	-	-4.8	-	-4.8	mAdc							1								14	7
		3		-4.8		-4.8		-4.8		-4.8		-4.8		-4.8	↓						-	3	-	-						↓	↓
		11		-1.6		-1.6		-1.6		-1.6		-1.6		-1.6								11									
Leakage Current	I_{IH}	1	-	120	-	120	-	120	-	120	-	120	-	120	μAdc								1	-						14	7
		3		120		120		120		120		120		120									3	-						14	7
		4		5.0		5.0		5.0		5.0		5.0		5.0									-							4	5,7
		11		40		40		40		40		40		40	↓								11	-						14	7
	I_{IHH}	1	-	-	-	1.0	-	-	-	-	-	1.0	-	-	mAdc									1						14	7
		3				↓						↓			↓									3						↓	↓
		11																						11							
Clamp Voltage	V_{IC}	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc					1				-						14	7
		3				-1.5						-1.5			Vdc					3				-						14	7
Output (Note 1)																															
Output Voltage	V_{OH}	6	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		6								1.3				14		7
		12	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		12								1.3				14		7
		••																							3	1			14		7
	V_{OL}	6		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	6										1.3			14		7
	V_{OH}	12	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		12									1.3			14		7
		••													Vdc										3	1			14		7
		••													Vdc										1.3				14		7
	V_{OH}	6	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		6								3	1			14		7
	V_{OL}	12		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	12									3	1			14		7
		••																							1.3				14		7
		••																							3	1			14		7
	V_{OH}	2	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		2								1.3				14		7
	V_{OL}	13		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	13									1.3				14		7
	V_{OH}	2	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		2								1	3			14		7
	V_{OL}	13		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	13									1	3			14		7
	V_{OH}	2	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		2								1.3				14		7
		13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		13								1.3				14		7
	V_{OH}	2	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		2								1	3			14		7
		13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		13								1	3			14		7
	V_{OL}	2		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	2									1.3				14		7
	V_{OH}	13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		13								1.3				14		7
	V_{OL}	2		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	2									1	3			14		7
	V_{OH}	13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		13								1	3			14		7
	V_{OL}	2		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	2									1.3				14		7
	V_{OH}	13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		13								1.3				14		7
	V_{OL}	2		0.4		0.4		0.4		0.4		0.4		0.4	Vdc	2									3	1			14		7
	V_{OH}	13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		13								3	1			14		7
	V_{OH}	2	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		2								1.3				14		7
		13	2.4		2.4		2.4		2.5		2.5		2.5		Vdc		13								1.3				14		7
Short Circuit Current (Note 1)	I_{OS}	*2	-20	*-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc													14			2,3,7,11
		6		↓		↓		↓		↓		↓		↓	↓													↓			1,3,6,7
		12																										↓			1,3,7,12
		*13																													1,3,7,13
Leakage Current (Note 1)	I_{OLK}	*2		250		250		250		250		250		250	μAdc													2,14			1,3,7
		6		↓		↓		↓		↓		↓		↓	↓													6,14			1,3,7
		12																										12,14			1,3,7
		*13																										13,14			1,3,7
Diode Voltage	V_F	5			0.5						0.5				Vdc				5												4,7
Output Voltage	V_{EH}	10	1.5		1.5		1.5		1.5		1.5		1.5		Vdc			10							11				14		7
Output Current	I_O	8	0.2		0.8		1.0		0.5		0.8		1.0		mAdc					9										8	7
Leakage Current	I_{OLK}	8		120		120		120		120		120		120	μAdc															8	7,9
		10		5.0		5.0		5.0		5.0		5.0		5.0	μAdc							11				10				14	7
Power Requirements (Total Device)																															
Power Supply Drain	I_{CC}	14		40		40		40		40		40		40	mAdc													14			7

Test Temperature		I_{OL}	I_{OH1}	I_{OH2}	I_{in}	I_{IC}	I_A	V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{out}	V_{CC}	V_{CCL}	V_{CCH}
		mA						Volts								
MC4344	-55°C	20	-1.6	-1.0			0.002	0.4	2.4		1.1	2.0	1.5	5.0	4.5	5.5
	+25°C	20	-1.6	-1.0	1.0	-1.0	0.002	0.4	2.4	5.5	1.1	1.8	1.5	5.0	4.5	5.5
	+125°C	20	-1.6	-1.0			0.002	0.4	2.4		0.9	1.8	1.5	5.0	4.5	5.5
MC4044	0°C	20	-1.6	-1.0			0.002	0.4	2.5		1.1	2.0	1.5	5.0	4.75	5.25
	+25°C	20	-1.6	-1.0	1.0	-1.0	0.002	0.4	2.5	5.5	1.1	1.8	1.5	5.0	4.75	5.25
	+75°C	20	-1.6	-1.0			0.002	0.4	2.5		0.9	1.8	1.5	5.0	4.75	5.25

Note 1. The output state of Pin 2 or Pin 13 depends upon the sequence that has been applied to the R and V inputs as shown in the Truth Table. In testing output voltage, the outputs of the device are tested by sequencing through the indicated input states according to the Truth Table. Procedures identified by a double asterisk (**) are necessary to change the state of the sequential logic. When testing I_{OS} and I_{OLK} on Pins 2 or 13, a single asterisk (*) indicates that the R and V inputs are sequenced per the Truth Table to input state 11 where the tests are performed. All input, power supply, and ground voltages must be maintained while sequencing and testing unless otherwise noted.

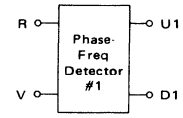
6

APPLICATION

Operation of the MC4344/4044 is best explained by initially considering each section separately. If phase detector #1 is used, loop lockup occurs when both outputs U1 and D1 remain high. This occurs only when all the negative transitions on R, the reference input, and V, the variable or feedback input, coincide. The circuit responds only to transitions, hence phase error is independent of input waveform duty cycle or amplitude variation. Phase detector #1 consists of sequential logic circuitry, therefore operation prior to lockup is determined by initial conditions.

When operation is initiated, by either applying power to the circuit or active input signals to R and V, the circuitry can be in one of several states. Given any particular starting conditions, the flow table of Figure 1 can be used to determine subsequent operation. The flow table indicates the status of U1 and D1 as the R and V inputs are varied. The numbers in the table which are in parentheses are arbitrarily assigned labels that correspond to stable states that can result for each input combination. The numbers without parentheses refer to unstable conditions. Input changes are traced by horizontal movement in the table; after each input change, circuit operation will settle in the numbered state indicated by moving horizontally to the appropriate R-V column. If the number at that location is not in parentheses, move vertically to the number of the same value that is in parentheses. For a given input pair, any one of three stable states can exist. As an example, if R = 1 and V = 0, the circuit will be in one of the stable states (4), (8), or (12).

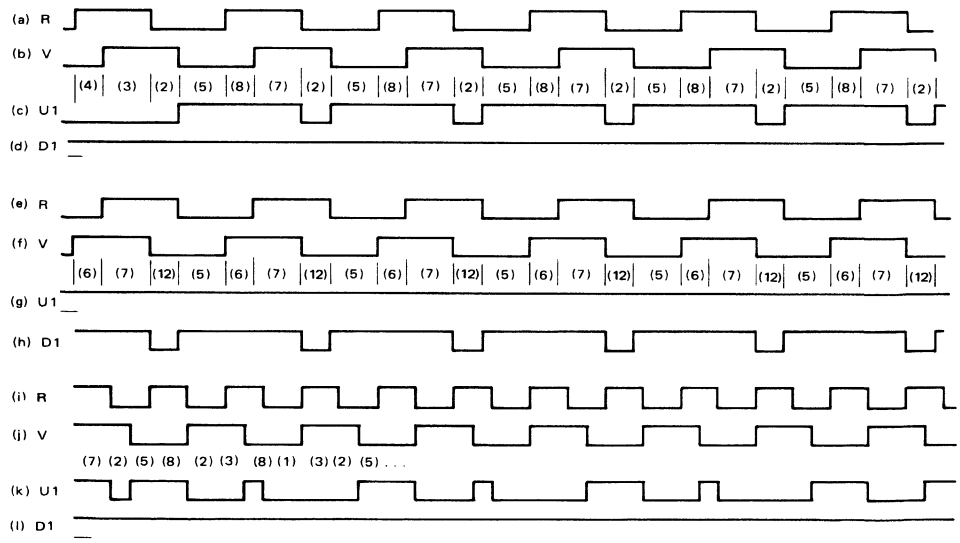
FIGURE 1 — PHASE DETECTOR #1 FLOW TABLE



R-V	R-V	R-V	R-V	U1	D1
0-0	0-1	1-1	1-0		
(1)	2	3	(4)	0	1
5	(2)	(3)	8	0	1
(5)	6	7	8	1	1
9	(6)	7	12	1	1
5	2	(7)	12	1	1
5	2	7	(8)	1	1
(9)	(10)	11	12	1	0
5	6	(11)	(12)	1	0

Use of the table in determining circuit operation is illustrated in Figure 2. In the timing diagram, the input to R is the reference frequency; the input to V is the same frequency but lags in phase. Stable state (4) is arbitrarily assumed as the initial condition. From the timing diagram and flow table, when the circuit is in stable state (4), outputs U1 and D1 are "0" an "1" respectively. The next input state is R-V = 1-1; moving horizontally from stable state (4) under R-V = 1-0 to the R-V = 1-1 column, state 3 is indicated. However, this is an unstable condition and the circuit will assume the state indicated by moving vertically in the R-V = 1-1 column to stable state (3). In this

FIGURE 2 — PHASE DETECTOR #1 TIMING DIAGRAM



6

instance, outputs U1 and D1 remain unchanged. The input states next become R-V = 0-1; moving horizontally to the R-V = 0-1 column, stable state (2) is indicated. At this point there is still no change in U1 or D1. The next input change shifts operation to the R-V = 0-0 column where unstable state 5 is indicated. Moving vertically to stable state (5), the outputs now change state to U1-D1 = 1-1. The next input change, R-V = 1-0, drives the circuitry to stable state (8), with no change in U1 or D1. The next input, R-V = 1-1, leads to stable state (7) with no change in the outputs. The next two input state changes cause U1 to go low between the negative transitions of R and V. As the inputs continue to change, the circuitry moves repeatedly through stable states (2), (5), (8), (7), (2), etc., as shown, and a periodic waveform is obtained on the U1 terminal while D1 remains high.

A similar result is obtained if V is leading with respect to R, except that the periodic waveform now appears on D1 as shown in rows e–h of the timing diagram of Figure 2. In each case, the average value of the resulting waveform is proportional to the phase difference between the two inputs. In a closed loop application, the error signal for controlling the VCO is derived by translating and filtering these waveforms.

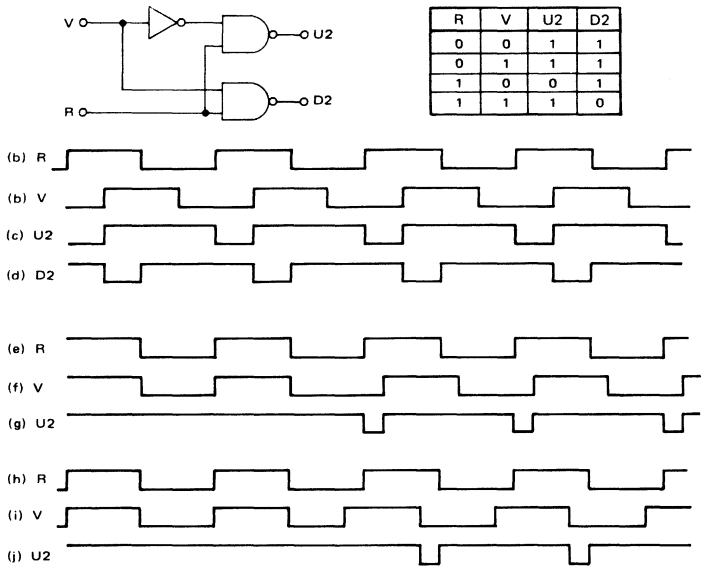
The results obtained when R and V are separated by a fixed frequency difference are indicated in rows i–l of the timing system. For this case, the U1 output goes low when R goes low and stays in that state until a negative transition on V occurs. The resulting waveform is similar to the fixed phase difference case, but now the duty cycle of the U1 waveform varies at a rate proportional to the difference frequency of the two inputs, R and V. It is this characteristic that permits the MC4344/4044 to be used as a frequency discriminator; if the signal on R has been frequency modulated and if the loop bandwidth is selected to pass the deviation frequency but reject R and V, the resulting error voltage applied to the VCO will be the recovered modulation signal.

Phase detector #2 consists only of combinatorial logic, therefore its characteristics can be determined from the simple truth table of Figure 3. Since circuit operation requires that both inputs to the charge pump either be high or have the same duty cycle when lock occurs, using this phase detector leads to a quadrature relationship between R and V. This is illustrated in rows a–d of the timing diagram of Figure 3. Note that any deviation from a fifty percent duty cycle on the inputs would appear as phase error.

Waveforms showing the operation of phase detector #2 when phase detector #1 is being used in a closed loop are indicated in rows e–j. When the main loop is locked, U2 remains high. If the loop drifts out of lock in either direction a negative pulse whose width is proportional to the amount of drift appears on U2. This can be used to generate a simple loss-of-lock indicator.

Operation of the charge pump is best explained by considering it in conjunction with the Darlington amplifier included in the package (see Figure 4). There will be

FIGURE 3 — PHASE DETECTOR #2 OPERATION



R	V	U2	D2
0	0	1	1
0	1	1	1
1	0	0	1
1	1	1	0

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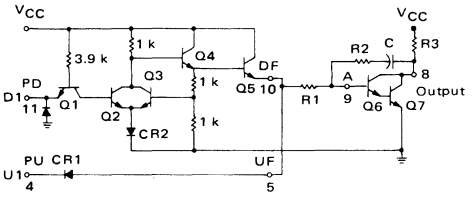
a pulsed waveform on either PD or PU, depending on the phase-frequency relationship of R and V. The charge pump serves to invert one of the input waveforms (D1) and translates the voltage levels before they are applied to the loop filter. When PD is low and PU is high, Q1 will be conducting in the normal direction and Q2 will be off. Current will be flowing through Q3 and CR2; the base of Q3 will be two V_{BE} drops above ground or approximately 1.5 volts. Since both of the resistors connected to the base of Q3 are equal, the emitter of Q4 (base of Q5) will be approximately 3.0 volts. For this condition, the emitter of Q5 (DF) will be on V_{BE} below this voltage, or about 2.25 volts. The PU input to the charge pump is high (> 2.4 volts) and CR1 will be reverse biased. Therefore Q5 will be supplying current to Q6. This will tend to lower the voltage at the collector of Q7, resulting in an error signal that lowers the VCO frequency as required by a "pump down" signal.

FIGURE 4 — CHARGE PUMP OPERATION

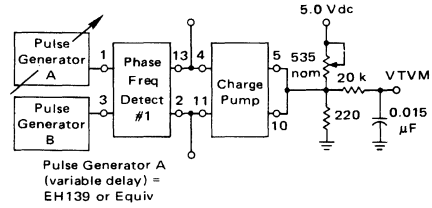


When PU is low and PD is high, CR1 is forward biased and UF will be approximately one V_{BE} above ground (neglecting the $V_{CE(sat)}$ of the driving gate). With PD high, Q1 conducts in the reverse direction, supplying base current for Q2. While Q2 is conducting, Q4 is prevented from supplying base drive to Q5; with Q5 cut off and UF low there is no base current for Q6 and the voltage at the collector of Q7 moves up, resulting in an increase in the VCO operating frequency as required by a "pump up" signal.

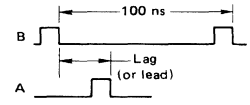
If both inputs to the charge pump are high (zero phase difference), both CR1 and the base-emitter junction of Q5 are reverse biased and there is no tendency for the error voltage to change. The output of the charge pump varies between one V_{BE} and three V_{BE} as the phase difference of R and V varies from minus 2π to plus 2π. If this signal is filtered to remove the high-frequency components, the phase detector transfer function, K_ϕ, of approximately 0.12 volt/radian is obtained (see Figure 5).

The specified gain constant of 0.12 volt/radian may not be obtained if the amplifier/filter combination is improperly designed. As indicated previously, the charge pump delivers pump commands of about 2.25 volts on the positive swings and 0.75 volt on the negative swings for a mean no-pump value of 1.5 volts. If the filter amplifier is biased to threshold "on" at 1.5 volts, then the pump up and down voltages have equal effects. The pump signals are established by V_{BE}s of transistors with milliamperes of current flowing. On the other hand, the transistors included for use as a filter amplifier will have very small currents flowing and will have correspondingly lower V_{BE}s — on the order of 0.6 volt each for a threshold of 1.2 volts. Any displacement of the threshold from 1.5 volts causes an increase in gain in one direction and a reduction in the other. The transistor configuration provided is hence not optimum but does allow for the use of an additional transistor to improve filter response. This addition also results in a non-symmetrical response since the threshold is now approximately 1.8 volts. The effective positive swing is limited to 0.45 volt while the negative swing below threshold can be greater than 1.0 volt. This means that the loop gain when changing from a high frequency to a lower frequency is less than when changing in the opposite direction. For type two loops this tends to increase overshoot when going from low to high and increases damping in the other direction. These problems and the selection of external filter components are intimately related to system requirements and are discussed in detail in the filter design section.

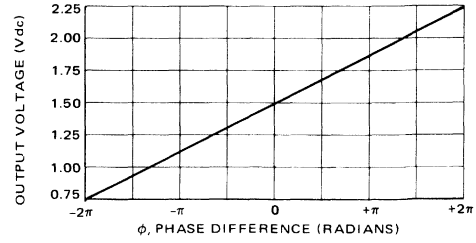
FIGURE 5 — PHASE DETECTOR TEST



Pulse Generator A (variable delay) = EH139 or Equiv



Shown for positive phase angle. Reverse A and B for negative phase angle.



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PHASE-LOCKED LOOP COMPONENTS

General

A basic phase-locked loop, when operating properly, will acquire ("lock on") an input signal, track it in frequency, and exhibit a fixed phase relationship relative to the input. In this basic loop, the output frequency will be identical to the input frequency (Figure 6). A fundamental loop consists of a phase detector, amplifier/filter, and voltage-controlled oscillator (Figure 7). It appears and acts like a unity gain feedback loop. The controlled variable is phase; any error between f_{in} and f_{out} is amplified and applied to the VCO in a corrective direction.

FIGURE 6 — BASIC PHASE-LOCKED LOOP FREQUENCY RELATIONSHIP

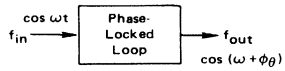
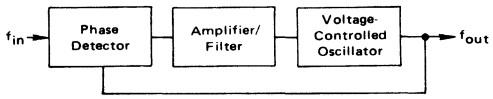


FIGURE 7 — FUNDAMENTAL PHASE-LOCKED LOOP



Simple phase detectors in digital phase-locked loops usually put out a series of pulses. The average value of these pulses is the "gain constant," K_ϕ, of the phase detector — the volts out for a given phase difference, expressed as volts/radian.

The VCO is designed so that its output frequency range is equal to or greater than the required output frequency range of the system. The ratio of change in output frequency to input control voltage is called "gain constant," K_O. If the slope of f_{out} to V_{in} is not linear (i.e., changes greater than 25%) over the expected frequency range, the curve should be piece-wise approximated and the appropriate constant applied for "best" and "worst" case analysis of loop performance.

System dynamics when in lock are determined by the amplifier/filter block. Its gain determines how much phase error exists between f_{in} and f_{out}, and filter characteristics shape the capture range and transient performance. This will be discussed in detail later.

Loop Filter

Fundamental loop characteristics such as capture range, loop bandwidth, capture time, and transient response are controlled primarily by the loop filter. The loop behavior is described by gains in each component block of Figure 8. The output to input ratio reflects a second order low pass filter in frequency response with a static gain of N:

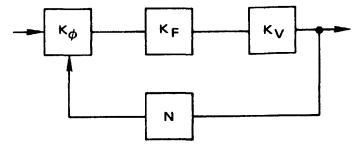
$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{K_\phi K_F K_V}{s + \frac{K_\phi K_F K_V}{N}} \quad (1)$$

where: $K_F = \frac{1 + T_1 s}{T_2 s}$ (2)

$T_1 = R_2C$ and $T_2 = R_1C$ of Figure 4. Therefore,

$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{N(1 + T_1 s)}{\frac{s^2 N T_2}{K_\phi K_V} + T_1 s + 1} \quad (3)$$

FIGURE 8 — GAIN CONSTANTS



K_ϕ = Phase Detector Gain (volts/radian)
K_F = Amplifier/Filter Gain
K_V = VCO Gain (radians/second/volt)
N = Integer Divisor

Both ω_n (loop bandwidth or natural frequency) and ζ (damping factor) are particularly important in the transient response to a step input of phase or frequency (Figure 9), and are defined as:

$$\omega_n = \sqrt{\frac{K_\phi K_V}{N T_2}} \quad (4)$$

$$\zeta = \sqrt{\frac{K_\phi K_V}{N T_2}}\left(\frac{T_1}{2}\right) \quad (5)$$

Using these terms in Equation 3,

$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{N(1 + T_1 s)}{\frac{s^2}{\omega_n^2} + \frac{2\zeta s}{\omega_n} + 1} \quad (6)$$

In a well defined system controlling factors such as ω_n and ζ may be chosen either from a transient basis (time domain response) or steady state frequency plot (roll-off point and peaking versus frequency). Once these two design goals are defined, synthesis of the filter is relatively straight-forward.

Constants K_ϕ, K_V, and N are usually fixed due to other design constraints, leaving T_1 and T_2 as variables to set ω_n and ζ. Since only T_2 appears in Equation 4, it is the easiest to solve for initially.

$$T_2 = \frac{K_\phi K_V}{N \omega_n^2} \quad (7)$$

From Equation 5, we find

$$T_1 = \frac{2\zeta}{\omega_n} \quad (8)$$

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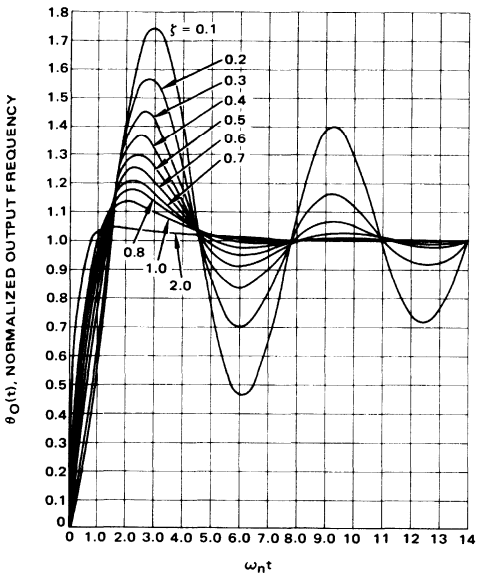
FIGURE 9 — TYPE 2 SECOND ORDER STEP RESPONSE



Using relationships 7 and 8, actual resistor values may be computed:

$$R_1 = \frac{K\phi K_V}{N\omega_n^2 C} \quad (9)$$

$$R_2 = \frac{2\zeta}{\omega_n C} \quad (10)$$

Although fundamentally the range of R_1 and R_2 may be from several hundred to several thousand ohms, sideband considerations usually force the value of R_1 to be set first, and then R_2 and C computed.

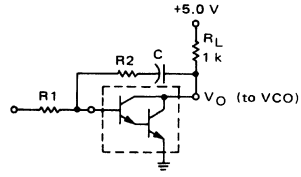
$$C = \frac{K\phi K_V}{N\omega_n^2 R_1} \quad (11)$$

Calculation of passive components R_2 and C (in synthesizers) is complicated by incomplete information on N, which is variable, and the limits of ω_n and ζ during that variance. Equally important are changes in K_V over the output frequency range. Minimum and maximum values of ω_n and ζ can be computed from Equations 4 and 5 when the appropriate worst case numbers are known for all the factors.

Amplifier/filter gain usually determines how much phase error exists between f_{in} and f_{out}, and the filter characteristic shapes capture range and transient performance. A relatively simple, low gain amplifier may usually be used in the loop since many designs are not constrained so much by phase error as by the need to make f_{in} equal f_{out}. Unnecessarily high gains can cause problems in linear loops when the system is out of lock if the amplifier output swing is not adequately restricted since integrating operational amplifier circuits will latch up in time and effectively open the loop.

The internal amplifier included in the MC4344/4044 may be used effectively if its limits are observed. The circuit configuration shown in Figure 10 illustrates the placement of R_1, R_2, C, and load resistor R_L (1 kΩ). Due to the non-infinite gain of this stage ($A_V \approx 30$) and other non-ideal characteristics, some restraint must be placed on passive component selection. Foremost is a lower limit on the value of R_2 and an upper limit on R_1. Placed in order of priority, the recommendations are as follows: (a) R2 > 50 Ω, (b) R1/R2 ≤ 10, (c) 1 kΩ < R1 < 5 kΩ.

FIGURE 10 — USING MC4344/4044 LOOP AMPLIFIER



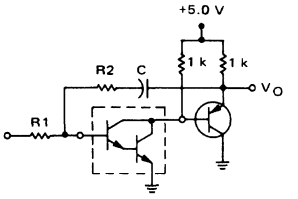
Limit (c) is the most flexible and may be violated with either higher sidebands and phase error (R_1 > 5 kΩ) or lower phase detector gain (R_1 < 1 kΩ). If limit (b) is exceeded, loop bandwidth will be less than computed and may not have any similarity to the prediction. For an accurate reproduction of calculated loop characteristics one should go to an operational amplifier which has sufficient gain to make limit (b) readily satisfied. Limit (a) is very important because T_1 in Equation 5 is in reality composed of three elements:

$$T_1 = C\left(R_2 - \frac{1}{g_m}\right) \quad (12)$$

where g_m = transconductance of the common emitter amplifier.

Normally g_m is large and T_1 nearly equals R_2C, but resistance values below 50 Ω can force the phase-compensating "zero" to infinity or worse (into the right half plane) and give an unstable system. The problem can be circumvented to a large degree by buffering the feedback with an emitter follower (Figure 11). Inequality (a) may then be reduced by at least an order of magnitude (R_2 > 5 Ω) keeping in mind that electrolytic capacitors used

FIGURE 11 — AMPLIFIER CAPABLE OF HANDLING LOWER R2



as C may approach this value by themselves at the frequency of interest (ω_n).

Larger values of R_1 may be accommodated by either using an operational amplifier with a low bias current ($I_b < 1.0\ \mu A$) as shown in Figure 12 or by buffering the internal Darlington pair with an FET (Figure 13). It is vitally important, however, that the added device be operated at zero V_{GS}. Source resistor R_4 should be adjusted for this condition (which amounts to I_{DSS} current for the FET). This insures that the overall amplifier input threshold remains at the proper potential of approximately two base-emitter drops. Use of an additional emitter follower instead of the FET and R_4 (Figure 14) gives a threshold near the upper limit of the phase detector charge pump, resulting in an extremely unsymmetrical phase detector gain in the pump up versus pump down mode. It is not unusual to note a 5:1 difference in K_ϕ for circuits having the bipolar buffer stage. If the initial design can withstand this variation in loop gain and remain stable, the approach should be considered since there are no critical adjustments as in the FET circuit.

FIGURE 12 — USING AN OPERATIONAL AMPLIFIER TO EXTEND THE VALUE OF R1

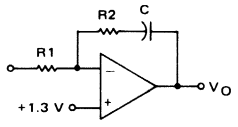


FIGURE 13 — FET BUFFERING TO RAISE AMPLIFIER INPUT IMPEDANCE

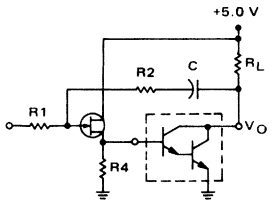
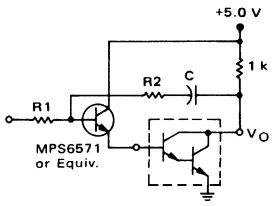


FIGURE 14 — EMITTER FOLLOWER BUFFERING OF AMPLIFIER INPUT



DESIGN PROBLEMS AND THEIR SOLUTIONS

Dynamic Range

A source of trouble for all phase-locked loops, as well as most electronics is simply overload or lack of sufficient dynamic range. One limit is the amplifier output drive to the VCO. Not only must a designer note the outside limits of the dc control voltage necessary to give the output frequency range, he must also account for the worst case of overshoot expected for the system. Relatively large damping factors ($\zeta = 0.5$) can contribute significant amounts of overshoot (30%). To be prepared for the worst case output swing the amplifier should have as much margin to positive and negative limits as the expected swing itself. That is, if a two-volt swing is sufficient to give the desired output frequency excursion, there should be at least a two-volt cushion above and below maximum expected steady-state values on the control line.

This increase in range, in order to be effective, must of course by followed by an equivalent range in the VCO or there is little to be gained. Any loss in loop gain will in general cause a decrease in ζ and a consequent increase in overshoot and ringing. If the loss in gain is caused by saturation or near saturation conditions, the problem tends to accelerate towards a situation where the system settles in not only a slow but oscillator manner as well.

Loss of amplifier gain may not be due entirely to normal system damping considerations. In loops employing digital phase detectors, an additional problem is likely to appear. This is due to amplifier saturation during a step input when there is a maximum phase detector output simultaneous with a large transient overshoot. The phase detector square wave rides on top of the normal transient and may even exceed the amplifier output limits imposed above. Since the input frequency will exceed the R_2C time constant, gain K_F for these annoying pulses will be R_2/R_1. Ordinarily this ratio will be less than 1, but some circumstances dictate a low loop gain commensurate with a fairly high ω_n. For these cases, R_2/R_1 may be higher than 10 and cause pulse-wise saturation of the amplifier. Since the dc control voltage is an average of phase detector pulses, clipping can be translated into a reduction in gain with all the "benefits" already outlined, i.e., poor settling time. An easy remedy to apply in many cases is a simple RC low pass section preceding or together with the integrator-lag section. To make transient suppression independent of amplifier response, the network may be imbedded within the input resistor R_1 (Figure 15) or be implemented by placing a feedback capacitor across R_2 (Figure 16). Besides rounding off and inhibiting pulses, these networks add an additional pole to the loop and may cause further overshoot if the cutoff frequency (ω_c) is too close to ω_n. If at all possible the cutoff point should be five to ten times ω_n. How far ω_c can be placed from ω_n depends on the input frequency relationship to ω_n since f_{in} is, after all, what is being filtered. A side benefit of this simple RC pulse "flattener" is a reduction in f_{in} sidebands around f_{out} for synthe-

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sizers with N > 1. However, a series of RC filters is not recommended for either extended pulse suppression or sideband improvement as excess phase will begin to build up at the loop crossover ($\approx \omega_n$) and tend to cause instability. This will be discussed in more detail later.

FIGURE 15 — IMPROVED TRANSIENT SUPPRESSION WITH R1 — C_c

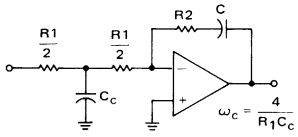
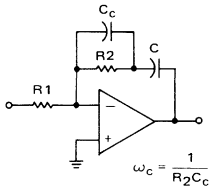


FIGURE 16 — IMPROVED TRANSIENT SUPPRESSION WITH R2 — C_c



Spurious Outputs

Although the major problem in phase-locked loop design is defining loop gain and phase margin under dynamic operating conditions, high-quality synthesizer designs also require special consideration to minimize spurious spectral components — the worst of which is reference-frequency sidebands. Requirements for good sideband suppression often conflict with other performance goals — loop dynamic behavior, suppression of VCO noise, or suppression of other in-loop noise. As a result, most synthesizer designs require compromised specifications. For a given set of components and loop dynamic conditions, reference sidebands should be predicted and checked against design specifications before any hardware is built.

Any steady-state signal on the VCO control will produce sidebands in accordance with normal FM theory. For small spurious deviations on the VCO, relative sideband-to-carrier levels can be predicted by:

$$\frac{\text{sidebands}}{\text{carrier}} \cong \frac{V_{ref} K_V}{2\omega_{ref}} \qquad (13)$$

where V_{ref} = peak voltage value of spurious frequency at the VCO input.

Unwanted control line modulation can come from a variety of sources, but the most likely cause is phase detector pulse components feeding through the loop filter. Although the filter does establish loop dynamic conditions, it leaves something to be desired as a low pass section for reference frequency components.

For the usual case where ω_{ref} is higher than $1/T_2$, the K_F function amounts to a simple resistor ratio:

$$K_F(j\omega)\Big|_{\omega = \omega_{ref}} \cong -\frac{R_2}{R_1} \qquad (14)$$

By substitution of Equations 9 and 10, this signal transfer can be related to loop parameters.

$$K_F(j\omega)\Big|_{\omega = \omega_{ref}} \cong \frac{2\zeta N\omega_n}{K_\phi K_V} = \frac{V_{ref}}{V_\phi} \qquad (15)$$

where V_{ref} = peak value of reference voltage at the VCO input, and

V_ϕ = peak value of reference frequency voltage at the phase detector output.

Sideband levels relative to reference voltage at the phase detector output can be computed by combining Equations 13 and 15:

$$\frac{\text{sideband level}}{f_{out}\ \text{level}} = V_\phi \left(\frac{\zeta N\omega_n}{\omega_{ref} K_\phi}\right) \qquad (16)$$

From Equation 16 we find that for a given phase detector, a given value of R_1 (which determines V_ϕ), and given basic system constraints (N, f_{ref}), only ζ and ω_n remain as variables to diminish the sidebands. If there are few limits on ω_n, it may be lowered indefinitely until the desired degree of suppression is obtained. If ω_n is not arbitrary and the sidebands are still objectionable, additional filtering is indicated.

One item worthy of note is the absence of K_V in Equation 16. From Equation 15 it might be concluded that decreasing K_V would be another means for reducing spurious sidebands, but for constant values of ζ and ω_n this is not a free variable. In a given loop, varying K_V will certainly affect sideband voltage, but will also vary ζ and ω_n.

On the other hand, the choice of ω_n may well affect spectral purity near the carrier, although reference sideband levels may be quite acceptable.

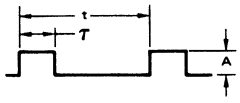
In computing sideband levels, the value of V_ϕ must be determined in relation to other loop components. Residual reference frequency components at the phase detector output are related to the dc error voltage necessary to supply charge pump leakage current and amplifier bias current. From these average voltage figures, spectral components of the reference frequency and its harmonics can be computed using an approximation that the phase detector output consists of square waves τ seconds

wide repeated at t second intervals (Figure 17). A Fourier analysis can be summarized for small ratios of τ/t by:

(1) the average voltage (V_{avg}) is $A(\tau/t)$
(2) the peak reference voltage value (V_ϕ) is twice V_{avg}, and
(3) the second harmonic ($2f_{ref}$) is roughly equal in amplitude to the fundamental.

By knowing the requirements for (1) due to amplifier bias and leakage currents, values for (2) and (3) are uniquely determined.

FIGURE 17 — PHASE DETECTOR OUTPUT



An example of this sideband approximation technique can be illustrated using the parameters specified for the synthesizer design included in the applications information section.

$N_{max} = 30$ $\quad \omega_n = 4500$ rad/s
$K_V = 11.2 \times 10^6$ rad/s/V $\quad R_1 = 2$ kΩ
$K_\phi = 0.12$ V/rad $\quad f_{ref} = 100$ kHz
$\zeta = 0.8$

Substituting these numbers into Equation 16:

$$\frac{\text{sideband}}{f_{out}} = V_\phi \frac{(0.8)(30)(4500)}{2\pi(10^5)(0.111)} \quad (17)$$

$$= V_\phi (1.55) \quad (18)$$

The result illustrates how much reference feedthrough will affect sideband levels. If 1.0 mV peak of reference appears at the output of the phase detector, the nearest sideband will be down 56.2 dB.

If the amplifier section included in the MC4344/4044 is used, with $R_L = 1$ kΩ, some approximations of the value of V_ϕ can be made based on the input bias current and the value of R_1. The phase detector must provide sufficient average voltage to supply the amplifier bias current, I_b, through R_1; when the bias current is about 5.0 μA and R_1 is 2 kΩ, V_{avg} must be 10 mV. From the assumptions earlier concerning the Fourier transform, and with the help of Figure 18, we can see that the phase detector duty cycle will be about 1.7% (A = 0.6 V), giving a fundamental (reference) of 20 mV peak. If this value for V_ϕ is substituted into Equation 18, the resulting sideband ratio represents 30 dB suppression due to this component alone.

In addition to the amplifier bias current, another factor to consider is transistor Q5 reverse leakage current I_L flowing into pin 10 of the MC4344/4044 charge pump. I_L is generally less than 1.0 μA and is no more than 5.0 μA over the temperature range. A typical design value for 25°C is 0.1 μA. Both I_L and amplifier bias current I_B are in a direction to deplenish the charge on filter capacitor C. A second charge pump leakage, I_L', attributed by diode CR1 flows out of pin 5. This current, however, is in a direction to help supply I_B and I_L and thus tends to minimize the discharge of C. Typically I_L' is much less than I_L and, since it is also in a direction to minimize discharge of the filter capacitor, it will be ignored in the following discussion. The total charge removed from C must be replaced by current supplied by the charge pump during the next up-date opportunity. This current flows through R1. To minimize the effects of I_B and I_L a relative small value of R1 should be chosen. A minimum value of 1 kΩ is a good choice.

FIGURE 18 — OUTPUT ERROR CHARACTERISTICS

DUTY CYCLE (%)	PHASE ERROR (Deg)	V_{avg} (mV)	$V_{\phi(peak)}$ (mV)
0.1	0.36	0.6	1.2
0.2	0.72	1.2	2.4
0.3	1.08	1.8	3.6
0.4	1.44	2.4	4.8
0.5	1.80	3.0	6.0
0.6	2.16	3.6	7.2
0.7	2.52	4.2	8.4
0.8	2.88	4.8	9.6
0.9	3.24	5.4	10.8
1.0	3.60	6.0	12.0
2.0	7.2	12.0	24.0
3.0	10.8	18.0	35.9
4.0	14.4	24.0	47.9
5.0	18.0	30.0	59.8
6.0	21.6	36.0	71.6
7.0	25.2	42.0	83.3
8.0	28.8	48.0	95.0
9.0	32.4	54.0	106.6
10.0	36.0	60.0	118.0

After values for C and R_2 have been computed on the basis of loop dynamic properties, the overall sideband to f_{out} ratio computation can be simplified.

Since

$$V_\phi = 2\,V_{avg} \qquad = 2R_1 (I_b + I_L) \left(\frac{R_2}{R_1}\right)$$
$$V_{avg} = (I_b + I_L)\,R_1$$
$$V_\phi = 2\,(I_b + I_L)\,R_1$$

$$V_{ref} = V_\phi \left(\frac{R_2}{R_1}\right) \qquad = 2R_2 (I_b + I_L)$$

we find that

$$\frac{\text{sideband}}{f_{out}} = \frac{V_{ref} K_V}{2\omega_{ref}} \quad (19)$$

$$\frac{\text{sideband}}{f_{out}} = \frac{2R_2(I_b + I_L)K_V}{2\omega_{ref}} \quad (20)$$

Equation 20 indicates that excellent suppression could be achieved if the bias and leakage terms were nulled by current summing at the amplifier input (Figure 19). This has indeed proved to be the case. Experimental results indicate that greater than 60 dB rejection can routinely

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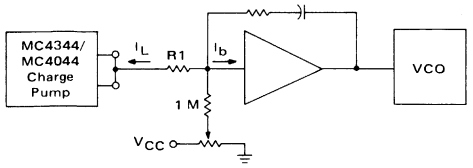
be achieved at a constant temperature. However when nulling fairly large values (> 100 nA), the rejection becomes quite sensitive since leakages are inherently a function of temperature. This technique has proved useful in achieving improved system performance when used in conjunction with good circuit practice and reference filtering.

FIGURE 19 — COMPENSATING FOR BIAS AND LEAKAGE CURRENT



Additional Loop Filtering

So far, only the effects of fundamental loop dynamics on resultant sidebands have been considered. If further sideband suppression is required, additional loop filtering is indicated. However, care must be taken in placement of any low pass rolloff with regard to the loop natural frequency (ω_n). On one hand, the "corner" should be well below (lower than) ω_{ref} and yet far removed (above) from ω_n. Although no easy method for placing the roll-off point exists, a rule of thumb that usually works is:

$$\omega_c = 5\omega_n \qquad (21)$$

Reference frequency suppression per pole is the ratio of ω_c to ω_{ref}.

$$SB_{dB} \cong n\ 20 \log_{10}\left(\frac{\omega_c}{\omega_{ref}}\right) \qquad (22)$$

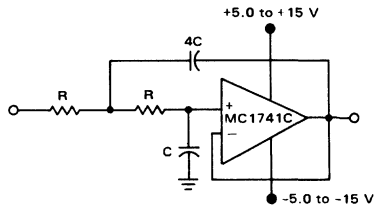
where n is the number of poles in the filter.

Equation 22 gives the additional loop suppression to ω_{ref}; this number should be added to whatever suppression already exists.

For non-critical applications, simple RC networks may suffice, but if more than one section is required, loop dynamics undergo undesirable changes. Loop damping factor decreases, resulting in a high percentage of overshoot and increased ringing since passive RC sections tend to accumulate phase shift more rapidly than signal suppression and part of this excess phase subtracts from the loop phase margin. Less phase margin translates into a lower damping factor and can, in the limit, cause outright oscillation.

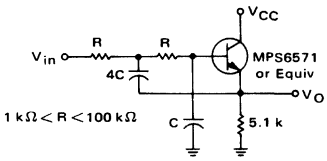
A suitable alternative is an active RC section, Figure 20, compatible with the existing levels and voltages. An active two pole filter (second order section) can realize a more gradual phase shift at frequencies less than the cutoff point and still get nearly equal suppression at frequencies above the cutoff point. Sections designed with a slight amount of peaking ($\zeta \cong 0.5$) show a good compromise between excess phase below cutoff (ω_c), without peaking enough to cause any danger of raising the loop gain for frequencies above ω_n. A fairly non-critical section may simply use an emitter follower as the active device with two resistors and capacitors completing the circuit (Figure 21). This provides a −12 dB/octave (−40 dB/decade) rolloff characteristic above ω_n, though the attenuation may be more accurately determined by Equation 22. If the sideband problem persists, an additional section may be added in series with the first. No more than two sections are recommended since at that time either (1) the constraint between ω_n and ω_{ref} is too close, or (2) reference voltage is modulating the VCO from a source other than the phase detector through the loop amplifier.

FIGURE 20 — OPERATIONAL AMPLIFIER LOW PASS FILTER



1. Choose R
   $1\ k\Omega < R < 1\ M\Omega$
2. $C = \frac{0.5}{\omega_c R}$

FIGURE 21 — EMITTER FOLLOWER LOW PASS FILTER

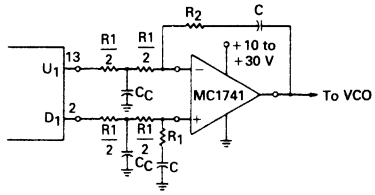


NOTE: If $V_O \geq V_{CC} - 1.0$ V, this stage is susceptible to power supply noise.

Operation without charge pump phase detector #1 of the MC4344/4044 can be implemented quite successfully in many applications without using the charge pump and internal darlington amplifier approach. An operational amplifier filter can be used to process the error information appearing at U1 and D1 (pins 13 and 2) directly (Figure 22).This phase detector/filter approach offers a potentially superior performing system because:

a. Charge pump delay time is eliminated.
b. Charge pump input signed threshold level need not be overcome before error information is obtained. This can result in a substantial improvement in the

FIGURE 22—TYPICAL FILTER AND SUMMING NETWORK



4044's transfer function linearity in the vicinity of zero phase error between the R and V inputs.

c. The filter amplifier ground location can be separated from the phase detector ground.

d. An "optimum" filter amplifier input threshold of approximately two diode drops need not be established.

The filter discussions and relationships developed for integrator-log filter sections can be applied to the system of Figure 22 and the previously derived equations can be used to determine values for R1, R2 and C.

It may be desirable to split each of the R1 resistors and incorporate a capacitor to ground in a manner similar to that shown in Figure 15. This should improve transient suppression and provide integration of the U1 and D1 signals to better enable the operational amplifier to develop corrective error information from very narrow U1 and D1 pulse widths.

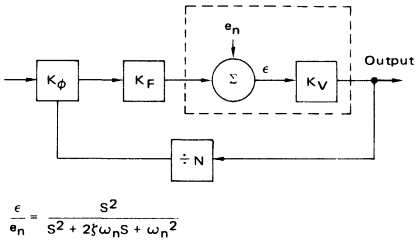
Phase error for the circuit in Figure 22 will result from input offset voltage in the operational amplifier, resistor mismatch and mismatch between the phase detector output states appearing at U1 and D1. Phase error can be trimmed to zero initially by adjusting either the amplifier input offset or one of the R1 resistors.

VCO Noise

Effects of noise within the VCO itself can be evaluated by considering a closed loop situation with an external noise source, e_n, introduced at the VCO (Figure 23). Resultant modulation of the VCO by error voltage, ε, is a second order high pass function:

$$\frac{\varepsilon}{e_n} = \frac{S^2}{S^2 + \frac{ST_1K\phi K_V}{T_2N} + \frac{K\phi K_V}{T_2N}} = \frac{S_2}{S^2 + 2\zeta\omega_n S + \omega_n{}^2} \quad (23)$$

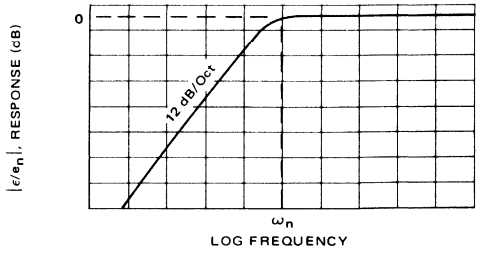
FIGURE 23 — EFFECTS OF VCO NOISE



$$\frac{\epsilon}{e_n} = \frac{S^2}{S^2 + 2\zeta\omega_n S + \omega_n{}^2}$$

This function has a slope of 12 dB/octave at frequencies less than ω_n (loop natural frequency), as shown in Figure 24. This means that noise components in the VCO above ω_n will pass unattenuated and those below will have some degree of suppression. Therefore choice of loop natural frequency may well rest on VCO noise quality.

FIGURE 24 — LOOP RESPONSE TO VCO NOISE

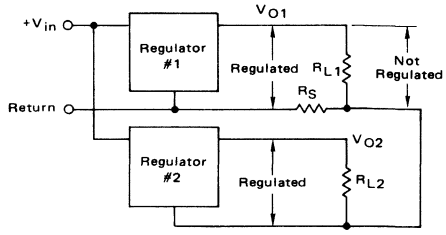


Other Spurious Responses

Spurious components appearing in the output spectrum are seldom due to reference frequency feedthrough alone. Modulation of any kind appearing on the VCO control line will cause spurious sidebands and can come in through the loop amplifier supply, bias circuitry in the control path, a translator, or even the VCO supply itself. Some VCOs have a relatively high sensitivity to power supply variation. This should be investigated and its effects considered. Problems of this nature can be minimized by operating all devices except the phase detector, charge pump, and VCO from a separate and well isolated supply. A common method uses a master supply of about 10 or 12 volts and two regulators to produce voltages for the PLL — one for all the logic (including the phase detector) and the other for all circuitry associated with the VCO control line.

Sideband and noise performance is also a function of good power supply and regulator layout. As mentioned earlier, extreme care should be exercised in isolating the control line voltage to the VCO from influences other than the phase detector. This not only means good voltage regulation but ac bypassing and adherence to good grounding techniques as well. Figure 25 shows two separate regulators and their respective loads. Resistor R_S is a small stray resistance due to a common thin ground return for both R_{L1} and R_{L2}. Any noise in R_{L2} is now reproduced (in a suppressed form) across R_{L1}. Load current from R_{L1} does not affect the voltage across R_{L2}. Even though the regulators may be quite good, they can hold V_O constant only across their outputs, not necessarily across the load (unless remote sensing is used).

FIGURE 25 — LOOP VOLTAGE REGULATION



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One solution to the ground-coupled noise problem is to lay out the return path with the most sensitive regulated circuit at the farthest point from power supply entry as shown in Figure 26.

Even for regulated subcircuits, accumulated noise on the ground bus can pose major problems since although the cross currents do not produce a differential load voltage directly, they do produce essentially common mode noise on the regulators. Output differential load noise then is a function of the input regulation specification. By far the best way to sidestep the problem is to connect each subcircuit ground to the power supply entry return line as shown in Figure 27.

FIGURE 26 — REGULATOR LAYOUT

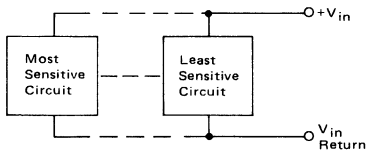
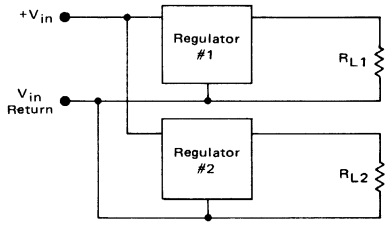


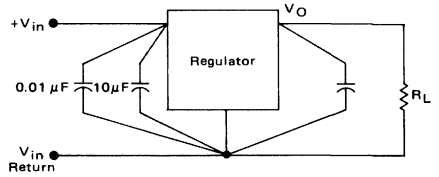
FIGURE 27 — REGULATOR GROUND CONNECTION



In Figures 25 and 27, R_{L1} and R_{L2} represent component groups in the system. The designer must insure that all ground return leads in a specific component group are returned to the common ground. Probably the most overlooked components are bypass capacitors. To minimize sidebands, extreme caution must be taken in the area immediately following the phase detector and through the VCO. A partial schematic of a typical loop amplifier and filter is shown in Figure 28 to illustrate the common grounding technique.

Bypassing in a phase-locked loop must be effective at both high frequencies and low frequencies. One capacitor in the 1.0-to-10 μF range and another between 0.01 and 0.001 μF are usually adequate. These can be effectively utilized both at the immediate circuitry (between supply and common ground) and the regulator if it is some distance away. When used at the regulator, a single electrolytic capacitor on the output and a capacitor pair at the input is most effective (Figure 29). It is important, again, to note that these bypasses go from the input/output pins to as near the regulator ground pin as possible.

FIGURE 29 — SUGGESTED BYPASSING PROCEDURE



APPLICATIONS INFORMATION

Frequency Synthesizers

The basic PLL discussed earlier is actually a special case of frequency synthesis. In that instance, $f_{out} = f_{in}$, although normally a programmable counter in the feedback loop insures the general rule that $f_{out} = Nf_{in}$ (Figure 30). In the synthesizer f_{in} is usually constant (crystal controlled) and f_{out} is changed by varying the programmable divider (÷ N). By stepping N in integer increments, the output frequency is changed by f_{in} per increment. In com-

FIGURE 30 — PHASE-LOCKED LOOP WITH PROGRAMMABLE COUNTER

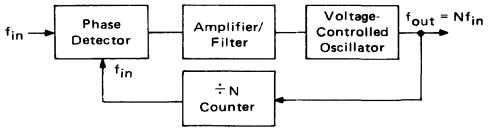
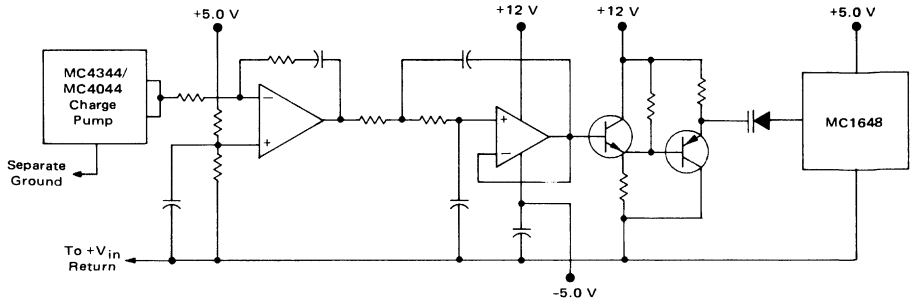


FIGURE 28 — PARTIAL SCHEMATIC OF LOOP AMPLIFIER AND FILTER



munication use, this input frequency is called the "channel spacing" or, in general, it is the reference frequency.

There is essentially no difference in loop dynamic problems between the basic PLL and synthesizers except that synthesizer designers must contend with problems peculiar to loops where N is variable and greater than 1. Also, sidebands or spectral purity usually require special attention. These and other aspects are discussed in greater detail in AN-535. The steps for a suitable synthesis procedure may be summarized as follows:

Synthesis Procedure

1. Choose input frequency. (f_{ref} = channel spacing)
2. Compute the range of digital division:

$$N_{max} = \frac{f_{max}}{f_{ref}}$$

$$N_{min} = \frac{f_{min}}{f_{ref}}$$

3. Compute needed VCO range:

$$(2f_{max} - f_{min}) < f_{VCO} < (2f_{min} - f_{max})$$

4. Choose minimum ζ from transient response plot, Figure 9. A good starting point is $\zeta = 0.5$.
5. Choose ω_n from needed response time (Figure 9):

$$\omega_n = \frac{\omega_n t}{t}$$

6. Compute C:

$$C = \frac{K_\phi K_V}{N_{max}\omega_n^2 R_1}$$

7. Compute R_2:

$$R_2 = \frac{2\zeta_{min}}{\omega_n C}$$

8. Compute ζ_{max}:

$$\zeta_{max} = \zeta_{min}\sqrt{\frac{N_{max}}{N_{min}}}$$

9. Check transient response of ζ_{max} for compatibility with transient specification.
10. Compute expected sidebands:

$$\frac{\text{sideband}}{f_{out}} \cong \frac{(I_b + I_L)R_2K_V}{\omega_{ref}} \qquad \text{(A)}$$

(I_L is about 100 nA at T_J = 25°C.)

11. If step 10 yields larger sidebands than are acceptable, add a single pole at the loop amplifier by splitting R_1 and adding C_c as shown in Figure 15:

$$C_c \cong \frac{0.8}{R_1\omega_n}$$

Added sideband suppression (dB) is:

$$dB \cong 20\log_{10}\frac{1}{\sqrt{1 + \frac{\omega_{ref}^2}{25(\omega_n)^2}}} \qquad \text{(B)}$$

12. If step 11 still does not give the desired results, add a second order section at $\omega_c = 5\,\omega_n$ using either the configuration of Figure 20 or 21. The expected improvement is twice that of the single pole in step 11.

$$dB \cong 40\log_{10}\frac{1}{\sqrt{1 + \frac{\omega_{ref}^2}{25(\omega_n)^2}}} \qquad \text{(C)}$$

Total sideband rejection is then the total of $20\log_{10}$(A) + (B) + (C).

Design Example (Figure 31)

Assume the following requirements:
Output frequency, f_{out} = 2.0 MHz to 3.0 MHz
Frequency steps, f_{in} = 100 kHz
Lockup time between channels (to 5%) = 1.0 ms
Overshoot < 20%.
Minimum sideband suppression = −30 dB

From the steps of the synthesis procedure:

1. $f_{ref} = f_{in}$ = 100 kHz
2. $N_{max} = \frac{f_{max}}{f_{ref}} = \frac{3.0\text{ MHz}}{0.1\text{ MHz}} = 30$

   $N_{min} = \frac{f_{min}}{f_{ref}} = \frac{2.0\text{ MHz}}{0.1\text{ MHz}} = 20$
3. VCO range:
   The VCO output frequency range should extend beyond the specified minimum-maximum limits to accommodate the overshoot specification. In this instance f_{out} should be able to cover an additional 20% on either end. End limits on the VCO are:

   $f_{out}max \geq 3.0 + 0.2(1.0) = 3.2$ MHz
   $f_{out}min \leq 2.0 - 0.2(1.0) = 1.8$ MHz

   This VCO range (≈ 1.8:1) is realizable with the MC4324/4024 voltage controlled multivibrator. From Figure 5 of the MC4324/4024 data sheet we find the required tuning capacitor value to be 120 pF and the VCO gain, K_V, typically 11 x 10^6 rad/s/v.
4. From the step response curve of Figure 9, $\zeta = 0.8$ will produce a peak overshoot less than 20%.
5. Referring to Figure 9, overshoot with $\zeta = 0.8$ will settle to within 5% at $\omega_n t = 4.5$. Since the required lock-up time is 1.0 ms,

$$\omega_n = \frac{\omega_n t}{t} = \frac{4.5}{t} = \frac{4.5}{0.001} = (4.5)(10^3)\text{rad/s}$$

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6. In order to compute C, phase detector gain and R1 must be selected. Phase detector gain, K_ϕ, for the MC4344/4044 is approximately 0.1 volt/radian with $R_1 = 1\ k\Omega$. Therefore,

$$C = \frac{(0.1)(11 \times 10^6)}{(30)(4.5 \times 10^3)^2(10^3)} = 1.8\ \mu F$$

7. At this point, R_2 can be computed:

$$R_2 = \frac{2\zeta_{min}}{\omega_n C} = \frac{1.6}{(4.5 \times 10^3)(1.8 \times 10^{-6})} = 200\ \Omega$$

8. $\zeta_{max} = \zeta_{min}\sqrt{\frac{N_{max}}{N_{min}}} = 0.98$

9. Figure 9 shows that $\zeta = 0.98$ will meet the settling time requirement.
10. Sidebands may be computed for two cases: (1) with I_L (charge pump leakage current) nominal (100 nA), and (2) with I_L maximum (5.0 μA). A value of 5 μA will also be assumed for the amplifier bias current, i_b.

$$\left.\frac{\text{sideband}}{f_{out}}\right|_{max} = \frac{(10 \times 10^{-6})(200)(11 \times 10^6)}{6.28 \times 10^5} \cong 35 \times 10^{-3}$$

The sideband-to-center frequency ratio nominally will be:

$$\left.\frac{\text{sideband}}{f_{out}}\right|_{nom} = \frac{5.1}{10} \times 35 \times 10^{-3}$$

$$= 20 \log_{10}(17.85 \times 10^{-3}) \cong -35\ dB$$

If desired additional sideband filtering can be obtained as noted in steps 11 and 12.

11. By splitting R_1 and C_C, further attenuation can be gained. The magnitude of C_C is approximately:

$$C_C = \frac{0.8}{R_1\omega_n} = \frac{0.8}{(10^3)(4.5)(10^3)} \cong 0.18\ \mu F$$

Improvement in sidebands will be:

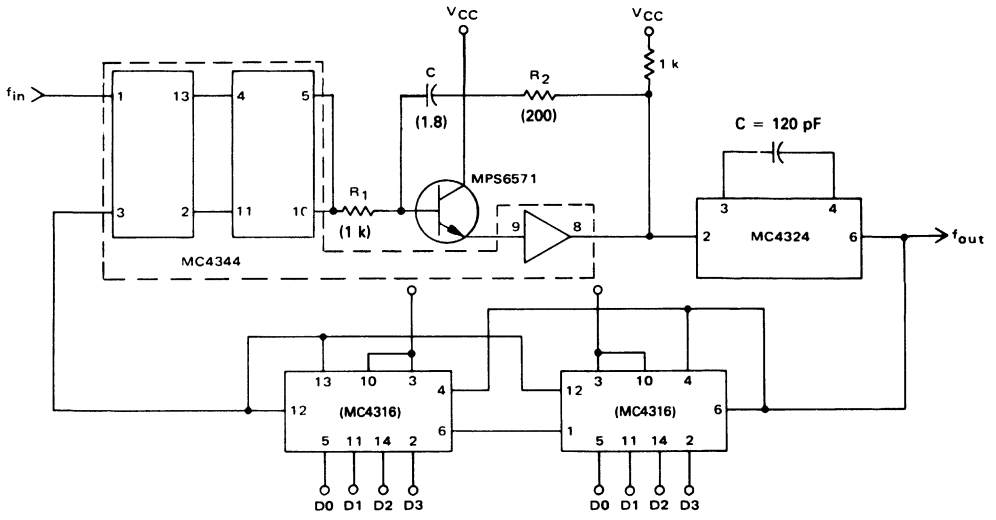
$$20 \log_{10} \frac{1}{\sqrt{1 + \frac{(2\pi \times 10^5)^2}{25(4.5 \times 10^3)^2}}} = -28\ dB$$

Nominal suppression is now −63 dB. Worst-case is 6 dB higher than nominal suppression of −57 dB. This is well within the −30 dB design requirement, step 12 is included for completeness only.

12. Attenuation of a second order filter is double that of the single order filter section described in step11. The calculations for a second order filter indicate an additional −56 dB of sideband rejection. Figures 20 and 21 show two second order filter configurations. If R is assigned a value of 10 kΩ then C may be calculated.

$$C = \frac{0.1}{\omega_n R} = \frac{0.1}{(4.5 \times 10^3)(10^4)} = 0.0022\ \mu F$$

FIGURE 31 — CIRCUIT DIAGRAM OF TYPE 2 PHASE-LOCKED LOOP



Clock Recovery from Phase-Encoded Data

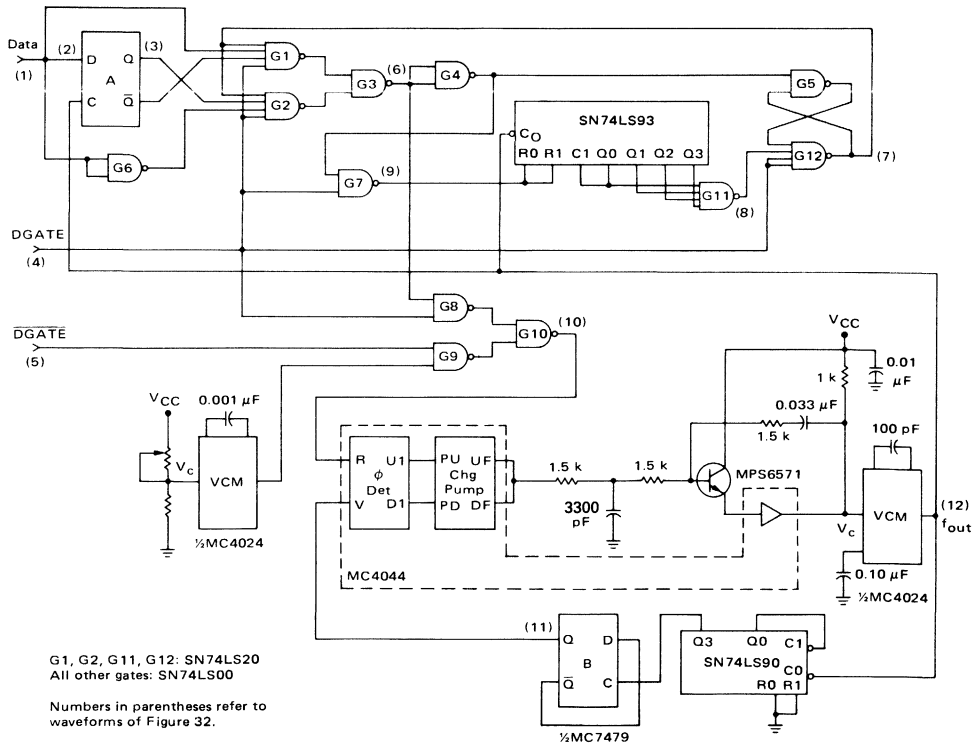
The electro-mechanical system used for recording digital data on magnetic tape often introduces random variations in tape speed and data spacing. Because of this and the encoding technique used, it is usually necessary to regenerate a synchronized clock from the data during this read cycle. One method for doing this is to phase-lock a voltage controlled multivibrator to the data as it is read (Figure 32).

A typical data block using the phase encoded format is shown in row 1 of Figure 33. The standard format calls for recording a preamble of forty "0"s followed by a single "1"; this is followed by from 18 to 2048 characters of data and a postamble consisting of a "1" followed by forty "0"s. The encoding format records a "0" as a transition from low to high in the middle of a data cell. A "1" is indicated by a transition from high to low at the data cell midpoint. When required, phase transitions occur at the end of data cells. If a string of either consecutive "0"s or consecutive "1"s is recorded, the format duplicates the original clock; the clock is easily recovered by straight forward synchronization with a phase-locked loop. In the general case, where the data may appear in any order, the phase-encoded data must be processed to obtain a single pulse during each data cell before it is applied to the phase detector. For example, if the data consisted only of alternating "1"s and "0"s, the phase-encoded format would result in a waveform equal to one-half the original clock frequency. If this were applied directly to the loop, the VCM would of course move down to that frequency. The encoding format insures that there will be a transition in the middle of each data time. If only these transitions are sensed they can be used to regenerate the clock. The schematic diagram of Figure 32 indicates one method of accomplishing this.

The logic circuitry generates a pulse at the midpoint of each data cell which is then applied to the reference input of the phase detector. The loop VCM is designed to operate at some multiple of the basic clock rate. The VCM frequency selected depends on the decoding resolution desired and other system timing requirements. In this example, the VCM operates at twenty-four times the clock rate (Figure 33, Row 12).

Referring to Figure 32 and the timing diagram of Figure 33, the phase-encoded data (Figure 33, Row 1) is combined with a delayed version of itself (output of flip-flop A row 3) to provide a positive pulse out of G3 for every transition of the input signal. Portions of the data block are shown expanded in row 2 of Figure 33. Flip-flop A delays the incoming data of one-half of a VCM clock period. Gates G1, G2 and G3 implement the logic Exclusive OR of waveforms 1 and 3 except when inhibited by DGATE (row 4) or the output of G12 (row 7). DGATE and

FIGURE 32 — CLOCK RECOVERY FROM PHASE-ENCODED DATA



G1, G2, G11, G12: SN74LS20
All other gates: SN74LS00

Numbers in parentheses refer to waveforms of Figure 32.

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its complement, $\overline{DGATE}$, serve to initialize the circuitry and insure that the first transition of the data block (a phase transition) is ignored. The MC7493 binary counter and the G5-G12 latch generate a suitable signal for gating out G3 pulses caused by phase transitions at the end of a data cell, such as the one shown dashed in row 6.

The initial data pulse from G3 sets G12 low and is combined with DGATE in G7 to reset the counter to its zero state. Subsequent VCM clock pulses now cycle the counter and approximately one-third of the way through the next data cell the counter's full state is decoded by G11, generating a negative transition. This causes G12 to go high, removing the inhibit signal until it is again reset by the next data transition. This pulse also resets the counter, continuing the cycle and generating a positive pulse at the midpoint of each data cell as required.

Acquisition time is reduced if the loop is locked to a frequency approximately the same as the expected data rate during inter-block gaps. In Figure 32, this is achieved by operating the remaining half of the dual VCM at slightly less than the data rate and applying it to the reference input of the phase detector via the G8-G9-G10 data selector. When data appears, DGATE and $\overline{DGATE}$ cause the output of G3 to be selected as the reference input to the loop.

The loop parameters are selected as a compromise between fast acquisition and jitter-free tracking once synchronization is achieved. The resulting filter component values indicated in Figure 32 are suitable for recovering the clock from data recorded at a 120 kHz rate, such as would result in a tape system operating at 75 i.p.s. with a recording density of 1600 b.p.i. Synchronization is achieved by approximately the twenty-fourth bit time of the preamble. The relationship between system requirements and the design procedure is illustrated by the following sample calculation:

Assume a −3.0 dB loop bandwidth much less than the input data rate (≈ 120 kHz), say 10 kHz. Further, assume a damping factor of $\zeta = 0.707$. From the expression for loop bandwidth as a function of damping factor and undamped natural frequency, ω_n, calculate ω_n as:

$$\omega_{-3\,dB} = \omega_n \left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right)^{1/2} \quad (24)$$

or for $\omega_{-3\,dB} = (2\pi)10^4$ rad/s and $\zeta = 0.707$:

$$\omega_n = \frac{(2\pi)10^4}{2.06} = (3.05)10^4 \text{ rad/s}$$

As a rough check on acquisition time, assume that lockup should occur not later than half-way through a 40-bit preample, or for twenty 8.34 μs data periods.

$$\omega_n t = (3.05)10^4(20)(8.34)10^{-6} = 5.1 \quad (26)$$

From Figure 9, the output will be within 2 to 3% of its final value for $\omega_n t \approx 5$ and $\zeta = 0.707$. The filter components are calculated by:

$$\frac{K_\phi K_V}{R_1 CN} = \omega_n^2 \quad (27)$$

and

$$\frac{K_\phi K_V R_2}{R_1 N} = 2\zeta\omega_n \quad (28)$$

where $K_\phi = 0.115$ v/rad
$K_V = (18.2)\ 10^6$ rad/s/volt
$N = 24$ = Feedback divider ratio
$\omega_n = (3.05)\ 10^4$ rad/s
$\zeta = 0.707$

$$\frac{K_\phi K_V}{N} = \frac{(0.115)(18.2)10^6}{24} = (8.72)10^4$$

From Equation 27:

$$R_1 C = \frac{K_\phi K_V}{N\omega_n^2} = \frac{(8.72)10^4}{(3.05)^2 10^8} = (9.34)10^{-5}$$

From Equation 28:

$$\frac{R_2}{R_1} = \frac{2\zeta\omega_n N}{K_\phi K_V} = \frac{2(0.707)(3.05)10^4}{(8.72)10^4} = 0.494 \approx \tfrac{1}{2}$$

Let $R_1 = 3.0$ kΩ; then $R_2 = 1.5$ kΩ and

$$C = \frac{(9.34)10^{-5}}{(3.0)10^3} = (3.1)10^{-8}$$

or using a close standard value, use C = 0.033 μF. Now add the additional prefiltering by splitting R_1 and selecting a time constant for the additional section so that it is large with respect to R_2C_2.

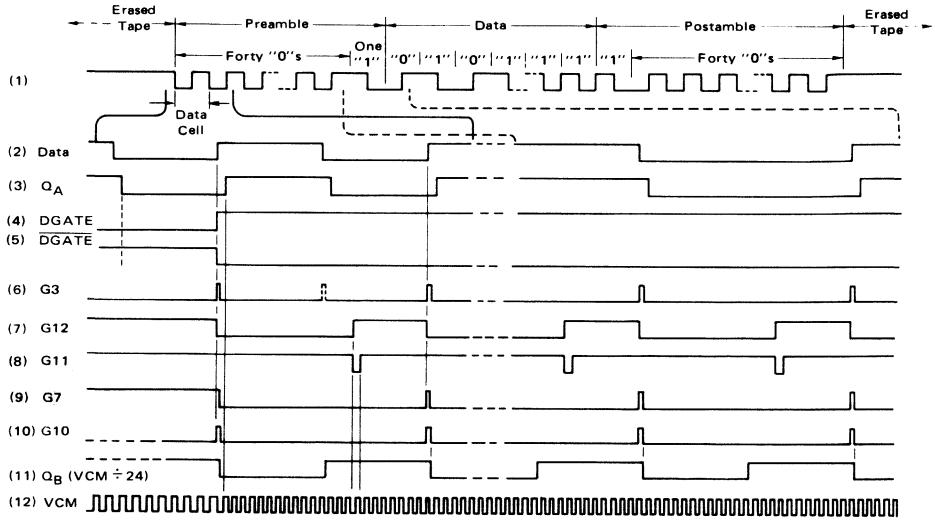
$$10(\tfrac{1}{2}R_1)C_C = R_2 C$$

or

$$C_C = \frac{2R_2 C}{10R_1} = \frac{2(1.5)10^3(3.3)10^{-8}}{10(3.0)10^3} = 3300 \text{ pF}$$

6

FIGURE 33 — TIMING DIAGRAM — CLOCK RECOVERY FROM PHASE-ENCODED DATA



MOTOROLA

MC12002

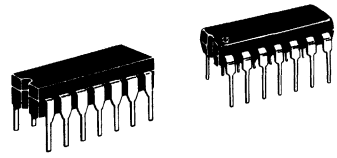
ANALOG MIXER

The MC12002 is a double balanced analog mixer, including an input amplifier feeding the mixer carrier port and a temperature compensated bias regulator. The input circuits for both the amplifier and mixer are differential amplifier circuits. The on-chip regulator provides all of the required biasing.

This circuit is designed for use as a balanced mixer in high-frequency wide-band circuits. Other typical applications include suppressed carrier and amplitude modulation, synchronous AM detection, FM detection, phase detection, and frequency doubling, at frequencies up to UHF.

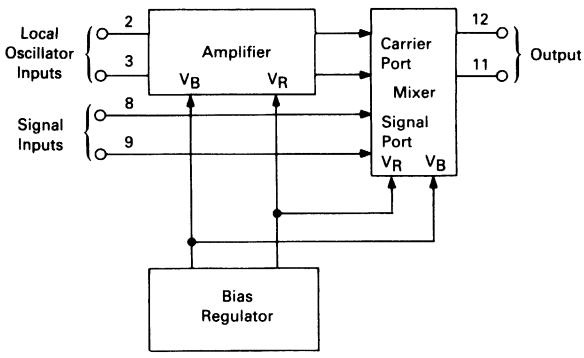
ANALOG MIXER

P SUFFIX
PLASTIC PACKAGE
CASE 646

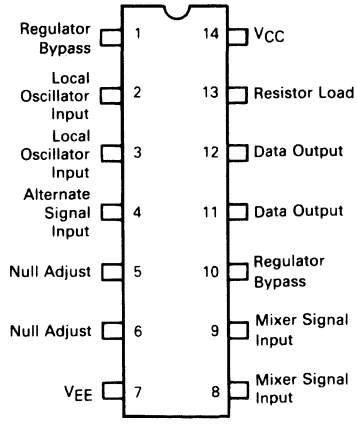


L SUFFIX
CERAMIC PACKAGE
CASE 632

LOGIC DIAGRAM



PIN ASSIGNMENT



6

ELECTRICAL CHARACTERISTICS

										TEST VOLTAGE VALUES (Volts)			
										V_{IHmax}	V_{ILmin}	V_{CC}	
										+2.9	+2.0	+5.0	
			Test Limits							VOLTAGE APPLIED TO PINS LISTED BELOW			
		Pin Under	−30°C		+25°C		+85°C						
Characteristic	Symbol	Test	Min	Max	Min	Max	Min	Max	Unit	V_{IHmax}	V_{ILmin}	V_{CC}	Gnd
Power Supply Drain	I_{CC}	14	—	—	—	16	—	—	mAdc	—	—	11,12,14	5,6,7
Input Current	I_{inH}	2	—	—	—	0.75	—	—	mAdc	2	—	11,12,14	5,6,7
		3	—	—	—	0.75	—	—	mAdc	3	—	11,12,14	5,6,7
		8	—	—	—	0.75	—	—	mAdc	8	—	11,12,14	5,6,7
		9	—	—	—	0.75	—	—	mAdc	9	—	11,12,14	5,6,7
	I_{inL}	2	—	—	−0.7	—	—	—	mAdc	—	2	11,12,14	5,6,7
		3	—	—	−0.7	—	—	—	mAdc	—	3	11,12,14	5,6,7
		8	—	—	−0.7	—	—	—	mAdc	—	8	11,12,14	5,6,7
		9	—	—	−0.7	—	—	—	mAdc	—	9	11,12,14	5,6,7
Output Current	IO_1	11	—	—	0.7	1.3	—	—	mAdc	—	—	11,12,14	7
		12	—	—	0.7	1.3	—	—	mAdc	—	—	11,12,14	7
	IO_2	11	—	—	2.1	3.9	—	—	mAdc	—	—	11,12,14	5,6,7
		12	—	—	2.1	3.9	—	—	mAdc	—	—	11,12,14	5,6,7
	I_{out}	11	—	—	4.2	7.8	—	—	mAdc	2,9	—	11,12,14	5,6,7
		11	—	—	4.2	7.8	—	—	mAdc	3,8	—	11,12,14	5,6,7
		12	—	—	4.2	7.8	—	—	mAdc	2,8	—	11,12,14	5,6,7
		12	—	—	4.2	7.8	—	—	mAdc	3,9	—	11,12,14	5,6,7
Differential Current	ΔIO_1	11,12	−100	+100	−100	+100	−100	+100	μAdc	—	—	11,12,14	7
	ΔIO_2	11,12	−200	+200	−200	+200	−200	+200	μAdc	—	—	11,12,14	5,6,7
Bias Voltage	V_{Bias}	1	2.33	2.53	2.32	2.52	2.3	2.5	Vdc	—	—	11,12,14	5,6,7
		4	390	590	400	600	410	610	mVdc	—	—	11,12,14	5,6,7
		5	275	415	285	425	295	435	mVdc	—	—	11,12,14	7
		6	275	415	285	425	295	435	mVdc	—	—	11,12,14	7
		10	1.26	1.46	1.185	1.385	1.105	1.305	Vdc	—	—	11,12,14	5,6,7
										Pulse In	Pulse Out	−3.0 V	Gnd	V_{EE}
AC Gain (See Figure 1)	A_V	11	—	—	5.0	—	—	—	V/V	2	11	9	14	7
(Frequency = 100 MHz) *Note		11	—	—	0.28	—	—	—	V/V	8	11	3	14	7

*Note: AC Gain is a function of collector load impedance.

ANALOG MIXER CIRCUIT SCHEMATIC

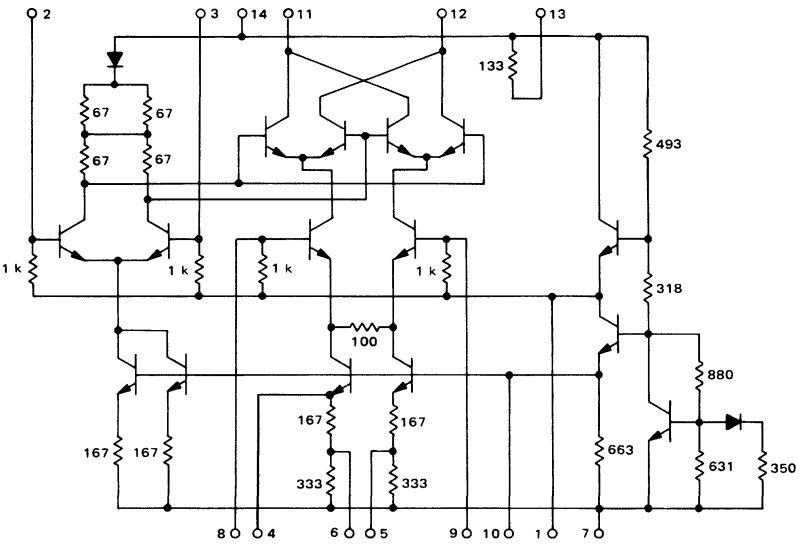
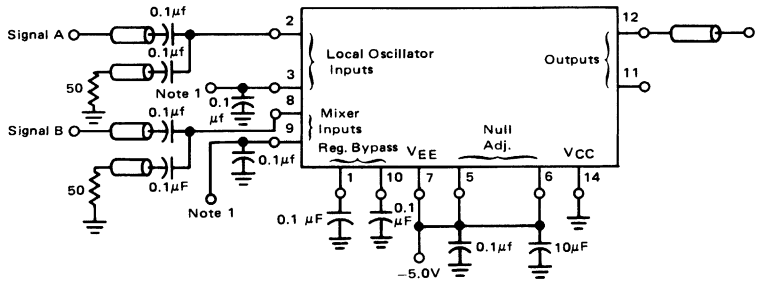


FIGURE 1 — A.C. GAIN TEST



Note 1:
V_{IL} = −3.0 V on pin 3 when pin 8 is under test.
V_{IL} = −3.0 V on pin 9 when pin 2 is under test.

Signal A = 30 mV p-p

Signal B = 300 mV p-p

Freq. = 100 MHz

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.
The unused output is connected to a 50-ohm resistor to ground.

6

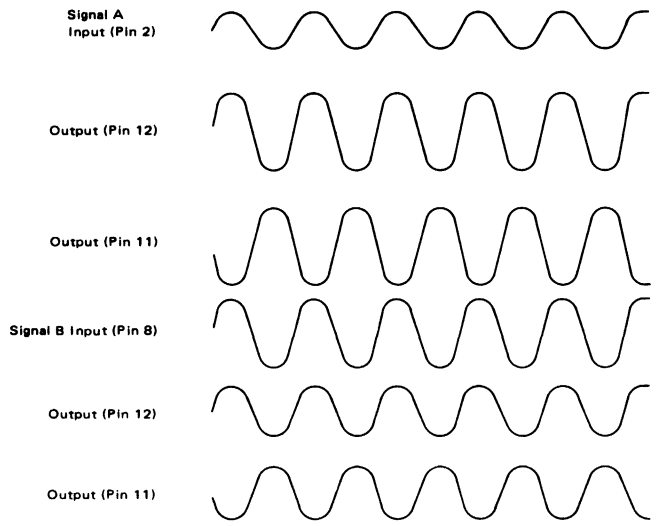
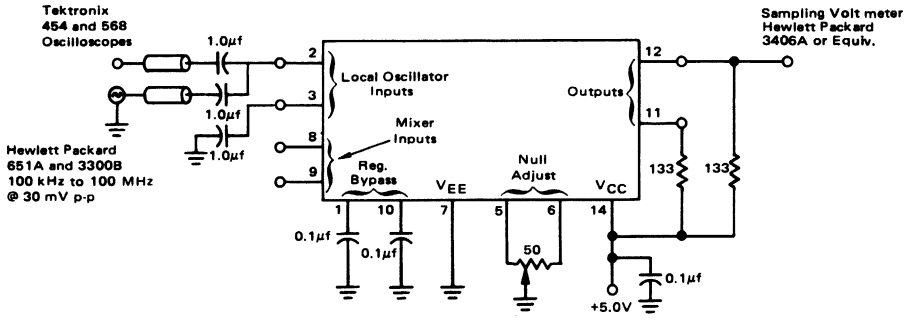


FIGURE 2 — CARRIER FEEDTHROUGH TEST CIRCUITS



Notes:
Test 1—Adjust potentiometer for carrier null at f_c = 100 kHz.
Test 2—Connect pins 5 and 6 to Gnd.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

6

FIGURE 3 — CARRIER FEEDTHROUGH VERSUS FREQUENCY (Test 1)

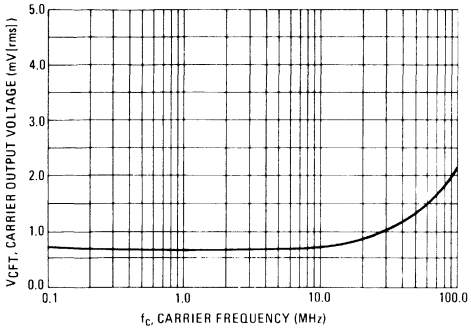


FIGURE 4 — CARRIER FEEDTHROUGH VERSUS FREQUENCY (Test 2)

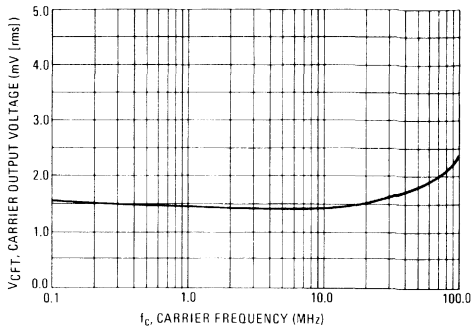
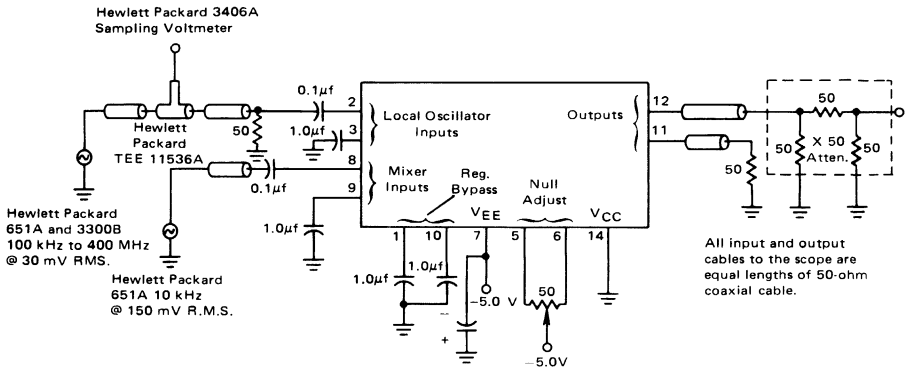


FIGURE 5 — CARRIER SUPPRESSION TEST CIRCUIT



Notes:
Test 1 — Adjust potentiometer for carrier null @ f_c = 100 kHz
Test 2 — Connect pins 5 and 6 to −5.0 volts
Test 3 — Adjust potentiometer for carrier null @ 25°C

6

FIGURE 6 — CARRIER SUPPRESSION VERSUS FREQUENCY (Test 1)

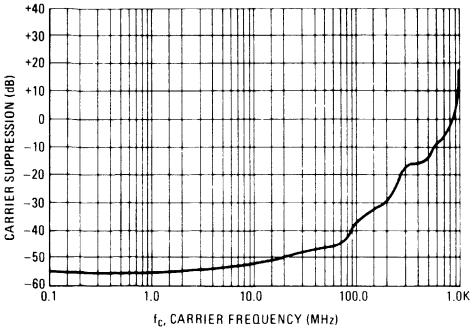


FIGURE 7 — CARRIER SUPPRESSION VERSUS FREQUENCY (Test 2)

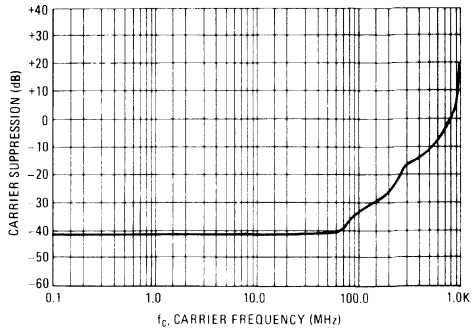


FIGURE 8 — CARRIER SUPPRESSION VERSUS TEMPERATURE

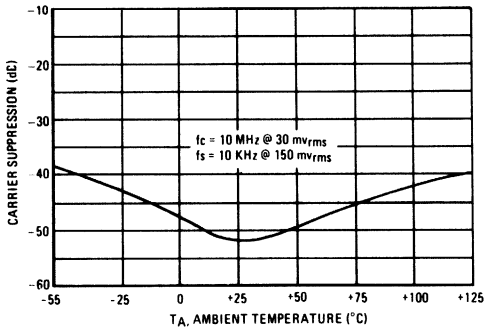
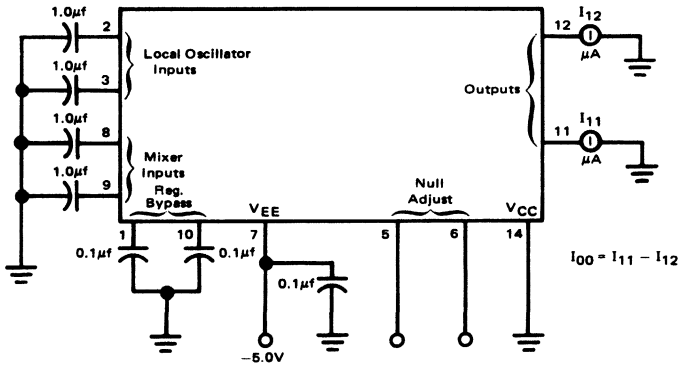


FIGURE 9 — OUTPUT OFFSET CURRENT (I_{OO}) VERSUS TEMPERATURE



Notes:
Test 1 — Pins 5 and 6 left open
Test 2 — Pins 5 and 6 are tied to −5.0 volts

FIGURE 10 — OUTPUT OFFSET CURRENT VERSUS TEMPERATURE

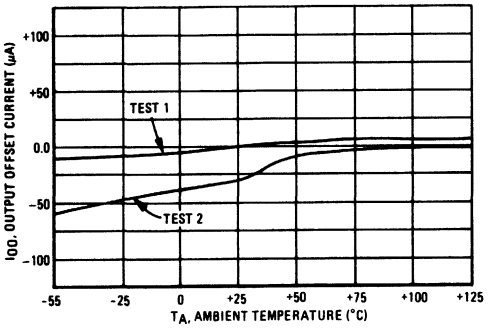
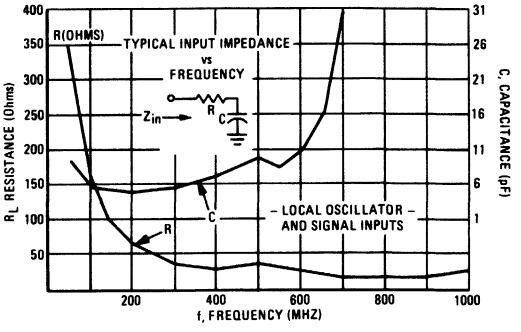


FIGURE 11 — TYPICAL INPUT IMPEDANCE VERSUS FREQUENCY (NO CIRCUIT)



6

MOTOROLA

MC12009
MC12011
MC12013

MECL PLL COMPONENTS

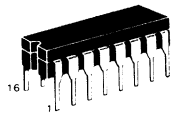
DUAL MODULUS PRESCALER

DUAL MODULUS PRESCALER

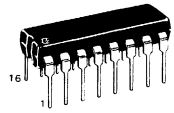
These devices are two-modulus prescalers which will divide by 5 and 6, 8 and 9, and 10 and 11, respectively. A MECL-to-MTTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.

- MC12009 480 MHz (÷ 5/6), MC12011 550 MHz (÷ 8/9), MC12013 550 MHz (÷ 10/11)
- MECL to MTTL Translator on Chip
- MECL and MTTL Enable Inputs
- +5.0 or −5.2 V Operation*
- Buffered Clock Input — Series Input RC Typ, 20 Ohms and 4 pF
- V_{BB} Reference Voltage
- 310 Milliwatts (Typ)

*When using a +5.0 V supply, apply +5.0 V to Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), Pin 16 (V_{CC}), and ground Pin 8 (V_{EE}). When using −5.2 V supply, ground Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), and Pin 16 (V_{CC}) and apply −5.2 V to Pin 8 (V_{EE}). If the translator is not required, Pin 6 may be left open to conserve dc power drain.



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
(Ratings above which device life may be impaired)			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current Continuous Surge	I_O	 <50 <100	mAdc
Storage Temperature Range	T_{stg}	−65 to +175	°C
(Recommended Maximum Ratings above which performance may be degraded)			
Operating Temperature Range MC12009, MC12011, MC12013	T_A	−30 to +85	°C
*DC Fan-Out (Gates and Flip-Flops)	n	70	—

*AC fan-out is limited by desired system performance.

PIN ASSIGNMENT

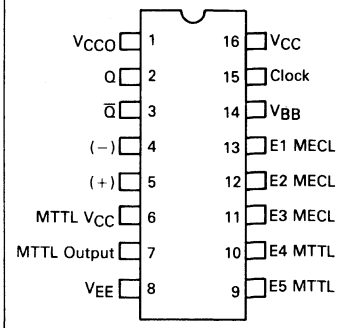


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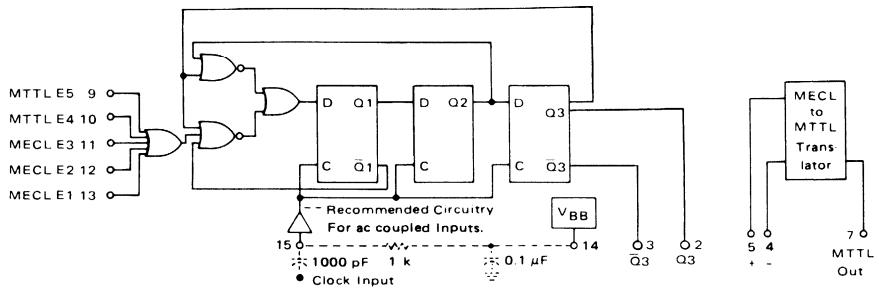
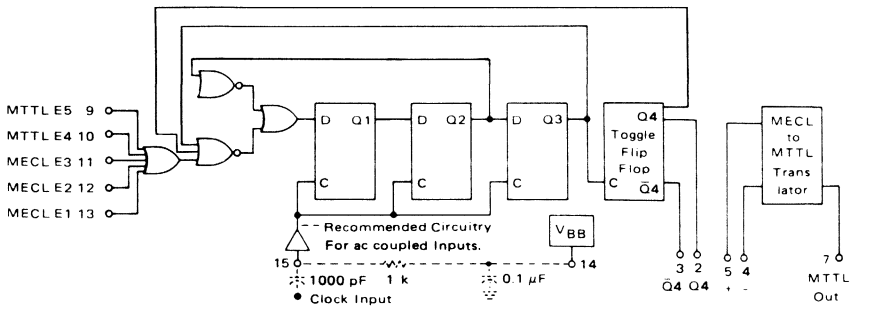
FIGURE 1 – LOGIC DIAGRAMS

MC12009

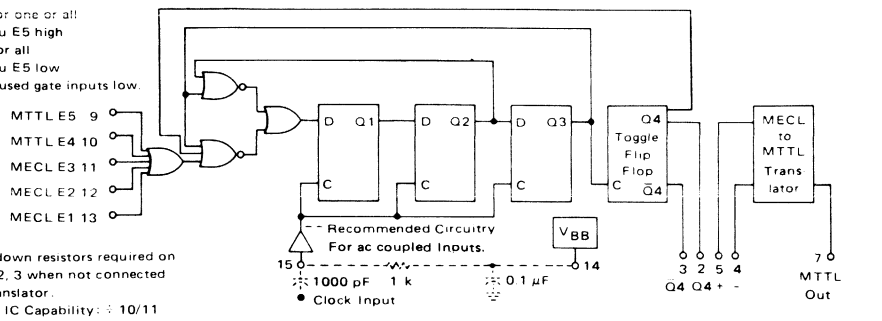


MC12011



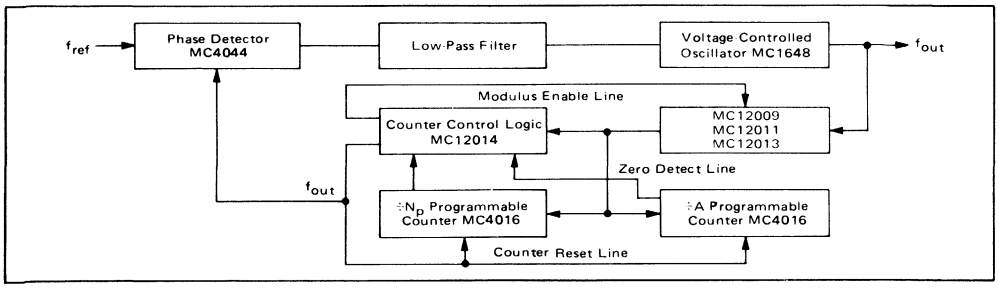
MC12013

÷ 10 for one or all E1 thru E5 high
÷ 11 for all E1 thru E5 low
Tie unused gate inputs low.



Pull-down resistors required on Pins 2, 3 when not connected to translator.
Basic IC Capability: ÷ 10/11

FIGURE 2 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION



6

ELECTRICAL CHARACTERISTICS . . . . . **Supply Voltage −5.2 V**

These devices are designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50-ohm resistor to −2.0 Vdc.

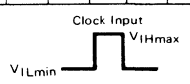
@Test Temperature	TEST VOLTAGE/CURRENT VALUES: Volts V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{EE}	mA I_L	I_{OL}	I_{OH}
−30°C	-0.890	-1.990	-1.205	-1.500	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
+25°C	-0.810	-1.950	-1.105	-1.475	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	0.40
+85°C	-0.700	-1.925	-1.035	-1.440	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40

Characteristic	Symbol	Pin Under Test	MC12009, MC12011, MC12013 −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	Gnd
Power Supply Drain Current	I_{CC1}	8	-88		-80	-	—	-80		mAdc									8				1,16
	I_{CC2}	6		5.2		-	5.2		5.2	mAdc	4	5							8				6
Input Current	I_{INH1}	15		375			250		250	μAdc	15						-		8				1,16
		11		↓			↓		↓	↓	11						9,10		↓				↓
		12									12						9,10						
		13									13						9,10						
	I_{INH2}	4	1.7	6.0	2.0		6.0	2.0	6.4	mAdc	5	4							8				6
		5	1.7	6.0	2.0		6.0	2.0	6.4	mAdc	5	4							8				6
	I_{INH3}	5	0.7	3.0	1.0		3.0	1.0	3.6	mAdc	4	5							8				6
	I_{INH4}	9			100		100		100	μAdc					9				8				1,16
		10			100		100		100	μAdc					10				8				1,16
Leakage Current	I_{INL1}	15	-10		-10			-10		μAdc									8,15				1,16
		11	↓		↓			↓		↓									8,11				↓
		12																	8,12				
		13																	8,13				
	I_{INL2}	9	-1.6		-1.6	-		-1.6		mAdc						9			8				1,16
		10	-1.6		-1.6	-		-1.6		mAdc						10			8				1,16
Reference Voltage	V_{BB}	14			-1.360		-1.160			Vdc									8	-4			1,16
Logic "1" Output Voltage	V_{OH1}	2	-1.100	-0.890	-1.000		-0.810	-0.930	-0.700	Vdc		11,12,13				9,10			8				1,16
①		3	-1.100	-0.890	-1.000		-0.810	-0.930	-0.700	Vdc		11,12,13				9,10			8				1,16
	V_{OH2}	7	-2.8		-2.6			-2.4		Vdc	5	4							8			7	6
Logic "0" Output Voltage	V_{OL1}	2	-1.990	-1.675	-1.950		-1.650	-1.925	-1.615	Vdc		11,12,13				9,10			8				1,16
①		3	-1.990	-1.675	-1.950		-1.650	-1.925	-1.615	Vdc		11,12,13				9,10			8				1,16
	V_{OL2}	7		-4.26			-4.40		-4.48	Vdc	4	5							8		7		6
Logic "1" Threshold Voltage	V_{OHA}	2	-1.120		-1.020			-0.950		Vdc			11,12,13				9,10		8				1,16
②		3	-1.120		-1.020			-0.950		Vdc			11,12,13				9,10		8				1,16
Logic "0" Threshold Voltage	V_{OLA}	2		-1.655			-1.630		-1.595	Vdc				11,12,13				9,10	8				1,16
③		3		-1.655			-1.630		-1.595	Vdc				11,12,13	-			9,10	8				1,16
Short Circuit Current	I_{OS}	7	-65	-20	-65		-20	-65	-20	mAdc	5	4				7	-	-	8	-	-	-	6

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.

② In addition to meeting the output levels specified, the device must divide by 5, 8, or 10 during this test. The clock input is the waveform shown.

③ In addition to meeting the output levels specified, the device must divide by 6, 9, or 11 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS . . . . . Supply Voltage +5.0 V

These devices are designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50-ohm resistor to +3.0 Vdc.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES											
	Volts									mA		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}
-30°C	+4.110	+3.070	+3.795	+3.500	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40
+25°C	+4.190	+3.110	+3.895	+3.525	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40
+85°C	+4.300	+3.135	+3.965	+3.560	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40

Characteristic	Symbol	Pin Under Test	MC12009, MC12011, MC12013 -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	(V_{EE}) Gnd
Power Supply Drain Current	I_{CC1}	8	-88		-80	–	–	-80		mAdc									1,16				8
	I_{CC2}	6		5.2		–	5.2		5.2	mAdc	4	5							6				8
Input Current	I_{INH1}	15		375			250		250	μAdc	15								1,16				8
		11		↓			↓		↓	↓	11					9,10			↓				↓
		12									12					9,10							
		13									13					9,10							
	I_{INH2}	4	1.7	6.0	2.0		6.0	2.0	6.4	mAdc	5	4	–						6				8
		5	1.7	6.0	2.0		6.0	2.0	6.4	mAdc	5	4	–						6				8
	I_{INH3}	5	0.7	3.0	1.0		3.0	1.0	3.6	mAdc	4	5							6				8
	I_{INH4}	9		100			100		100	μAdc					9				1,16				8
		10		100			100		100	μAdc					10				1,16				8
Leakage Current	I_{INL1}	15	-10		10			-10		μAdc									1,16				8,15
		11	↓		↓			↓		↓		–							↓				8,11
		12																					8,12
		13																					8,13
	I_{INL2}	9	-1.6		-1.6			-1.6		mAdc						9			1,16				8
		10	-1.6		-1.6			-1.6		mAdc						10			1,16				8
Reference Voltage	V_{BB}	14			3.67		3.87			Vdc									1,16	14			8
Logic "1" Output Voltage	V_{OH1} ①	2	3.900	4.110	4.000		4.190	4.070	4.300	Vdc		11,12,13				9,10			1,16				8
		3	3.900	4.110	4.000		4.190	4.070	4.300	Vdc		11,12,13				9,10			1,16				8
	V_{OH2}	7	2.4		2.6			2.8		Vdc	5	4							6			7	8
Logic "0" Output Voltage	V_{OL1} ①	2	3.070	3.385	3.110		3.410	3.135	3.445	Vdc		11,12,13				9,10			1,16				8
		3	3.070	3.385	3.110		3.410	3.135	3.445	Vdc		11,12,13				9,10			1,16				8
	V_{OL2}	7		0.94			0.80		0.72	Vdc	4	5							6		7		8
Logic "1" Threshold Voltage	V_{OHA} ②	2	3.880		3.980			4.050		Vdc			11,12,13				9,10		1,16				8
		3	3.880		3.980			4.050		Vdc			11,12,13				9,10		1,16				8
Logic "0" Threshold Voltage	V_{OLA} ③	2		3.405			3.430		3.465	Vdc				11,12,13				9,10	1,16				8
		3		3.405			3.430		3.465	Vdc				11,12,13				9,10	1,16				8
Short Circuit Current	I_{OS}	7	-65	-20	-65		-20	-65	-20	mAdc	5	4				7			6				8

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.

② In addition to meeting the output levels specified, the device must divide by 5, 8, or 10 during this test. The clock input is the waveform shown.

③ In addition to meeting the output levels specified, the device must divide by 6, 9, or 11 during this test. The clock input is the waveform shown.

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC12009, MC12011, MC12013									Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW:							
			-30°C			+25°C			+85°C				Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	V_{IHmin} †	V_{ILmin} †	V_F -3.0 V	V_{EE} -3.0 V	V_{CC} +2.0
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max									
Propagation Delay (See Figures 3 and 5)	t_{15+2+}	2	–	–	8.1	–	–	8.1	–	–	8.9	ns	15	–	–	–	11,12,13	9,10	8	1,6,16
	t_{15+2-}	2	–	–	7.5	–	–	7.5	–	–	8.2	↓	15	–	–	–	11,12,13	9,10	8	1,6,16
	t_{5+7+}	7	–	–	8.4	–	–	8.1	–	–	8.9		A	–	–	–	–	–	8	1,6,16
	t_{5-7-}	7	–	–	6.5	–	–	6.5	–	–	7.1	↓	A	–	–	–	–	–	8	1,6,16
Setup Time (See Figures 4 and 5)	t_{setup1}	11	5.0	–	–	5.0	–	–	5.0		–	ns	15	*	–	–	*	9,10	8	1,6,16
	t_{setup2}	9	5.0	–	–	5.0	–	–	5.0		–	ns	15	–	*	–	11,12,13	*	8	1,6,16
Release Time (See Figures 4 and 5)	t_{rel1}	11	5.0	–	–	5.0	–	–	5.0	–	–	ns	15	*	–	–	*	9,10	8	1,6,16
	t_{rel2}	9	5.0	–	–	5.0	–	–	5.0	–	–	ns	15	–	*	–	11,12,13	*	8	1,6,16
Toggle Frequency (See Figure 6)	f_{max}	2										MHz								
MC12009 5,6			440	–		480	–	–	440	–			–	–		11			8	16
MC12011 8,9			500	–		550	–	–	500	–	–		–	–		11			8	16
MC12013 10,11			500	–		550	–	–	500	–	–		–	–		11	–		8	16

*Test inputs sequentially, with Pulse Generator 2 or 3 as indicated connected to input under test, and the voltage indicated applied to the other input(s) of the same type (i.e., MECL or MTTL).

	-30°C	+25°C	+85°C	
† V_{IHmin}	+1.03	+1.115	+1.20	Vdc
† V_{ILmin}	+0.175	+0.200	+0.235	Vdc

FIGURE 3 – AC VOLTAGE WAVEFORMS

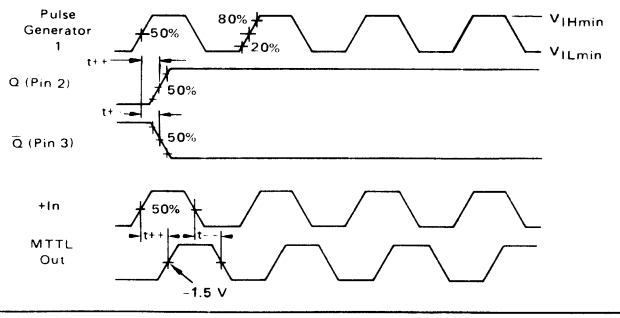


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FIGURE 4 – SETUP AND RELEASE TIME WAVEFORMS

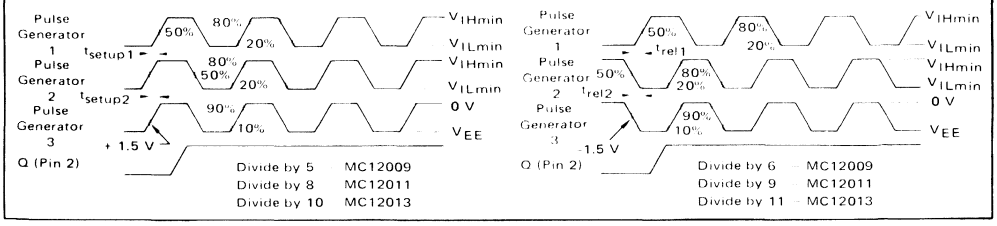
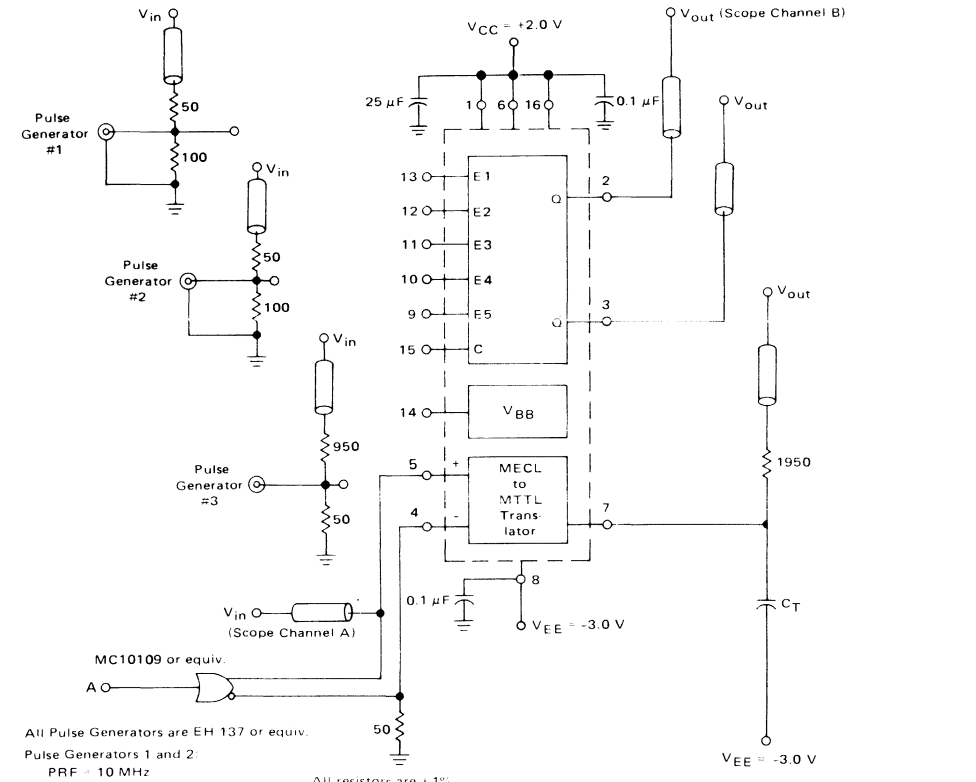
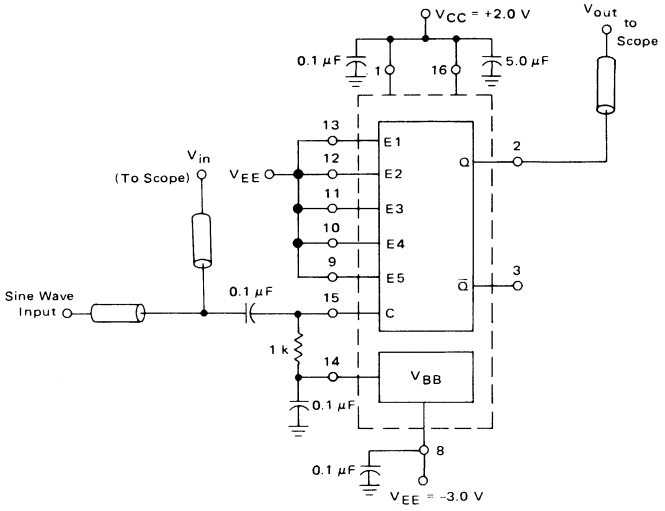


FIGURE 5 – AC TEST CIRCUIT



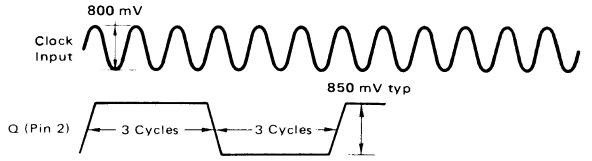
6

FIGURE 6 – MAXIMUM FREQUENCY TEST CIRCUIT

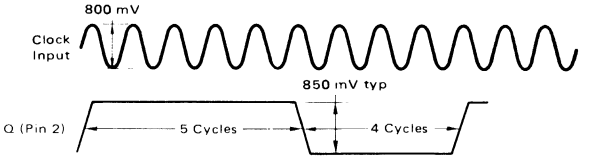


Unused output connected to a 50-ohm resistor to ground

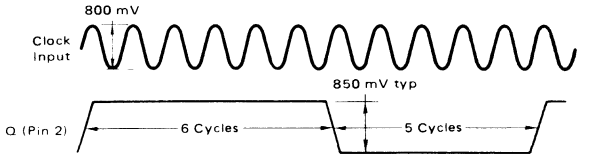
DIVIDE BY 6



DIVIDE BY 9



DIVIDE BY 11



6

FIGURE 7 – STATE DIAGRAM

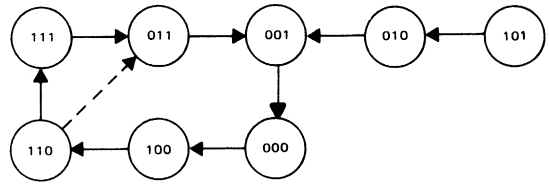
DIVIDE BY 5/6 (MC12009/MC12509)

Q1	Q2	Q3
1	1	1
0	1	1
0	0	1
0	0	0
1	0	0
1	1	0

Enable = 0

Enable = 1

– – – Enable = 1



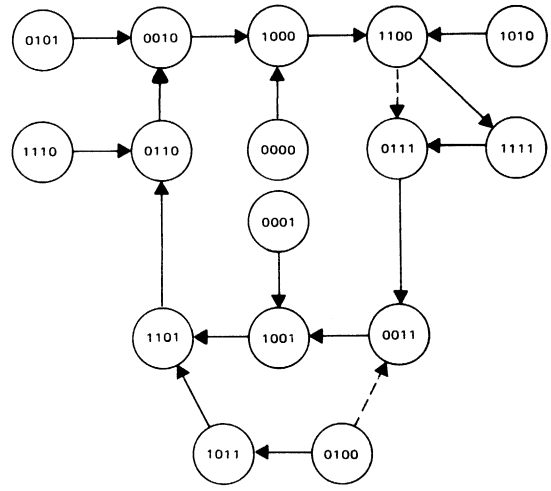
DIVIDE BY 8/9 (MC12011)

Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
1	0	0	0
1	1	0	0

Enable = 0

Enable = 1

– – – Enable = 1

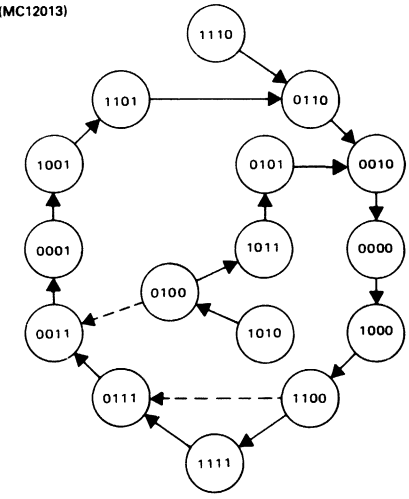


DIVIDE BY 10/11 (MC12013)

Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
0	0	0	0
1	0	0	0
1	1	0	0

Enable = 0

Enable = 1



NOTES:

– – – Enable = 1.

The State of the Enable is important only for the positive Clock Transition when the counter is in state 1100.

6

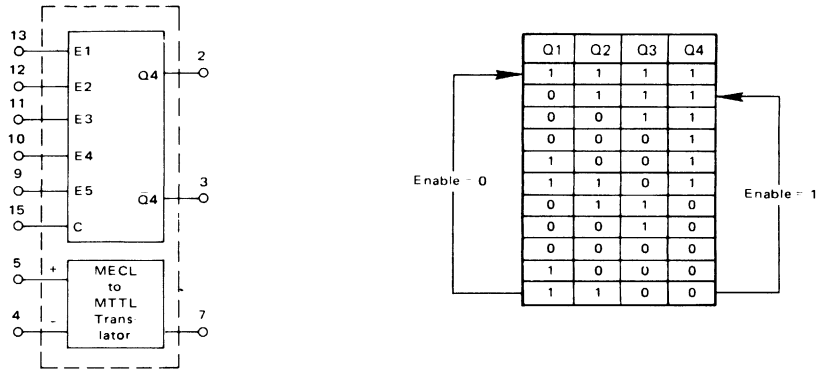
APPLICATIONS INFORMATION

The primary application of these devices is as a high-speed variable modulus prescaler in the divide by N section of a phase-locked loop synthesizer used as the local oscillator of two-way radios. The theory and advantages of variable modulus prescaling, along with typical applications, are covered in Motorola's "Electronic Tuning Address Systems" (SG72).

Proper VHF termination techniques should be followed when the clock is separated from the prescaler by any appreciable distance.

In their basic form, these devices will divide by 5/6, 8/9, or 10/11. Division by 5, 8, or 10 occurs when any one or all of the five gate inputs E1 through E5 are high. Division by 6, 9, or 11 occurs when all inputs E1 through E5 are low. (Unconnected MTTL inputs are normally high, unconnected MECL inputs are normally low). With the addition of extra parts, many different division configurations may be obtained (20/21, 40/41, 50/51, 100/101, etc.) A few of the many configurations are shown below, only for the MC12013.

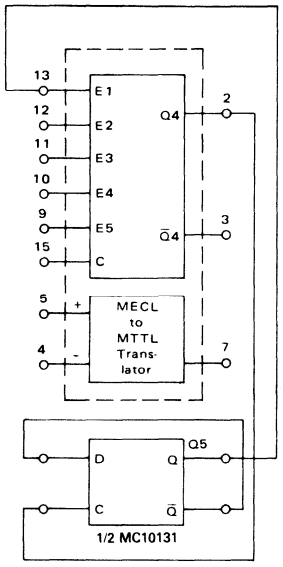
FIGURE 8 — DIVIDE BY 10/11 (MC12013)



Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
0	0	0	0
1	0	0	0
1	1	0	0

6

FIGURE 9 — DIVIDE BY 20/21 (MC12013)



COUNT	Q1	Q2	Q3	Q4	Q4
31	1	1	1	1	1
30	0	1	1	1	1
28	0	0	1	1	1
24	0	0	0	1	1
25	1	0	0	1	1
27	1	1	0	1	1
22	0	1	1	0	1
20	0	0	1	0	1
16	0	0	0	0	1
17	1	0	0	0	1
19	1	1	0	0	1
14	0	1	1	1	0
12	0	0	1	1	0
8	0	0	0	1	0
9	1	0	0	1	0
11	1	1	0	1	0
6	0	1	1	0	0
4	0	0	1	0	0
0	0	0	0	0	0
1	1	0	0	0	0
3	1	1	0	0	0

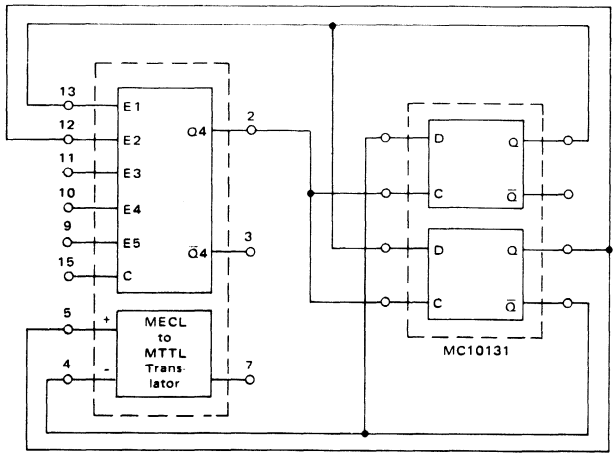
E2 + E3 + E4 + E5 = 0

E2 + E3 + E4 + E5 = 1

To obtain an MTTL output, connect Pins 5 and 4 to Pins 2 and 3 respectively. Termination resistors for the MECL outputs are not shown, but are required except for the flip-flop driving the translator section.

The ÷ 20/21 counter may also be built using an MTTL flip-flop by connecting Pins 5 and 4 to Pins 2 and 3 respectively, and driving the MTTL flip-flop with Pin 7. MC12013 inputs E4 and E5 are used rather than E1. With E1 + E2 + E3 = 0, operation remains as shown.

FIGURE 10 — DIVIDE BY 40/41 (MC12013)



For ÷ 40: E4 + E5 = 1
For ÷ 41: E4 + E5 = 0

Termination resistors for MECL outputs are not shown, but are required except for the flip-flop driving the translator section.

6

MOTOROLA

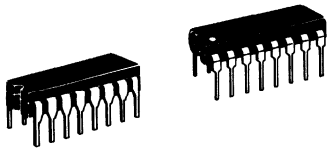
MC12014

COUNTER CONTROL LOGIC

The MC12014 monolithic counter control logic unit is designed for use with the MC12013 Two-Modulus Prescaler and the MC4016 Programmable Counter to accomplish direct high-frequency programming. The MC12014 consists of a zero detector which controls the modulus of the MC12013, and an early decode function which controls the MC4016. The early decode feature also increases the useful frequency range of the MC4016 from 8.0 MHz to 25 MHz.

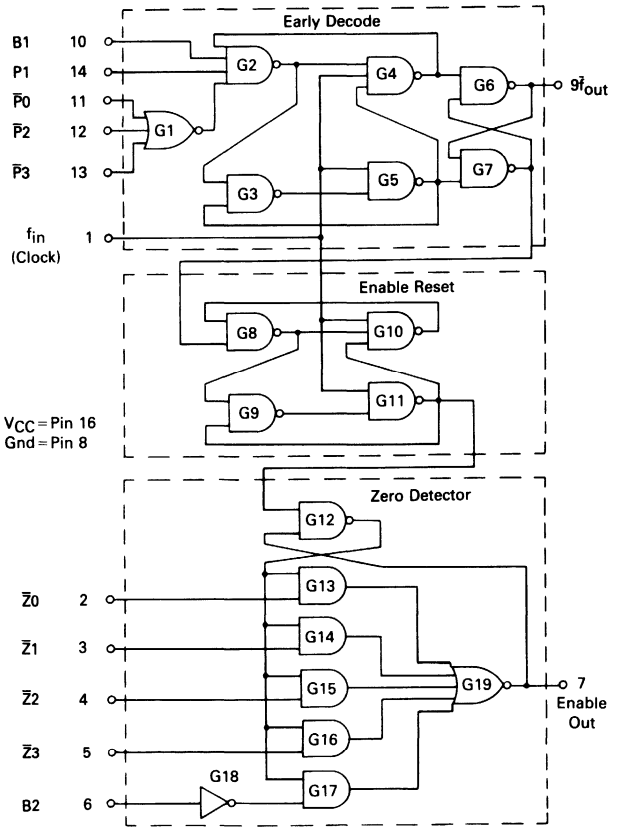
COUNTER CONTROL LOGIC

P SUFFIX
PLASTIC PACKAGE
CASE 648

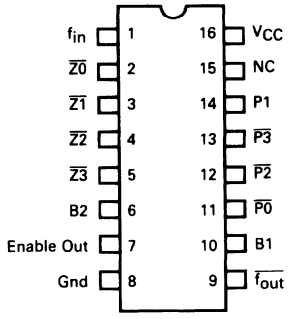


L SUFFIX
CERAMIC PACKAGE
CASE 620

LOGIC DIAGRAM



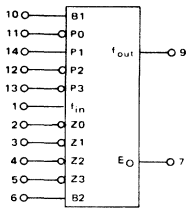
PIN ASSIGNMENT



6

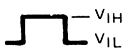
ELECTRICAL CHARACTERISTICS

Test procedures are shown for the f_{in}, $\overline{Z0}$, B1 and P1 inputs. All other inputs are tested in the same manner as the $\overline{Z0}$ input.



			TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
			mA			Volts							
			I_{OL}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	
			16	-1.6	-10	0.5	2.4	5.5	4.5	5.0	4.75	5.25	
Characteristic	Symbol	Pin Under Test	Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																
Forward Current	I_{IL}	1	–	-6.4	mAdc	–	–	–	1	–	–	–	–	–	16	8,10
		2	–	-1.6	↓	–	–	–	2	–	–	–	–	–	↓	8
		10	–	↓	↓	–	–	–	10	–	–	–	–	–		1,8,11,12,13
		14	–			–	–	–	14	–	–	–	–	–		1,8,11,12,13
Leakage Current	I_{IH}	1	–	160	μAdc	–	–	–	–	1	–	–	–	–	16	8,10
		2	–	40	↓	–	–	–	–	2	–	–	–	–	↓	8
		10	–	↓	↓	–	–	–	–	10	–	–	–	–		1,8,11,12,13
		14	–			–	–	–	–	14	–	–	–	–		1,8,11,12,13
	I_{IHH}	1	–	1.0	mAdc	–	–	–	–	–	1	–	–	–	16	8
		2	–	↓	↓	–	–	–	–	–	2	–	–	–	↓	8
		10	–			–	–	–	–	–	10	–	–	–		1,8,11,12,13
		14	–			–	–	–	–	–	14	–	–	–		1,8,11,12,13
Clamp Voltage	V_{IC}	1	–	-1.2	Vdc	–	–	1	–	–	–	–	–	16	–	8
		2	–	↓	↓	–	–	2	–	–	–	–	–	↓	–	↓
		10	–			–	–	10	–	–	–	–	–		–	
		14	–			–	–	14	–	–	–	–	–		–	
Output																
Output Voltage	V_{OL}*	7	–	0.5	Vdc	7	–	–	11,12,13	–	–	2,3,4,5,10,11	–	16	–	8
		9	–	0.5	Vdc	9	–	–	11,12,13	–	–	10,14	–	16	–	8
	V_{OH}	7	2.4	–	Vdc	–	7	–	2,3,4,5	–	–	6	–	16	–	8
		9**	2.4	–	Vdc	–	9	–	–	–	–	11,12,13	–	16	–	8
Short-Circuit Current	I_{OS}	7	-20	-65	Vdc	–	–	–	2,3,4,5	–	–	6	16	–	–	7,8
		9**	-20	-65	Vdc	–	–	–	–	–	–	11,12,13	16	–	–	8,9
Power Requirements																
Power Supply Drain	I_{CC}	16	–	35	mAdc	–	–	–	–	–	–	–	16	–	–	1,8

*Output level to be measured after waveform 1 is applied to f_{in}, pin 1.
**Output level to be measured after waveform 2 is applied to f_{in}, pin 1.

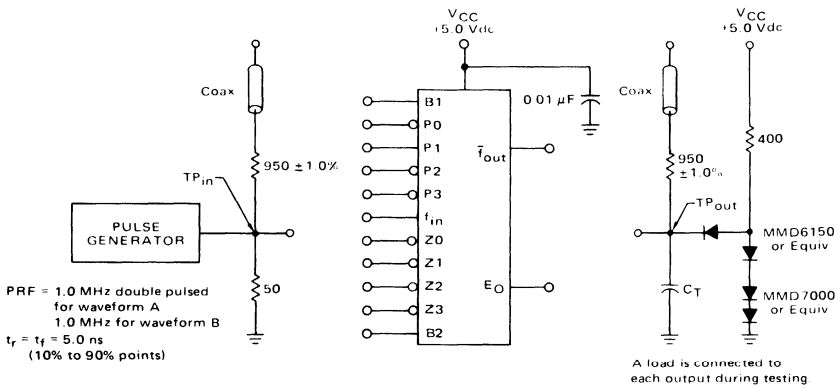
Waveform 1: 

Waveform 2: 

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, waveform letters refer to waveforms on next page.)

Characteristic	Symbol	Pin Under Test		Test Limits (ns)							Pulse Gen. 1		Pulse Gen. 2		Pulse Out		Voltage Applied to Pins Listed Below	
				0°C		+25°C			+75°C									
		In	Out	Min	Max	Min	Typ	Max	Min	Max	Wave-form	Pin	Wave-form	Pin	Wave-form	Pin	V_{IL} = 0.5 V	V_{IH} = 2.4 V
Propagation Delay	t_{PLH1}	1	9	7.0	15	7.0	10	15	7.0	17	A	1	J	10	K	9	11,12,13	14
	t_{PHL1}	1	9	7.0	16	7.0	11	16	7.0	18	A	1	J	10	K	9	11,12,13	14
	t_{PLH2}	2	7	5.0	12	5.0	8.5	12	5.0	14	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
		3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	3	↓	↓	2,4,5,11,12,13	↓
		4												4			2,3,5,11,12,13	
		5												5			2,3,4,11,12,13	
	t_{PHL2}	1	7	7.0	16	7.0	11	16	7.0	18	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
	t_{PLH3}	6	7	7.0	16	7.0	11	16	7.0	18	A	1	J	6	L	7	2,3,4,5,11,12,13	10,14
Setup Time	t_{setup}"1"	10	–	–	–	–	1.0	2.0	–	–	A	1	B	10	G	9	11,12,13	14
		11	–	–	–	–	7.0	12	–	–	↓	↓	↓	11	F	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	1.0	2.0	–	–				14	G		11,12,13	10
	t_{setup}"0"	10	–	–	–	–	4.5	8.0	–	–	A	1	C	10	F	9	11,12,13	14
		11	–	–	–	–	5.0	9.0	–	–	↓	↓	↓	11	G	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	4.5	8.0	–	–				14	F		11,12,13	10
Hold Time	t_{hold}"1"	10	–	–	–	–	4.0	8.0	–	–	A	1	D	10	G	9	11,12,13	14
		11	–	–	–	–	5.0	10	–	–	↓	↓	↓	11	F	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	4.0	8.0	–	–				14	G		11,12,13	10
	t_{hold}"0"	10	–	–	–	–	1.0	2.0	–	–	A	1	E	10	F	9	11,12,13	14
		11	–	–	–	–	7.5	14	–	–	↓	↓	↓	11	G	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	1.0	2.0	–	–				14	F		11,12,13	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

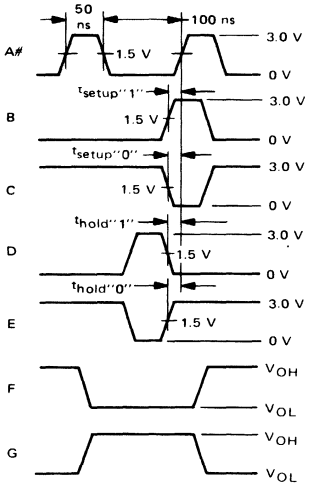


Two pulse generators are required and must be slaved together to provide the waveforms shown.

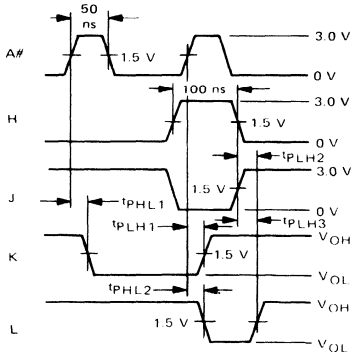
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50 ohm impedance. The 950 ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



#Pulse A (f_{in}) used with all tests.

APPLICATIONS INFORMATION

The MC12014 Counter Control Logic incorporates two features for enhancing operation of the MC4016/4018 Programmable Counters.[1] Maximum operating frequency of the counters is limited by the time required for re-programming at the end of each count-down cycle. Operation can be extended to approximately 25 MHz by using the "early decode" feature included in the MC12014. The appropriate connections are shown in Figure 2. Only three counter stages are shown; however, up to eight stages can be satisfactorily cascaded. Note the following differences between this and the non-extended method: the counter gate inputs are not connected to the input clock; all parallel enables are connected to the $\overline{Q}$ output (f_{out}) of a type D flip-flop formed by gates G2 through G7 in the MC12014 package; the bus terminal of the least significant stage is grounded; all other bus terminals and one internal resistor, R, are connected together and serve as a data input, B1, to the flip-flop. Four additional data inputs, $\overline{P0}$ through $\overline{P3}$, serve to decode the "two" state of the least significant counter stage. Circuit operation is illustrated in waveforms of Figure 2, where the timing for the end of a count-down cycle is shown in expanded form. The counter parallel inputs are assumed to have N = 245 programmed. Timing is not shown for the third stage since it has already been counted down to the all zero state. As the next-to-least significant stage reaches zero, the common bus line goes high. Count down of the least significant stage continues until the "two" state is reached, causing the remaining data inputs to the flip-flop to go high. The next-to-last clock pulse of the cycle then triggers the flip-flop $\overline{Q}$ output low. This takes the parallel enables of all three counter stages low, resetting the programmed data to the outputs. The next input pulse clocks $\overline{Q}$ back to the high state since the data inputs to the flip-flop are no longer all high. The resulting negative output pulse at f_{out} is one input clock period in duration. Note that division by N equal to 001 or 002 is not available using this method.

The frequency synthesizer shown in Figure 8 requires that the programmable counters be quickly stopped after reaching their terminal (zero) count. This can be simply accomplished by taking the master reset of all stages low at the appropriate time. The bus output of the counters could be used for this function since a transition there signals the end of a count-down sequence. However, due to the relatively long delay between the last positive clock transition and the bus transition a faster method is required in this application.

The "zero detection" feature of the MC12014 provides a convenient means of implementing a faster method. Gates G12 through G19 form a latch whose output goes high if B2 is high and low logic levels are applied to the Z0 thru Z3 inputs. When once set to a one by appropriate input conditions, the output of G19 remains high until it is reset by the circuit comprised of gates G8 through G11. Note that since the required information is stored, the counter can be allowed to continue cycling.

The G8-G11 circuit monitors the G7 output of the "early decode" type D flip-flop. When the counter stage connected to the $\overline{P0}$ thru $\overline{P3}$ inputs has counted down to its two state the output of G7 goes high; this enables the G8-G11 circuitry and the next positive clock transition causes the output of G11 to go high, resetting the output of G19 to zero.

FIGURE 1 — TYPICAL FREQUENCY SYNTHESIZER APPLICATION

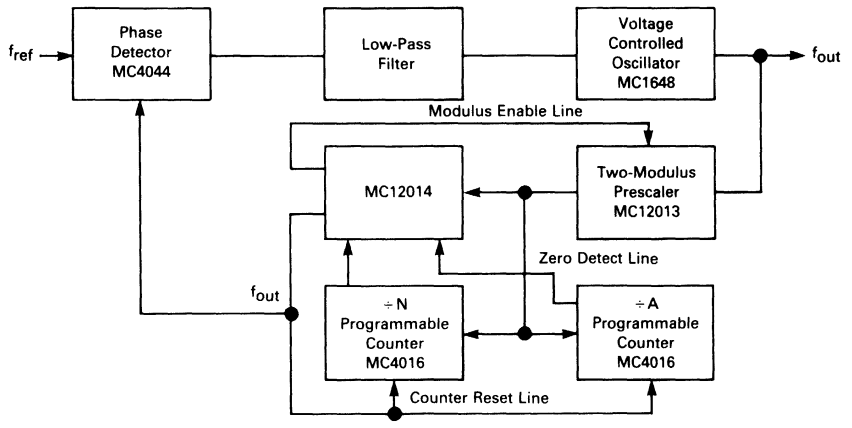


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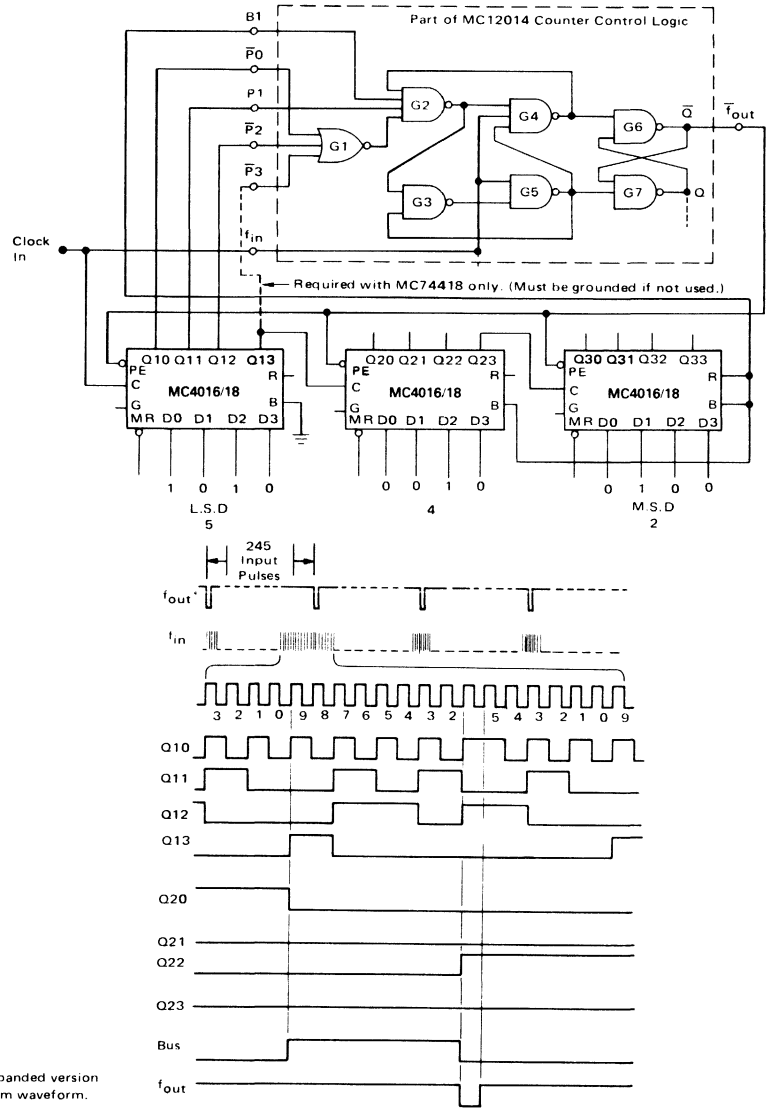
FIGURE 2 — INCREASING THE OPERATING RANGE OF MC74416/74418 PROGRAMMABLE COUNTERS USING MC12014



*Non expanded version of bottom waveform.

1 See the MC54416/54418 data sheet for additional information.

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Operation of the Counter Control Logic can be further clarified by considering a typical system application for programmable counters illustrated in the frequency synthesizer shown in Figure 3. There the counter provides a means of digitally selecting some integral multiple of a stable reference frequency. The circuit phase locks the output, f_{VCO}, of a voltage controlled oscillator to a reference frequency, f_{ref}.[2] Circuit operation is such that $f_{VCO} = Nf_{ref}$, where N is the divider ratio of the feedback counter, permitting frequency selection by means of thumbwheel switches.

In many synthesizer applications the VCO is operated at VHF frequencies too high for direct division by TTL counters. In these cases the VCO output is usually prescaled by using a suitable fixed divide-by-M ECL circuit as shown in Figure 4. For this configuration, $f_{VCO} = NMf_{ref}$, where N is variable (programmable) and M is fixed. Design of the optimum loop filter requires that the input reference frequency be as high as possible where the upper limit is established by the required channel spacing. Since $f_{VCO} = Nf_{ref}$ in the non-prescaled case, if N is changed by one, the VCO output changes by f_{ref}, or the synthesizer channel spacing is just equal to f_{ref}. When the prescaler is used as in Figure 4, $f_{VCO} = NMf_{ref}$, and a change of one in N results in the VCO changing by Mf_{ref}, i.e., if f_{ref} is set equal to the minimum permissible channel spacing as is desirable, then only every M channels in a given band can be selected. One solution is to set f_{ref} = channel spacing/M but this leads to more stringent loop filter requirements.

FIGURE 3 — TTL PHASE-LOCKED LOOP

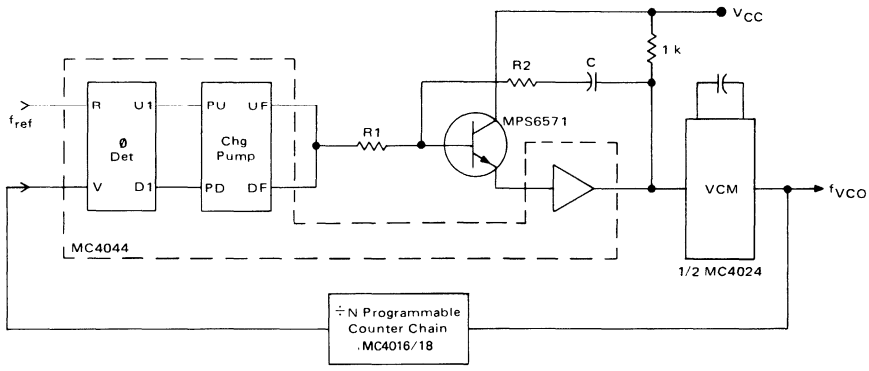
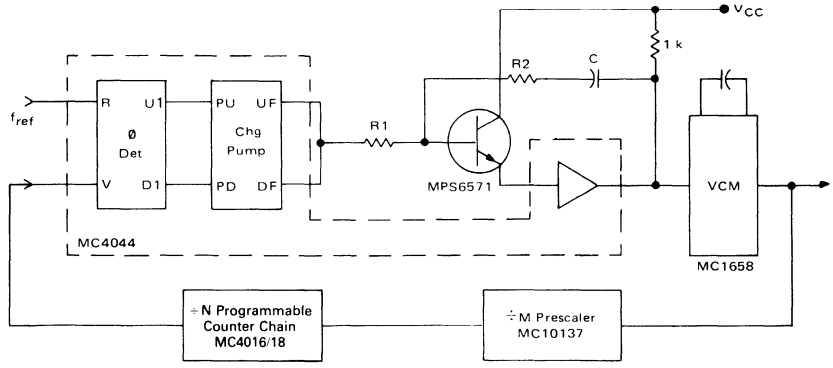


FIGURE 4 — TTL-MECL PHASE-LOCKED LOOP



2 See Motorola Application Notes AN-535, AN-532, and the MC4344/4044 Data Sheet for detailed explanation of over-all circuit operation.

An alternate approach that avoids this problem is provided by the counter configuration shown in Figure 5. It too uses a prescaler ahead of a programmable counter, however the modulus of the prescaler is now controlled by a third counter, causing it to alternate between M and M + 1. Operation is best explained by assuming that all three counters have been set for the beginning of a cycle: the prescaler for division by (M + 1), the modulus control counter for division by N_{mc}, and the programmable counter for division by N_{pc}. The prescaler will divide by (M + 1) until the modulus control counter has counted down to zero; at this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle.

To determine the relationship between f_{out} and f_{in}, let T_1 be the time required for the modulus control counter to reach its terminal count and let T_2 be the remainder of one cycle. That is, T_2 is the time between terminal count in the modulus control counter and terminal count in the programmable counter. When the modulus control counter reaches zero, N_{mc} pulses will have entered it at a rate given by $f_{in}/(M + 1)$ pulses/second or T_2 is:

$$T_1 = \frac{(M + 1)}{f_{in}} \cdot N_{mc} \qquad (1)$$

At this time, N_{mc} pulses have also entered the programmable counter and it will reach its terminal counter after $(N_{pc} - N_{mc})$ more pulses have entered. The rate of entry is now f_{in}/M pulses/second since the prescaler is now dividing by M. From this T_2 is given by:

$$T_2 = \frac{M}{f_{in}} \cdot (N_{pc} - N_{mc}) \qquad (2)$$

Since $f = \frac{1}{T}$:

$$f_{out} = \frac{1}{T_{total}} = \frac{1}{T_1 + T_2} = \frac{1}{\frac{(M+1)N_{mc}}{f_{in}} + \frac{M(N_{pc} - N_{mc})}{f_{in}}} \qquad (3)$$

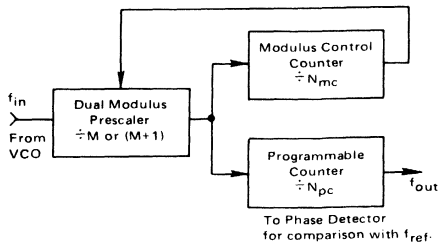
$$f_{out} = \frac{f_{in}}{(M+1)N_{mc} + M(N_{pc} - N_{mc})}$$

$$= \frac{f_{in}}{MN_{mc} + N_{mc} + MN_{pc} - MN_{mc}}$$

$$= \frac{f_{in}}{MN_{pc} + N_{mc}}$$

In terms of the synthesizer application, $f_{VCO} = (MN_{pc} + N_{mc})\, f_{ref}$ and channels can be selected every f_{ref} by letting N_{pc} and N_{mc} take on suitable integer values, including zero.

FIGURE 5 — FEEDBACK COUNTERS WITH DUAL MODULUS PRESCALER



A simplified example of this technique is shown in Figure 6. The MC12013 Dual Modulus Prescaler divides by either 10 or 11 when connected as shown in Figure 6. If the E3 and E4 Enable inputs are high at the start of a prescaler cycle, division by 10 results; if the Enable inputs are low at the beginning of the cycle, division by 11 results. The zero detection circuitry of the MC12014 Counter Control Logic is connected to monitor the outputs of the modulus control counter; this provides a suitable enable signal at E0 as the modulus control counter reaches its terminal (zero) count. The remainder of the MC12014 is connected to extend the operating frequency of the programmable counter chain. Appropriate waveforms for division by 43 are shown in Figure 7a.

The beginning of the timing diagram indicates circuit status just prior to the end of a countdown cycle, i.e., the modulus control counter has been counted down to one and the programmable counter is in the two state. The next positive transition from the prescaler (f1 in the timing diagram) then initiates the following sequence of events. Since the two state of the programmable counter enables the early decode circuitry in the MC12014, the positive f1 transition causes f_{out} to go low. Since f_{out} is connected to the Parallel Enables of all the MC4016 counters this low signal will re-program the counters in readiness for another cycle. However, due to the propagation time through the decode circuitry, the programmable and modulus control counters are briefly decremented to one and zero, respectively, before reprogramming occurs. The momentary zero state of the modulus control counter is detected, setting E_O of the MC12014 high, enabling the MC12013 for division by ten during its next cycle. After eleven more f_{in} pulses (E_O went high after the beginning of the prescaler cycle and so doesn't change the modulus until the next prescaler cycle), f1 again goes high, causing f_{out} to return to the one state. This releases the Parallel Enables and simultaneously resets E_O to zero. However, since E_O was high when the current prescaler cycle began, the next positive f1 transition occurs only ten f_{in} pulses later. Subsequent f1 transitions now decrement the MC4016 counters down through another cycle with the prescaler dividing by eleven. From the waveforms, 11 + 10 + 11 + 11 = 43 input pulses occur for each output pulse.

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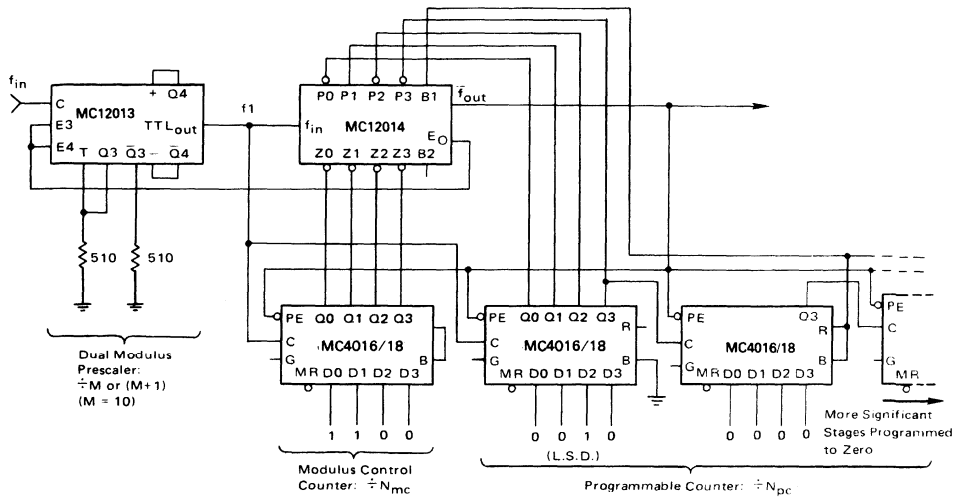
FIGURE 6 — FREQUENCY DIVISION: $f_O = f_{in}/(MN_{pc} + N_{mc})$



Division by 42 is shown in Figure 7b. Operation is similar except that the modulus control counter reaches its terminal count one f1 cycle earlier than before. Since E_O is reset by the trailing edge of the f_{out} pulse, E_O now remains high for two prescaler cycles leading to 10 + 10 + 11 + 11 = 42 input pulses for each output pulse.

Other combinations lead to similar results, however note that N_{pc} must be greater than or equal to N_{mc} for operation as described. If N_{mc} is greater than N_{pc} erroneous results are obtained, however this is not a serious restriction since N_{pc} is greater than N_{mc} in most practical applications.

The synthesizer shown in Figure 8 generates frequencies in the range from 144 to 178 MHz with 30 kHz channel spacing. It uses the dual modulus prescaler approach discussed earlier. General synthesizer design considerations are detailed in the publications listed in footnote 2, hence only the feedback counter is discussed here. Requirements for the feedback divider are determined from:

$$\text{Minimum Divider Ratio} = N_{Tmin} = \frac{144.00\ \text{MHz}}{30\ \text{kHz}} = 4800$$

$$\text{Maximum Divider Ratio} = N_{Tmax} = \frac{177.99\ \text{MHz}}{30\ \text{kHz}} = 5933$$

If the prescaler divides by at least ten, the maximum input frequency to the TTL counters will be 17.799 MHz, allowing use of MC4016 Programmable Counters with the MC12014 frequency extension feature.

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FIGURE 7a — DIVISION BY 43

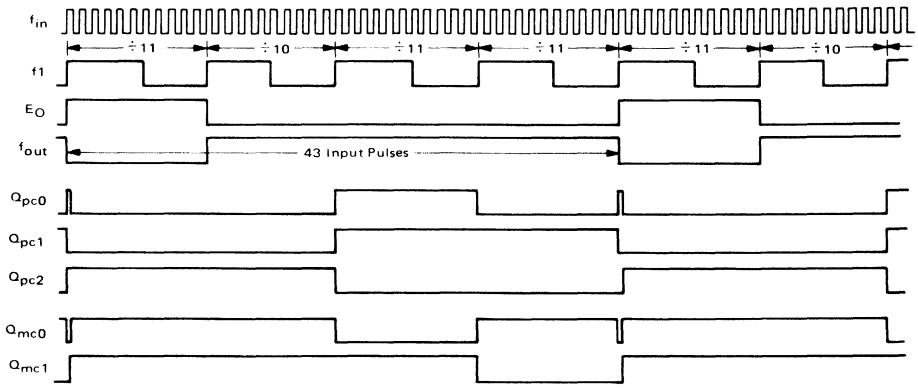
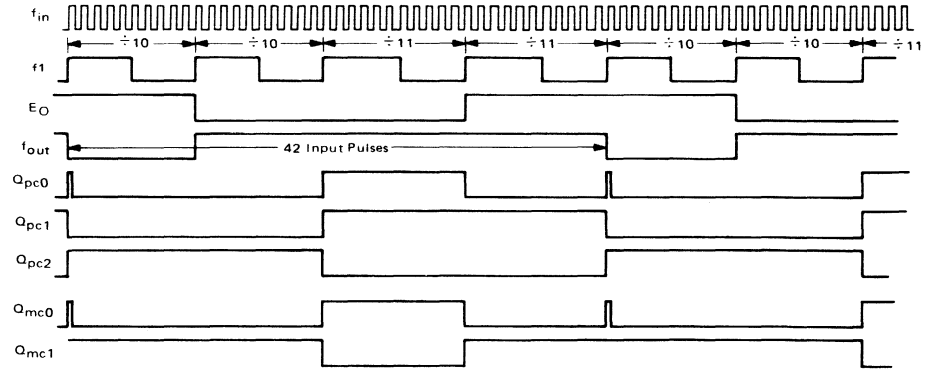


FIGURE 7b — DIVISION BY 42



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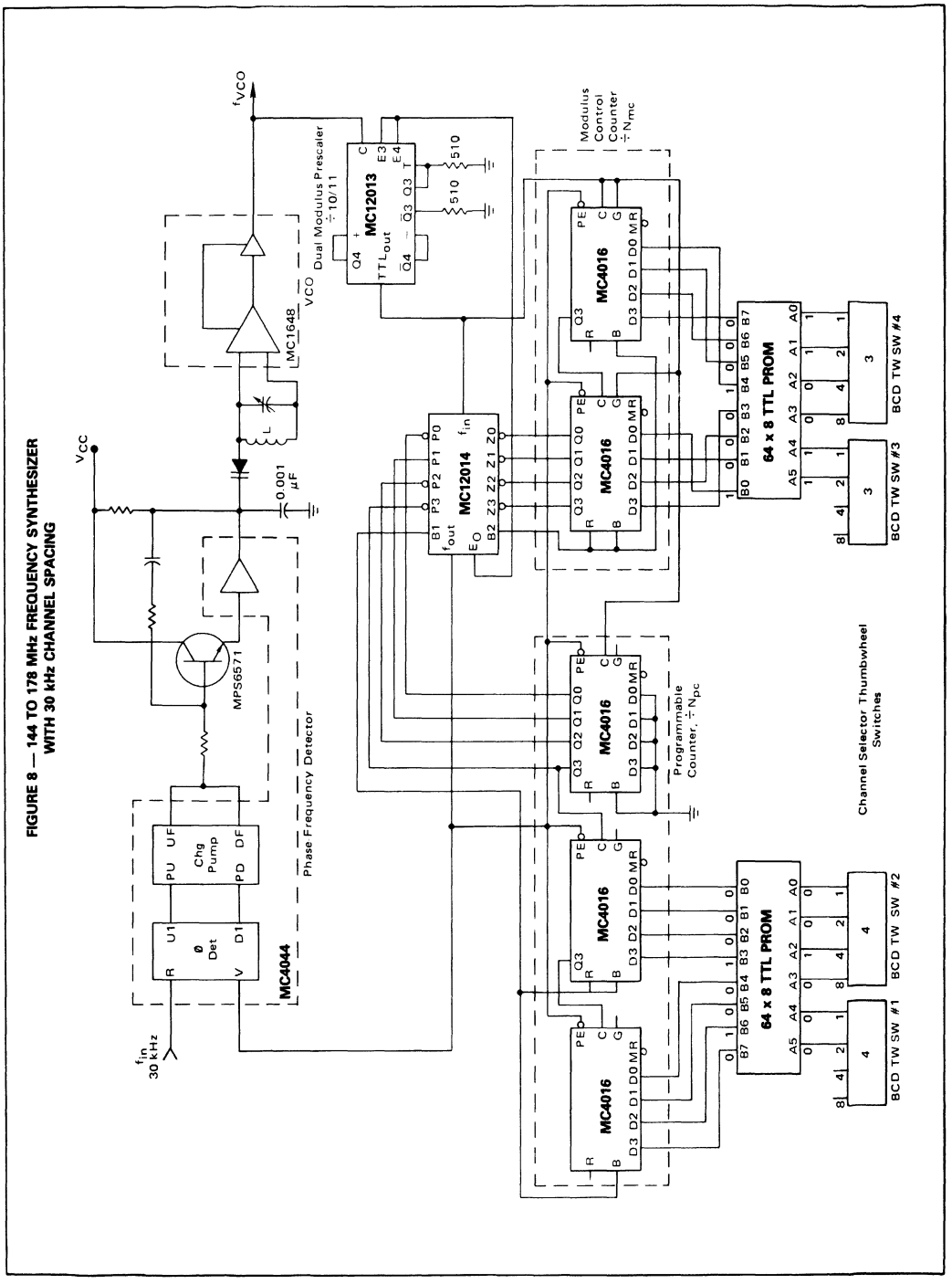

FIGURE 8 — 144 TO 178 MHz FREQUENCY SYNTHESIZER WITH 30 kHz CHANNEL SPACING

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FIGURE 9 — N_{pc} PROM PROGRAMMING

	SW #1	SW #2	SW #1 A5 A4	SW #2 A3 A2 A1 A0	PROM WORD	PROM OUTPUT M.S.B.	PROM OUTPUT L.S.B.	N_{pc}	
(144 MHz)	44		0 1 0 0	0 1 0 0	4	0 1 0 0	1 0 0 0	48	480
	45		0 1 0 0	0 1 0 1	5	0 1 0 0	1 0 0 0	48	
	46		0 1 0 0	0 1 1 0	6	0 1 0 0	1 0 0 0	48	
	47		0 1 0 0	0 1 1 1	7	0 1 0 0	1 0 0 1	49	
	48		0 1 0 0	1 0 0 0	8	0 1 0 0	1 0 0 1	49	
	49		0 1 0 0	1 0 0 1	9	0 1 0 0	1 0 0 1	49	
	50		0 1 0 1	0 0 0 0	16	0 1 0 1	0 0 0 0	50	
	51		0 1 0 1	0 0 0 1	17	0 1 0 1	0 0 0 0	50	
	52		0 1 0 1	0 0 1 0	18	0 1 0 1	0 0 0 0	50	
	53		0 1 0 1	0 0 1 1	19	0 1 0 1	0 0 0 1	51	
	54		0 1 0 1	0 1 0 0	20	0 1 0 1	0 0 0 1	51	
	55		0 1 0 1	0 1 0 1	21	0 1 0 1	0 0 0 1	51	
	56		0 1 0 1	0 1 1 0	22	0 1 0 1	0 0 1 0	52	
	57		0 1 0 1	0 1 1 1	23	0 1 0 1	0 0 1 0	52	
	58		0 1 0 1	1 0 0 0	24	0 1 0 1	0 0 1 0	52	
	59		0 1 0 1	1 0 0 1	25	0 1 0 1	0 0 1 1	53	
	60		0 1 1 0	0 0 0 0	32	0 1 0 1	0 0 1 1	53	
	61		0 1 1 0	0 0 0 1	33	0 1 0 1	0 0 1 1	53	
	62		0 1 1 0	0 0 1 0	34	0 1 0 1	0 1 0 0	54	
	63		0 1 1 0	0 0 1 1	35	0 1 0 1	0 1 0 0	54	
	64		0 1 1 0	0 1 0 0	36	0 1 0 1	0 1 0 0	54	
	65		0 1 1 0	0 1 0 1	37	0 1 0 1	0 1 0 1	55	
	66		0 1 1 0	0 1 1 0	38	0 1 0 1	0 1 0 1	55	
	67		0 1 1 0	0 1 1 1	39	0 1 0 1	0 1 0 1	55	
	68		0 1 1 0	1 0 0 0	40	0 1 0 1	0 1 1 0	56	
	69		0 1 1 0	1 0 0 1	41	0 1 0 1	0 1 1 0	56	
	70		0 1 1 1	0 0 0 0	48	0 1 0 1	0 1 1 0	56	
	71		0 1 1 1	0 0 0 1	49	0 1 0 1	0 1 1 1	57	
	72		0 1 1 1	0 0 1 0	50	0 1 0 1	0 1 1 1	57	
	73		0 1 1 1	0 0 1 1	51	0 1 0 1	0 1 1 1	57	
	74		0 1 1 1	0 1 0 0	52	0 1 0 1	1 0 0 0	58	
	75		0 1 1 1	0 1 0 1	53	0 1 0 1	1 0 0 0	58	
	76		0 1 1 1	0 1 1 0	54	0 1 0 1	1 0 0 0	58	
(177 MHz)	77		0 1 1 1	0 1 1 1	55	0 1 0 1	1 0 0 1	59	590

WORD	BIT 7	6	5	4	3	2	1	0
0	–	–	–	–	–	–	–	–
1	–	–	–	–	–	–	–	–
2	–	–	–	–	–	–	–	–
3	–	–	–	–	–	–	–	–
4	0	1	0	0	1	0	0	0
5	0	1	0	0	1	0	0	0
6	0	1	0	0	1	0	0	0
7	0	1	0	0	1	0	0	1
8	0	1	0	0	1	0	0	1
9	0	1	0	0	1	0	0	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	0	1	0	0	0	0
17	0	1	0	1	0	0	0	0
18	0	1	0	1	0	0	0	0
19	0	1	0	1	0	0	0	1
20	0	1	0	1	0	0	0	1
21	0	1	0	1	0	0	0	1
22	0	1	0	1	0	0	1	0
23	0	1	0	1	0	0	1	0
24	0	1	0	1	0	0	1	0
25	0	1	0	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	1	0	1	0	0	1	1
33	0	1	0	1	0	0	1	1
34	0	1	0	1	0	1	0	0
35	0	1	0	1	0	1	0	0
36	0	1	0	1	0	1	0	0
37	0	1	0	1	0	1	0	1
38	0	1	0	1	0	1	0	1
39	0	1	0	1	0	1	0	1
40	0	1	0	1	0	1	1	0
41	0	1	0	1	0	1	1	0
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	0	1	0	1	0	1	1	0
49	0	1	0	1	0	1	1	1
50	0	1	0	1	0	1	1	1
51	0	1	0	1	0	1	1	1
52	0	1	0	1	1	0	0	0
53	0	1	0	1	1	0	0	0
54	0	1	0	1	1	0	0	0
55	0	1	0	1	1	0	0	1
56	–	–	–	–	–	–	–	–
57	–	–	–	–	–	–	–	–
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

The required divider range, 4800 to 5933, is obtained in the following manner: the MC12013 Dual Modulus Prescaler is connected in the divide by 10/11 mode; the modulus control counter uses two MC4016 stages with N_{mc} ranging from 00 to 99, establishing the two least significant digits of N_T. The remaining two digits of N_T are obtained from a three stage programmable counter generating N_{pc}. The least significant stage of the N_{pc} counter is fixed programmed to zero. The required programming for all remaining stages is derived from four channel selector BCD thumbwheel switches. The relationship between N_T and the counters is given by $N_T = MN_{pc} + N_{mc}$; for a typical channel, say 144.33 MHz, $N_T = 4811$ requires that $M = 10$, $N_{pc} = 480$, and $N_{mc} = 11$, or $N_T = (10)(480) + 11 = 4811$.

A general problem associated with synthesizer design arises from the fact that there is not always a one-to-one correspondence between the code provided by the channel selector switches and the code required for proper programming of the counters. For instance, in the example above where 144.33 MHz was selected, the channel selector switches are set to 44.33 while the required divider ratio is 4811. There are numerous solutions for a given translation requirement, however the method shown here using read only memories offers a straightforward design method. While field programmable read only memories (PROMs) are shown, they would normally be used only during development; suitable fixed ROMs are more economical in production quantities. The design procedure for the code conversion is illustrated in Figure 9. The required programming for the two most

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FIGURE 10 — N_{mc} PROM #1 PROGRAMMING

	SW #3	SW #4	SW #3 A5 A4	SW #4 A3 A2 A1 A0	PROM WORD	PROM OUTPUT M.S.B	PROM OUTPUT L.S.B.	N_{mc}
(144)	.00		0 0	0 0 0 0	0	0 0 0 0	0 0 0 0	00
	.03		0 0	0 0 1 1	3	0 0 0 0	0 0 0 1	01
	.06		0 0	0 1 1 0	6	0 0 0 0	0 0 1 0	02
	.09		0 0	1 0 0 1	9	0 0 0 0	0 0 1 1	03
	.12		0 0	0 0 1 0	18	0 0 0 0	0 1 0 0	04
	.15		0 0	0 1 0 1	21	0 0 0 0	0 1 0 1	05
	.18		0 0	1 0 0 0	24	0 0 0 0	0 1 1 0	06
	.21		0 0	0 0 0 1	33	0 0 0 0	0 1 1 1	07
	.24		0 0	0 1 0 0	36	0 0 0 0	1 0 0 0	08
	.27		0 0	0 1 1 1	39	0 0 0 0	1 0 0 1	09
	.30		0 0	1 0 0 0	48	0 0 0 1	0 0 0 0	10
	.33		0 0	1 0 0 1	51	0 0 0 1	0 0 0 1	11
	.36		0 0	0 1 1 0	54	0 0 0 1	0 0 1 0	12
	.39		0 0	1 1 0 1	57	0 0 0 1	0 0 1 1	13
	.42		0 1	0 0 1 0	2	0 0 0 1	0 1 0 0	14
	.45		0 1	0 0 0 1	5	0 0 0 1	0 1 0 1	15
	.48		0 1	0 0 0 0	8	0 0 0 1	0 1 1 0	16
	.51		0 1	0 0 0 1	17	0 0 0 1	0 1 1 1	17
	.54		0 1	0 1 0 0	20	0 0 0 1	1 0 0 0	18
	.57		0 1	0 1 1 1	23	0 0 0 1	1 0 0 1	19
	.60		0 1	1 0 0 0	32	0 0 1 0	0 0 0 0	20
	.63		0 1	1 0 0 1	35	0 0 1 0	0 0 0 1	21
	.66		0 1	1 0 1 0	38	0 0 1 0	0 0 1 0	22
	.69		0 1	1 0 0 1	41	0 0 1 0	0 0 1 1	23
	.72		0 1	1 1 0 0	49	0 0 1 0	0 1 0 0	24
	.75		0 1	1 1 0 1	53	0 0 1 0	0 1 0 1	25
	.78		0 1	1 1 0 0	56	0 0 1 0	0 1 1 0	26
	.81		1 0	0 0 0 1	1	0 0 1 0	0 1 1 1	27
	.84		1 0	0 0 1 0	4	0 0 1 0	1 0 0 0	28
	.87		1 0	0 0 1 1	7	0 0 1 0	1 0 0 1	29
	.90		1 0	0 1 0 0	16	0 0 1 1	0 0 0 0	30
	.93		1 0	0 1 0 1	19	0 0 1 1	0 0 0 1	31
	.96		1 0	0 1 1 0	22	0 0 1 1	0 0 1 0	32
(144)	.99		1 0	0 1 1 1	25	0 0 1 1	0 0 1 1	33

Use with frequency ranges:

144.00 – 144.99	162.00 – 162.99
147.00 – 147.99	165.00 – 165.99
150.00 – 150.99	168.00 – 168.99
153.00 – 153.99	171.00 – 171.99
156.00 – 156.99	174.00 – 174.99
159.00 – 159.99	177.00 – 177.99

WORD	BIT 7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	1	1
2	0	0	0	1	0	1	0	0
3	0	0	0	0	0	0	0	1
4	0	0	1	0	1	0	0	0
5	0	0	0	1	0	1	0	1
6	0	0	0	0	0	0	1	0
7	0	0	1	0	1	0	0	1
8	0	0	0	1	0	1	1	0
9	0	0	0	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	0	1	1	0	0	0	0
17	0	0	0	1	0	1	1	1
18	0	0	0	0	0	1	0	0
19	0	0	1	1	0	0	0	1
20	0	0	0	1	1	0	0	0
21	0	0	0	0	0	1	0	1
22	0	0	1	1	0	0	1	0
23	0	0	0	1	1	0	0	1
24	0	0	0	0	0	1	1	0
25	0	0	1	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	0	1	0	0	0	0	0
33	0	0	0	0	0	1	1	1
34	–	–	–	–	–	–	–	–
35	0	0	1	0	0	0	0	1
36	0	0	0	0	1	0	0	0
37	–	–	–	–	–	–	–	–
38	0	0	1	0	0	0	1	0
39	0	0	0	0	1	0	0	1
40	–	–	–	–	–	–	–	–
41	0	0	1	0	0	0	1	1
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	0	0	0	1	0	0	0	0
49	0	0	1	0	0	1	0	0
50	–	–	–	–	–	–	–	–
51	0	0	0	1	0	0	0	1
52	–	–	–	–	–	–	–	–
53	0	0	1	0	0	1	0	1
54	0	0	0	1	0	0	1	0
55	–	–	–	–	–	–	–	–
56	0	0	1	0	0	1	1	0
57	0	0	0	1	0	0	1	1
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

significant digits of N_{pc} is shown versus the code provided by switches #1 and #2 of the channel selector. If the four outputs of switch #2 and the two least significant outputs of switch #1 are regarded as address bits A0 through A5 for a 64 x 8 TTL PROM, a memory location can be associated with each switch setting. The required N_{pc} programming for each switch setting is then set into the appropriate memory location by the user. In Figure 9, the required programming has been transferred into a truth table to be used while programming the PROM. A similar result for the N_{mc} programming is shown in Figure 10. Note that the PROM shown, N_{mc} PROM #1, selects only N_{mc} numbers 00 through 33. This means that the synthesizer as shown in Figure 8 selects only the adjacent channels in a one megahertz slice of the total band. The frequency ranges that can be selected using N_{mc} PROM #1 are summarized in Figure 10. For other ranges, N_{mc} PROM #1 must be replaced by one of two additional PROMs required for generating the remaining N_{mc} numbers. Appropriate truth tables along with the ranges they can be used with are shown in Figures 11 and 12.

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FIGURE 11 – N_{mc} PROM #2 TRUTH TABLE

WORD	BIT 7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	0	0
1	0	1	0	0	0	1	1	1
2	0	0	1	1	0	1	0	0
3	0	1	1	0	0	0	0	1
4	0	1	0	0	1	0	0	0
5	0	0	1	1	0	1	0	1
6	0	1	1	0	0	0	1	0
7	0	1	0	0	1	0	0	1
8	0	0	1	1	0	1	1	0
9	0	1	1	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	0	1	0	0	0	0
17	0	0	1	1	0	1	1	1
18	0	1	1	0	0	1	0	0
19	0	1	0	1	0	0	0	1
20	0	0	1	1	1	0	0	0
21	0	1	1	0	0	1	0	1
22	0	1	0	1	0	0	1	0
23	0	0	1	1	1	0	0	1
24	0	1	1	0	0	1	1	0
25	0	1	0	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	1	0	0	0	0	0	0
33	–	–	–	–	–	–	–	–
34	0	1	0	1	0	1	0	0
35	0	1	0	0	0	0	0	1
36	–	–	–	–	–	–	–	–
37	0	1	0	1	0	1	0	1
38	0	1	0	0	0	0	1	0
39	–	–	–	–	–	–	–	–
40	0	1	0	1	0	1	1	0
41	0	1	0	0	0	0	1	1
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	–	–	–	–	–	–	–	–
49	0	1	0	1	0	1	1	1
50	0	1	0	0	0	1	0	0
51	–	–	–	–	–	–	–	–
52	0	1	0	1	1	0	0	0
53	0	1	0	0	0	1	0	1
54	–	–	–	–	–	–	–	–
55	0	1	0	1	1	0	0	1
56	0	1	0	0	0	1	1	0
57	–	–	–	–	–	–	–	–
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

Use with frequency ranges:

145.02 – 145.98
148.02 – 148.98
151.02 – 151.98
154.02 – 154.98
157.02 – 157.98
160.02 – 160.98
163.02 – 163.98
166.02 – 166.98
169.02 – 169.98
172.02 – 172.98
175.02 – 175.98

FIGURE 12 – N_{mc} PROM #3 TRUTH TABLE

WORD	BIT 7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0	0
1	0	1	1	0	0	1	1	1
2	1	0	0	1	0	1	0	0
3	1	0	0	0	0	0	0	1
4	0	1	1	0	1	0	0	0
5	1	0	0	1	0	1	0	1
6	1	0	0	0	0	0	1	0
7	0	1	1	0	1	0	0	1
8	1	0	0	1	0	1	1	0
9	1	0	0	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	1	1	0	0	0	0
17	1	0	0	1	0	1	1	1
18	1	0	0	0	0	1	0	0
19	0	1	1	1	0	0	0	1
20	1	0	0	1	1	0	0	0
21	1	0	0	0	0	1	0	1
22	0	1	1	1	0	0	1	0
23	1	0	0	1	1	0	0	1
24	1	0	0	0	0	1	1	0
25	0	1	1	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	–	–	–	–	–	–	–	–
33	1	0	0	0	0	1	1	1
34	0	1	1	1	0	1	0	0
35	–	–	–	–	–	–	–	–
36	–	–	–	–	–	–	–	–
37	0	1	1	1	0	1	0	1
38	1	0	0	0	1	0	0	0
39	1	0	0	0	1	0	0	1
40	0	1	1	1	0	1	1	0
41	–	–	–	–	–	–	–	–
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	1	0	0	1	0	0	0	0
49	0	1	1	1	0	1	1	1
50	–	–	–	–	–	–	–	–
51	1	0	0	1	0	0	0	1
52	0	1	1	1	1	0	0	0
53	–	–	–	–	–	–	–	–
54	1	0	0	1	0	0	1	0
55	0	1	1	1	1	0	0	1
56	–	–	–	–	–	–	–	–
57	1	0	0	0	0	0	1	1
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

Use with frequency ranges:

146.01 – 146.97
149.01 – 149.97
152.01 – 152.97
155.01 – 155.97
158.01 – 158.97
161.01 – 161.97
164.01 – 164.97
167.01 – 167.97
170.01 – 170.97
173.01 – 173.97
176.01 – 176.97

6

MOTOROLA

MC12015
MC12016
MC12017

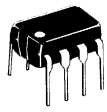
MECL PLL COMPONENTS

225 MHz DUAL MODULUS PRESCALER

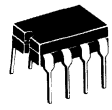
225 MHz DUAL MODULUS PRESCALER

The MC12015, MC12016 and MC12017 are two-modulus prescalers which will divide by 32 and 33, 40 and 41, and 64 and 65 respectively. An internal regulator is provided to allow these devices to be used over a wide range of power-supply voltages. The devices may be operated by applying a supply voltage of 5.0 Vdc ±10% at pin 7 or by applying an unregulated voltage source from 5.5 Vdc to 9.5 Vdc to pin 8.

- 225 MHz Toggle Frequency
- Low-Power — 7.5 mA Max at 6.8 V
- Control Input and Output are Compatible with Standard CMOS
- Connecting Pins 2 and 3 Allows Driving One TTL Load
- Supply Voltage 4.5 V to 9.5 V



P SUFFIX
PLASTIC PACKAGE
CASE 626



L SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Regulated Voltage, Pin 7	V_{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	V_{CC}	10.0	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

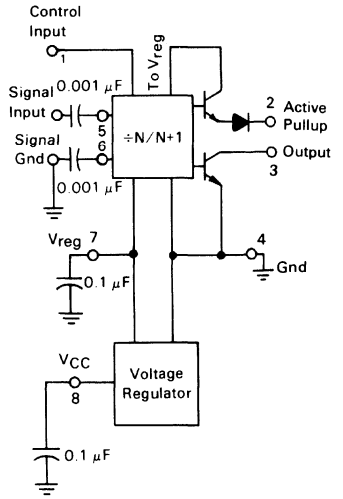
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.5 to 9.5, V_{reg} = 4.5 to 5.5 V, T_A = -40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine wave input)	f_{max}	225	—	—	MHz
	f_{min}	—	—	35	MHz
Supply Current	I_{CC}	—	6.0	7.8	mA
Control Input High (÷32, 40 or 64)		2.0	—	—	V
Control Input Low (÷33, 41 or 65)		—	—	0.8	V
Output Voltage High* (I_{source} = 50 μA)	V_{OH}	2.5	—	—	V
Output Voltage Low* (I_{sink} = 2 mA)	V_{OL}	—	—	0.5	V
Input Voltage Sensitivity 35 MHz	V_{in}	400	—	800	mVPP
50-225 MHz		200	—	800	
PLL Response Time (Notes 1 and 2)	t_{PLL}	—	—	t_{out} -70	ns

Notes:
1. t_{PLL} = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform.

*Pin 2 connected to Pin 3

PRESCALER BLOCK DIAGRAM



1. V_{reg} @ pin 7 is not guaranteed to be between 4.5 and 5.5 V when Vcc is being applied to pin 8.
2. Pin 7 is not to be used as a source of regulated output voltage.

6

MOTOROLA

MC12018

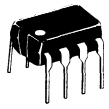
MECL PLL COMPONENTS

520 MHz ÷128/129 DUAL MODULUS PRESCALER

520 MHz DUAL MODULUS PRESCALER

The MC12018 is a two-modulus prescaler which divides by 128 and 129. An internal regulator is provided to allow this device to be used over a wide range of power-supply voltages. The devices may be operated by applying a supply voltage of 5.0 Vdc ±10% at pin 7 or by applying an unregulated voltage source from 5.5 Vdc to 9.5 Vdc to pin 8.

- 520 MHz Toggle Frequency
- Low-Power — 8.0 mA Typical
- Control Input Is Compatible with Standard CMOS and TTL
- Supply Voltage 4.5 V to 9.5 V



P SUFFIX
PLASTIC PACKAGE
CASE 626

L SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

MAXIMUM RATINGS

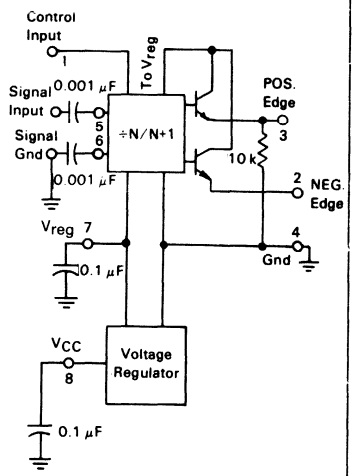
Characteristic	Symbol	Range	Unit
Regulated Voltage, Pin 7	V_{reg}	8.0	Vdc
Power Supply Voltage, Pin 8	V_{CC}	10.0	Vdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.5 to 9.5, V_{reg} = 4.5 to 5.5 V, T_A = −40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_{max} f_{min}	520 —	— —	— 75	MHz MHz
Supply Current (Pin 8)	I_{CC}	—	8.0	10.2	mA
Control Input High (÷ 128)	V_{IH}	2.0	—	—	V
Control Input Low (÷ 129)	V_{IL}	—	—	0.8	V
Differential Output Voltage (I_{sink} = 200 μA)	V_{out}	0.8	1.0	—	V
PLL Response Time (Notes 1 and 2)	t_{PLL}	—	—	t_{out} -50	ns
Input Voltage Sensitivity 75 MHz 125–520 MHz	V_{in}	 400 200	 — —	 800 800	mVpp

Notes:
1. t_{PLL} = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform

PRESCALER BLOCK DIAGRAM



1. V_{reg} @ pin 7 is not guaranteed to be between 4.5 and 5.5 V when V_{CC} is being applied to pin 8.
2. Pin 7 is not to be used as a source of regulated output voltage.
3. 10KΩ pulldown recommended with negative edge output. (pin 2).

6

MOTOROLA

MC12019

225 MHz DUAL MODULUS PRESCALER

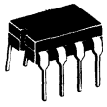
The MC12019 is a divide by 20 and 21 two-modulus prescaler. It will divide by 20 when the modulus control input is high and by 21 when the modulus control input is low.

- 225 MHz Toggle Frequency
- Low-Power—7.5 mA Max at 5.5 V
- Control Input Compatible with Standard Motorola CMOS Synthesizers
- Emitter Follower Outputs

MECL PLL COMPONENTS

225 MHz ÷20/21 DUAL MODULUS PRESCALER

P SUFFIX
PLASTIC PACKAGE
CASE 626



L SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

MAXIMUM RATINGS

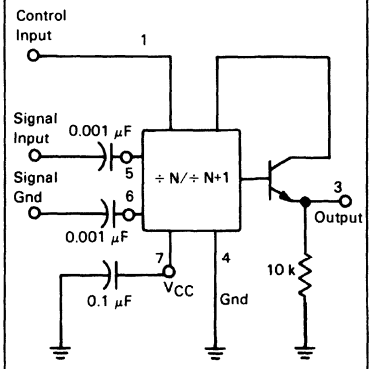
Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 7	V_{CC}	8.0	Vdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = −40° to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_{max} f_{min}	225 —	— —	— 20	MHz MHz
Supply Current	I_{CC}	—	—	7.5	mA
Control Input High (÷20)	V_{IH}	2.0	—	—	V
Control Input Low (÷21)	V_{IL}	—	—	0.8	V
Output Voltage Swing	V_{out}	600	—	1200	mV_{pp}
Input Voltage Sensitivity 20–225 MHz	V_{in}	200	—	800	mV_{pp}
PLL Response Time (Notes 1 and 2)	t_{PLL}	—	—	$t_{out}-70$	ns

Notes:
1. t_{PLL} = the time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
2. t_{out} = period of output waveform.

PRESCALER BLOCK DIAGRAM



6

MOTOROLA

MC12022A/ MC12022B

1.1 GHz DUAL MODULUS PRESCALER

The MC12022A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

The MC12022B can be used with CMOS synthesizers requiring negative edges to trigger internal counters such as Fujitsu's MB87001.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

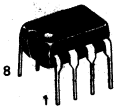
The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5 V
- Low Power 7.5 mA Typical
- Operating Temperature Range of −40°C to +85°C
- Short Setup Time (t_{set}) 16 ns Maximum @ 1.1 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL. Maximum Input Voltage Should be Limited to 6.5 Vdc.

MECL PLL COMPONENTS

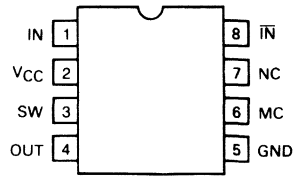
1.1 GHz ÷64/65, ÷128/129 DUAL MODULUS PRESCALER

P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

PRESCALER PIN ASSIGNMENT



(Top View)

Note 1:
For positive edge triggered synthesizers, order the MC12022A.
For negative edge triggered synthesizers, order the MC12022B.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	−0.5 to +7.0	Vdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Modulus Control Input, Pin 6	MC	−0.5 to +6.5	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = −40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.6	1.1	GHz
Supply Current Output Unloaded (Pin 2)	I_{CC}	—	7.5	10	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	—	—	V
Modulus Control Input Low (MC)	V_{IL1}	—	—	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	OPEN	OPEN	OPEN	—
Output Voltage Swing (C_L = 12 pF, R_L = 2.2 kΩ)	V_{out}	1.0	1.6	—	V_{p-p}
Modulus Setup Time MC to Out	t_{SET}	—	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	V_{in}	100 400	— —	1500 1500	mVpp
Output Current C_L = 12 pF, R_L = 2.2 kΩ	I_O	—	—	2.0	mA

FUNCTION TABLE		
SW	**MC**	**Divide Ratio**
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC}
L = Gnd to 0.8 V

6

LOGIC DIAGRAM (MC12022A)

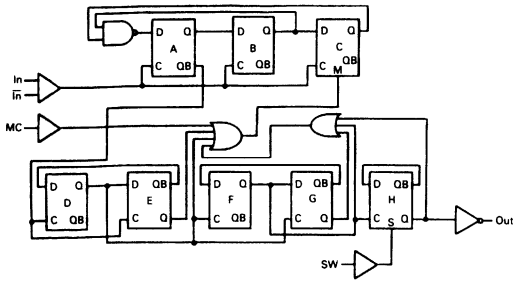
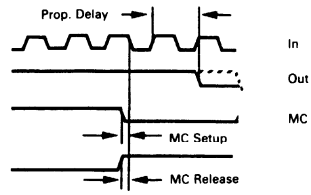


FIGURE 1 — MODULUS SETUP TIME



Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

FIGURE 2 — TYPICAL OUTPUT WAVEFORMS

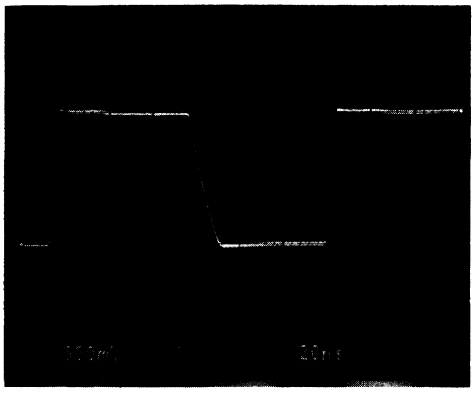


FIGURE 2A — ÷64, 500 MHz, 5.0 V, +25°C, OUTPUT LOADED

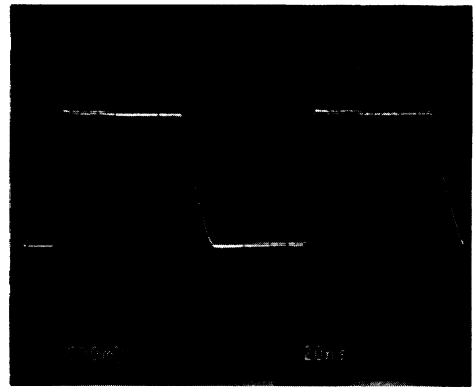
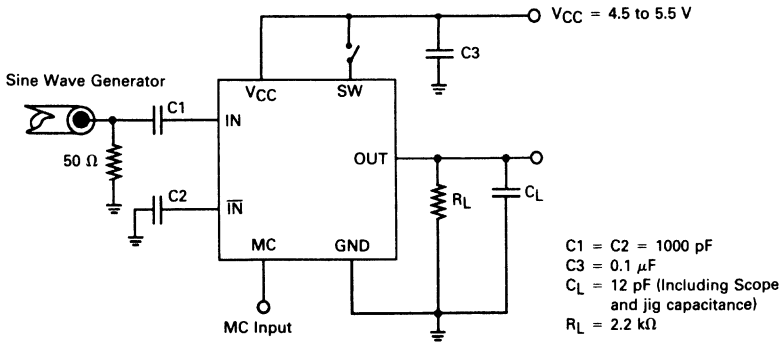


FIGURE 2B — ÷128, 1.1 GHz, 5.0 V, +25°C, OUTPUT LOADED

FIGURE 3 — AC TEST CIRCUIT



C1 = C2 = 1000 pF
C3 = 0.1 μF
C_L = 12 pF (Including Scope and jig capacitance)
R_L = 2.2 kΩ

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FIGURE 4 — MC12022 TYPICAL CHARACTERISTIC CURVES

FIGURE 4A — INPUT SIGNAL AMPLITUDE versus INPUT FREQUENCY. DIVIDE RATIO = 128

FIGURE 4B — OUTPUT AMPILTUDE versus INPUT FREQUENCY

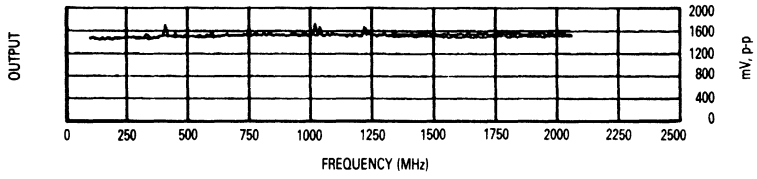
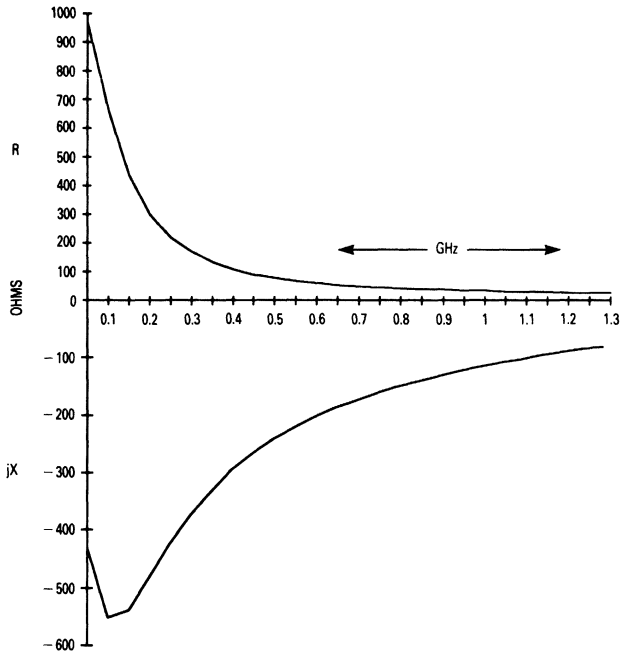


FIGURE 4C — TYPICAL INPUT IMPEDANCE versus INPUT FREQUENCY



6

MOTOROLA

MC12022LVA
MC12022LVB

1.1 GHz LOW VOLTAGE DUAL MODULUS PRESCALER

The MC12022LVA can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

The MC12022LVB can be used with CMOS synthesizers requiring negative edges to trigger internal counters such as Fujitsu's MB87001.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 2.7 to 5.0 V
- Low Power 4.0 mA Typical @ V_{CC} = 2.7 V
- Operating Temperature Range of −40°C to +85°C
- Short Setup Time (t_{set}) 16 ns Maximum @ 1.1 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL

Design Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

*Equivalent to a two-input NAND gate.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	−0.5 to +7.0	Vdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Modulus Control Input, Pin 6	MC	−0.5 to +6.5	Vdc

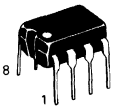
ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.0 V, T_A = −40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current Output Unloaded (Pin 2) @ 2.7 Vdc	I_{CCL}	—	4.0	6.5	mA
Supply Current Output Unloaded (Pin 2) @ 5.0 Vdc	I_{CCH}	—	5.8	8.0	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	—	—	V
Modulus Control Input Low (MC)	V_{IL1}	—	—	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	OPEN	OPEN	OPEN	—
Output Voltage Swing (C_L = 12 pF, R_L = 1.1 kΩ @ 2.7 Vdc)	V_{out}	0.8	1.0	—	V_{p-p}
Output Voltage Swing (C_L = 12 pF, R_L = 2.2 kΩ @ 5.0 Vdc)	V_{out}	1.0	1.6	—	V_{p-p}
Modulus Setup Time MC to Out	t_{SET}	—	11	16	ns
Input Voltage Sensitivity @ 250–1100 MHz 100–250 MHz	V_{in} Min	100 400	— —	1500 1500	mVpp
Output Current C_L = 12 pF, R_L = 2.2 kΩ	I_O	—	—	2.0	mA

MECL PLL COMPONENTS

1.1 GHz ÷64/65, ÷128/129
LOW VOLTAGE
DUAL MODULUS

P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
SOIC PACKAGE
CASE 751

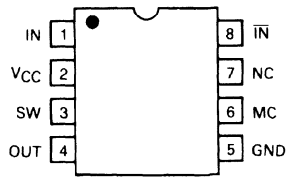
ORDERING INFORMATION

MC12022LVAP/BP	Plastic
MC12022LVAD/BD	SOIC

Note: For positive edge triggered synthesizers, order the MC12022LVA

For Negative edge triggered synthesizers, order the MC12022LVB

PRESCALER PIN ASSIGNMENT



(Top View)

FUNCTION TABLE		
SW	**MC**	**Divide Ratio**
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H = V_{CC}, L = Open
MC: H = 2.0 V to V_{CC}
L = Gnd to 0.8 V

6

LOGIC DIAGRAM (MC12022LVA)

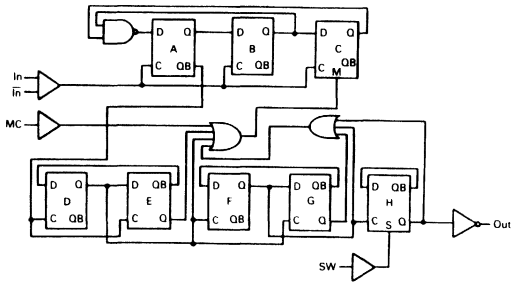
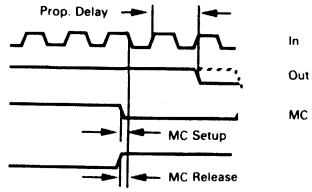


FIGURE 1 — MODULUS SETUP TIME



Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

FIGURE 2 — TYPICAL OUTPUT WAVEFORMS

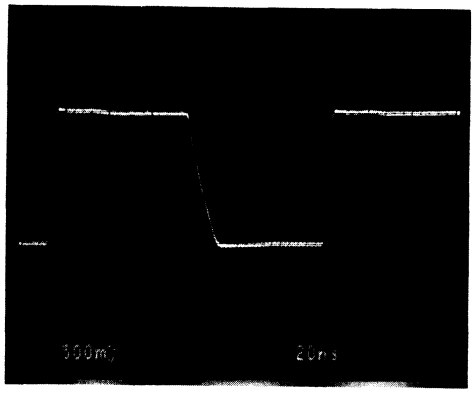


FIGURE 2A — ÷64, 500 MHz, 5.0 V, +25°C, OUTPUT LOADED

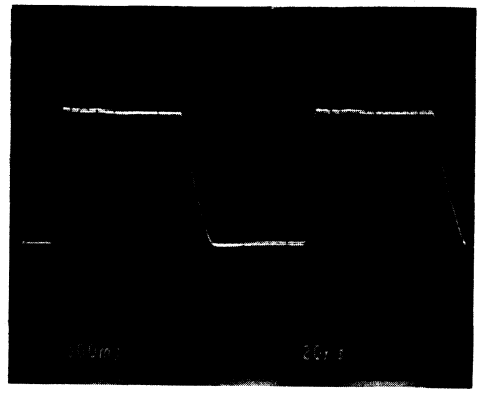
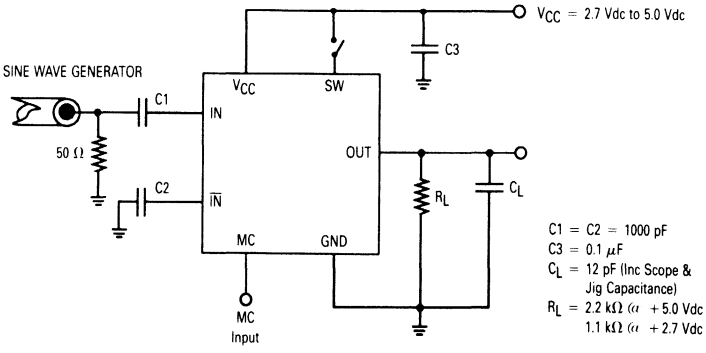


FIGURE 2B — ÷128, 1.1 GHz, 5.0 V, +25°C, OUTPUT LOADED

FIGURE 3 — AC TEST CIRCUIT



6

FIGURE 4A — INPUT SIGNAL AMPLITUDE versus INPUT FREQUENCY
DIVIDE RATIO = 128

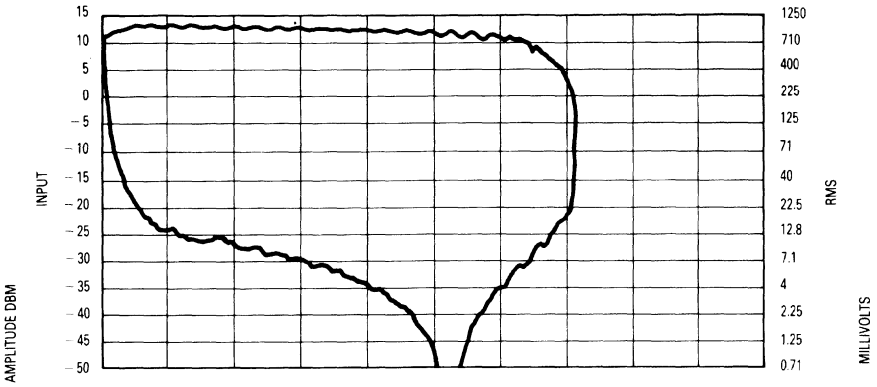


FIGURE 4B — OUTPUT AMPLITUDE versus INPUT FREQUENCY

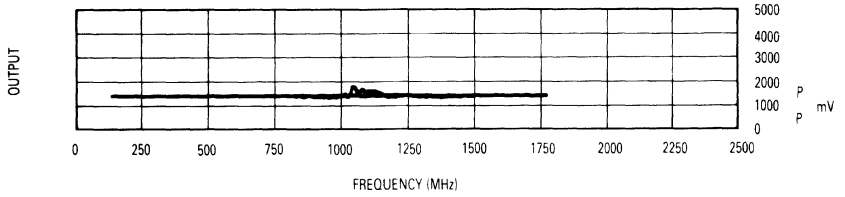
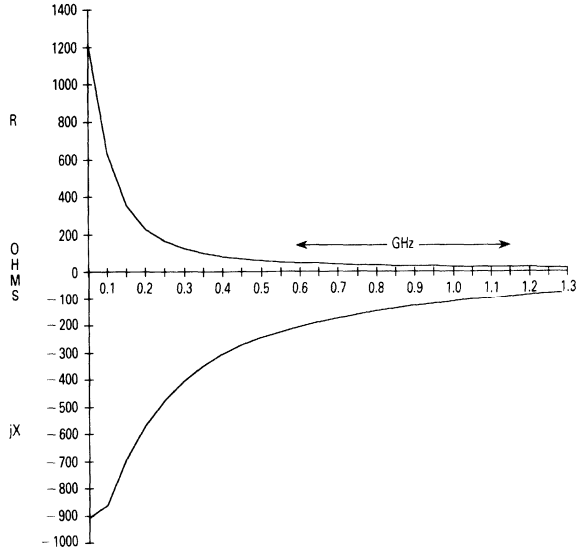


FIGURE 4C — TYPICAL INPUT IMPEDANCE versus INPUT FREQUENCY



6

MOTOROLA

MC12022SLA
MC12022SLB

1.1 GHz DUAL MODULUS PRESCALER

The MC12022SLA can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

The MC12022SLB can be used with CMOS synthesizers requiring negative edges to trigger internal counters such as Fujitsu's MB87001.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

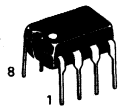
The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5 V
- Low Power 4.0 mA Typical
- Operating Temperature Range of −40°C to +85°C
- Short Setup Time (t_{set}) 16 ns Maximum @ 1.1 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL

MECL PLL COMPONENTS

1.1 GHz ÷64/65, ÷128/129 DUAL MODULUS PRESCALER

P SUFFIX
PLASTIC PACKAGE
CASE 626

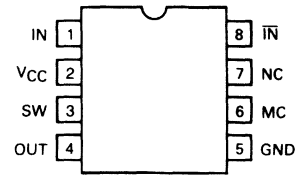


D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

Design Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

*Equivalent to a two-input NAND gate.

PRESCALER PIN ASSIGNMENT



(Top View)

Note 1:
For positive edge triggered synthesizers, order the MC12022SLA.
For negative edge triggered synthesizers, order the MC12022SLB.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	−0.5 to +7.0	Vdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Modulus Control Input, Pin 6	MC	−0.5 to +6.5	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = −40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current Output Unloaded (Pin 2)	I_{CC}	—	4.0	6.5	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	—	—	V
Modulus Control Input Low (MC)	V_{IL1}	—	—	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	OPEN	OPEN	OPEN	—
Output Voltage Swing (C_L = 8 pF, R_L = 4.4 kΩ)	V_{out}	1.0	1.6	—	V_{p-p}
Modulus Setup Time MC to Out	t_{SET}	—	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	V_{in}	100 400	— —	1500 1500	mVpp
Output Current C_L = 8 pF, R_L = 4.4 kΩ	I_O	—	—	1.0	mA

FUNCTION TABLE		
SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC}
L = Gnd to 0.8 V

6

LOGIC DIAGRAM (MC12022SLA)

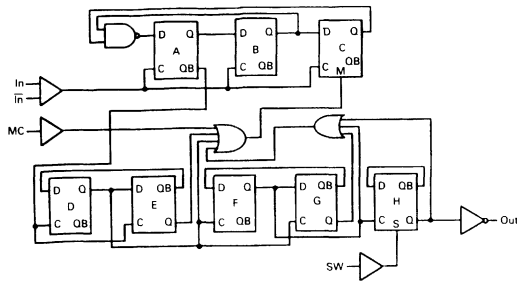
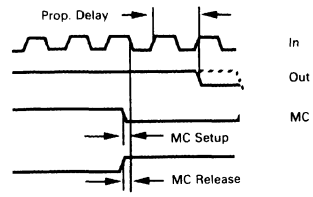


FIGURE 1 — MODULUS SETUP TIME



Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

FIGURE 2 — TYPICAL OUTPUT WAVEFORMS

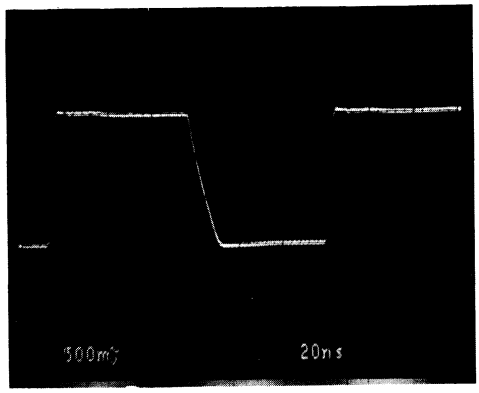


FIGURE 2A — ÷64, 500 MHz, 5.0 V, +25°C, OUTPUT LOADED

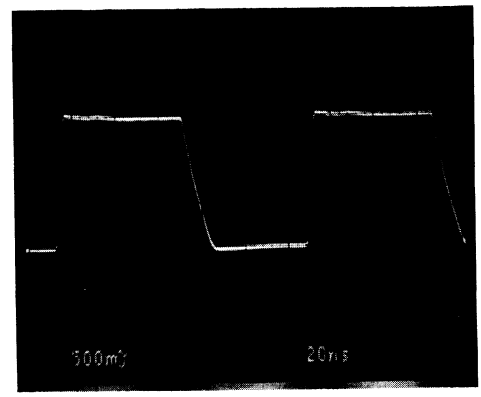
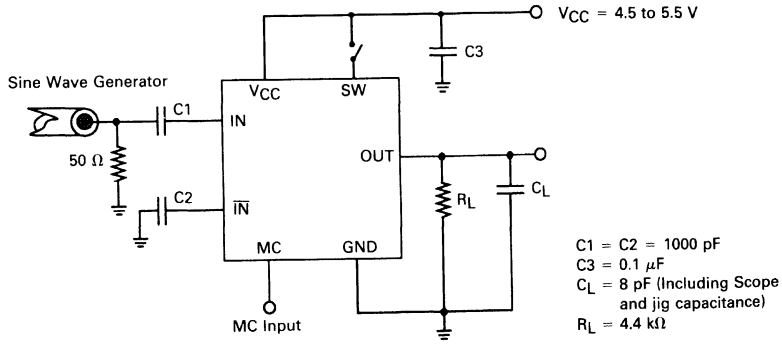


FIGURE 2B — ÷128, 1.1 GHz, 5.0 V, +25°C, OUTPUT LOADED

FIGURE 3 — AC TEST CIRCUIT



C1 = C2 = 1000 pF
C3 = 0.1 μF
C_L = 8 pF (Including Scope and jig capacitance)
R_L = 4.4 kΩ

6

FIGURE 4 — MC12022SL TYPICAL CHARACTERISTIC CURVES

FIGURE 4A — INPUT SIGNAL AMPLITUDE versus INPUT FREQUENCY
DIVIDE RATIO = 128

FIGURE 4B — OUTPUT AMPLITUDE versus INPUT FREQUENCY

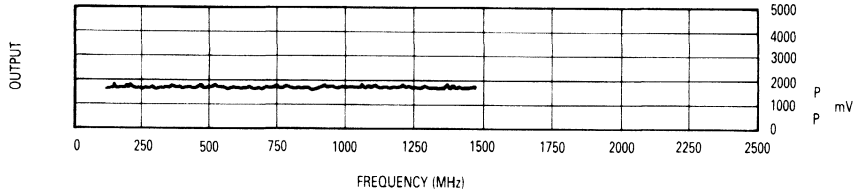
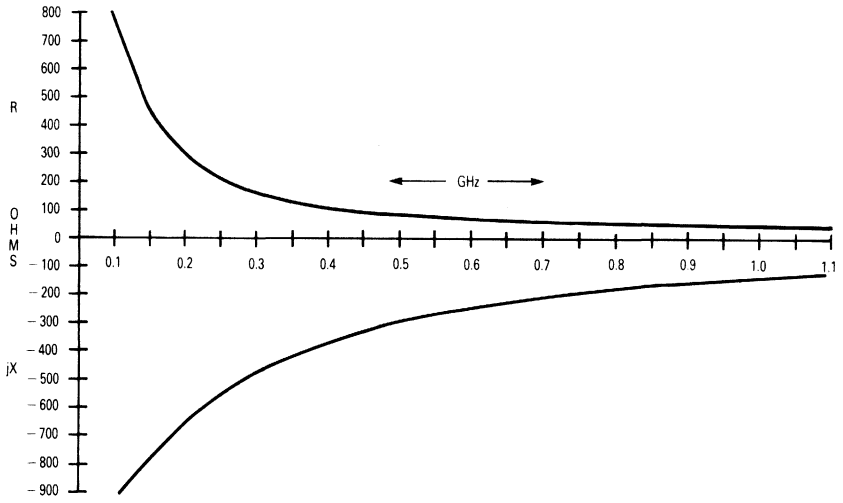


FIGURE 4C — TYPICAL INPUT IMPEDANCE versus INPUT FREQUENCY



6

MOTOROLA

MC12022TSA
MC12022TSB

1.1 GHz DUAL MODULUS PRESCALER

The MC12022TSA can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

The MC12022TSB can be used with CMOS synthesizers requiring negative edges to trigger internal counters such as Fujitsu's MB87001.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

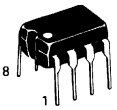
The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5 V
- Low Power 4.0 mA Typical
- Operating Temperature Range of −40°C to +85°C
- Short Setup Time (t_{set}) 16 ns Maximum @ 1.1 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Output Load Resistor on Die

MECL PLL COMPONENTS

1.1 GHz ÷64/65, ÷128/129 DUAL MODULUS PRESCALER

P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

Design Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

*Equivalent to a two-input NAND gate.

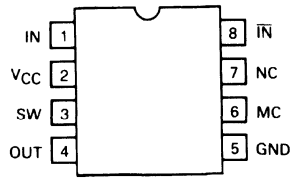
MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 8	V_{CC}	−0.5 to +7.0	Vdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = −40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current Output	I_{CC}	—	4.0	6.5	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	—	—	V
Modulus Control Input Low (MC)	V_{IL1}	—	—	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	OPEN	OPEN	OPEN	—
Output Voltage Swing (C_L = 8 pF)	V_{out}	1.0	1.4	—	V_{p-p}
Modulus Setup Time MC to Out	t_{SET}	—	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	V_{in}	100 400	— —	1500 1500	mVpp

PRESCALER PIN ASSIGNMENT



(Top View)

WARNING: DO NOT CONNECT PIN 7.
LEAVE PIN 7 OPEN.

FUNCTION TABLE		
SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC}
L = Gnd to 0.8 V

6

LOGIC DIAGRAM (MC12022TSA)

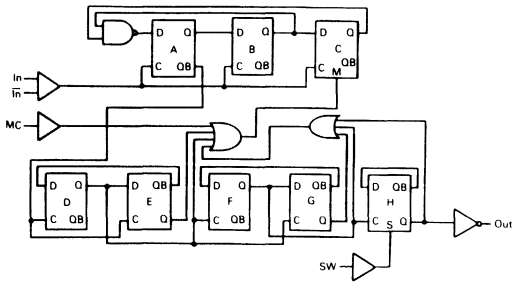
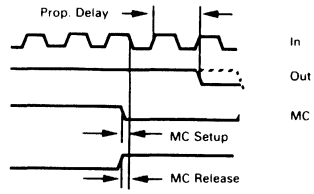


FIGURE 1 — MODULUS SETUP TIME



Modulus setup time MC to out is the MC setup or MC release plus the prop. delay

FIGURE 2 — TYPICAL OUTPUT WAVEFORMS

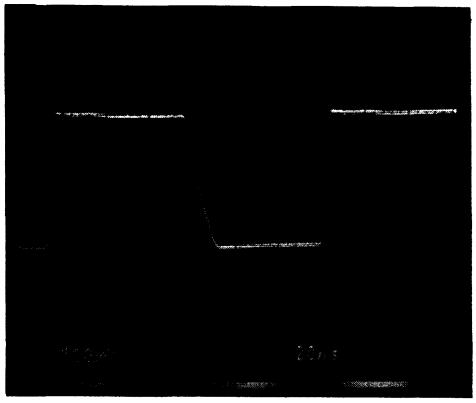


FIGURE 2A — ÷64, 500 MHz, 5.0 V, +25°C, OUTPUT LOADED

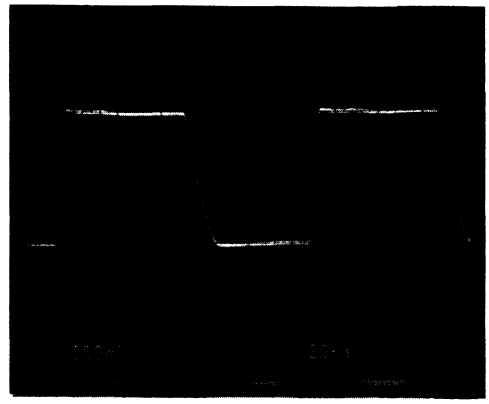
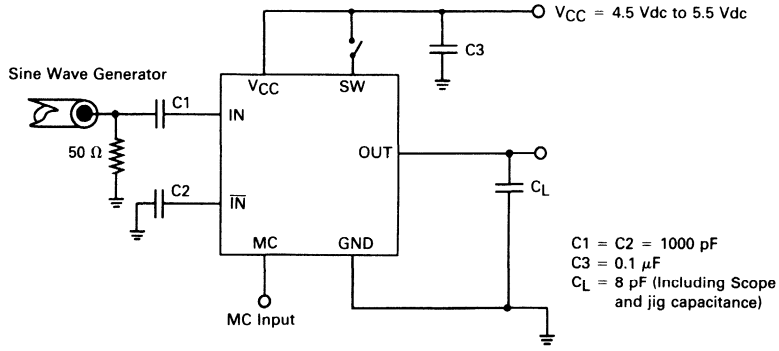


FIGURE 2B — ÷128, 1.1 GHz, 5.0 V, +25°C, OUTPUT LOADED

FIGURE 3 — AC TEST CIRCUIT



6

MOTOROLA

MC12022TVA

MECL PLL COMPONENTS

1.1 GHz ÷64/65, ÷128/129
LOW VOLTAGE
DUAL MODULUS
PRESCALER

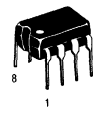
1.1 GHz Low Voltage Dual Modulus Prescaler

The MC12022TVA can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX.

A Divide Ratio Control (SW) permits selection of a 64/64 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

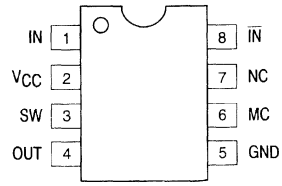
- 1.1 GHz Toggle Frequency
- Supply Voltage of 2.7 to 5.0 V
- Low Power 4.0 mA Typical @ V_{CC} = 2.7 V
- Operating Temperature Range of −40°C to +85°C
- Short Setup Time (t_{set}) 16 ns Maximum @ 1.1 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Output Load Resistor on Die



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

PIN ASSIGNMENTS
(Top View)



MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 8	V_{CC}	−0.5 to + 7.0	Vdc
Operating Temperature Range	T_A	−40 to + 85	°C
Storage Temperature Range	T_{stg}	−65 to + 150	°C
Modulus Control Input, Pin 6	MC	−0.5 to + 6.5	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.0 Vdc, T_A = −40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current (Pin 2 at 2.7 Vdc)	I_{CCL}	–	4.0	6.5	mA
Supply Current (Pin 2 at 5.0 Vdc)	I_{CCH}	–	5.8	8.0	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	–	V
Modulus Control Input Low (MC)	V_{IL1}	–	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	–
Output Voltage Swing (C_L = 8 pF @ 2.7 Vdc)	V_{out}	0.8	1.0	–	V_{p-p}
Output Voltage Swing (C_L = 8 pF @ 5.0 Vdc)	V_{out}	1.0	1.4	–	V_{p-p}
Modulus Setup Time MC to Out	t_{set}	–	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	V_{in}	100 400	– –	1500 1500	mVpp

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H = V_{CC}, L = Open
MC: H = 2.0 V to V_{CC}, L = Gnd to 0.8 V

6

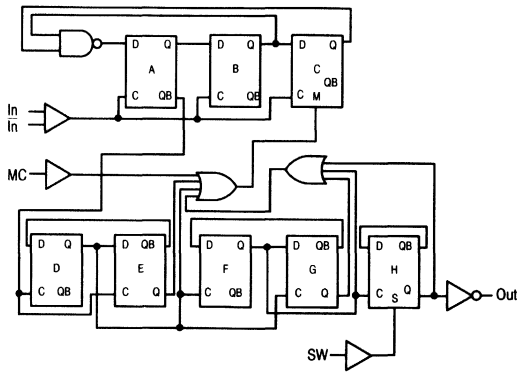
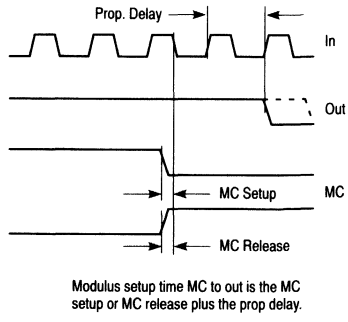


Figure 1. Logic Diagram (MC12022TVA)



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 2. Modulus Setup Time

TYPICAL OUTPUT WAVEFORMS

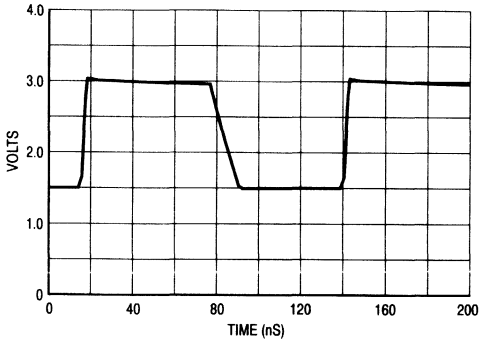


Figure 3. ÷64, 500 MHz, 5.0 V, +25°C, Output Loaded

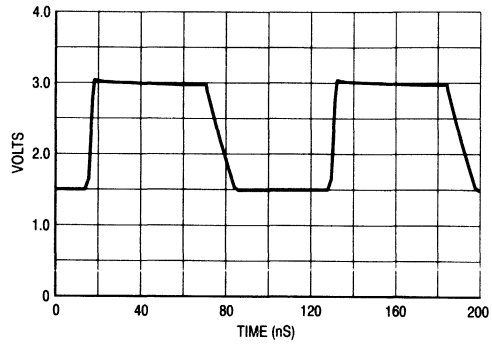


Figure 4. ÷128, 1.1 GHz, 5.0 V, +25°C, Output Loaded

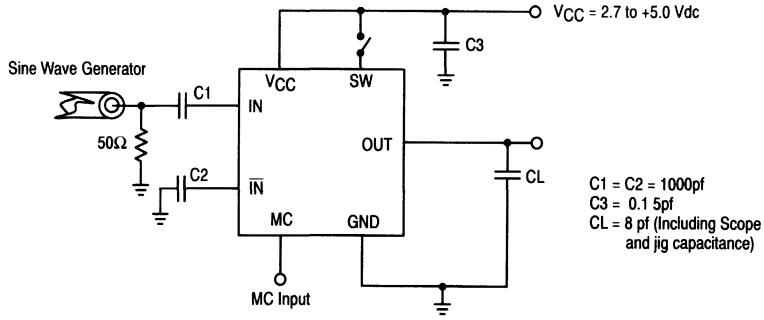


Figure 5. AC Test Circuit

6

MOTOROLA

MC12022TVB

MECL PLL COMPONENTS

1.1 GHz ÷64/65, ÷128/129
LOW VOLTAGE
DUAL MODULUS
PRESCALER

1.1 GHz LOW VOLTAGE DUAL MODULUS PRESCALER

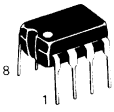
The MC12022TVB can be used with CMOS synthesizers requiring negative edges to trigger internal counters such as Fujitsu's MB87001.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 2.7 to 5.0 V
- Low Power 4.0 mA Typical @ V_{CC} = 2.7 V
- Operating Temperature Range of −40°C to +85°C
- Short Setup Time (t_{set}) 16 ns Maximum @ 1.1 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Output Load Resistor on Die

P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

Design Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

*Equivalent to a two-input NAND gate.

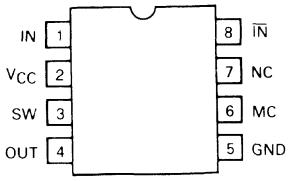
MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 8	V_{CC}	−0.5 to +7.0	Vdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Modulus Control Input, Pin 6	MC	−0.5 to +6.5	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.0 Vdc, T_A = −40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current Output Unloaded (Pin 2) at 2.7 Vdc	I_{CCL}	—	4.0	6.5	mA
Supply Current Output Unloaded (Pin 2) at 5.0 Vdc	I_{CCH}	—	5.8	8.0	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	—	—	V
Modulus Control Input Low (MC)	V_{IL1}	—	—	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	OPEN	OPEN	OPEN	—
Output Voltage Swing (C_L = 8 pF @ 2.7 Vdc)	V_{out}	0.8	1.0	—	Vp-p
Output Voltage Swing (C_L = 8 pF @ 5.0 Vdc)	V_{out}	1.0	1.4	—	Vp-p
Modulus Setup Time MC to Out	t_{SET}	—	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	V_{in}	100 400	— —	1500 1500	mVpp

PRESCALER PIN ASSIGNMENT



(Top View)

FUNCTION TABLE		
SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC}
L = Gnd to 0.8 V

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LOGIC DIAGRAM (MC12022TVB)

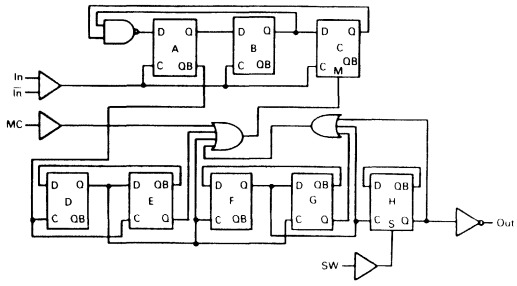
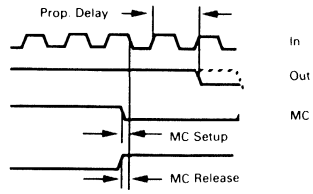


FIGURE 1 — MODULUS SETUP TIME



Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

FIGURE 2 — TYPICAL OUTPUT WAVEFORMS

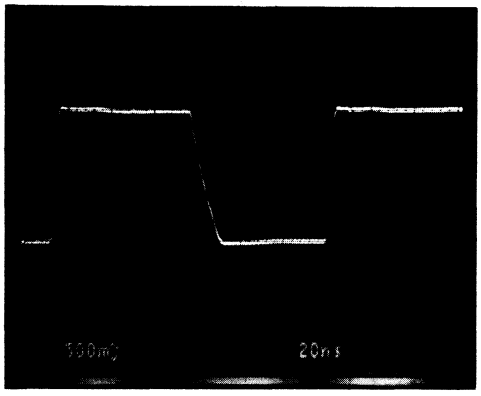


FIGURE 2A — ÷64, 500 MHz, 5.0 V, +25°C, OUTPUT LOADED

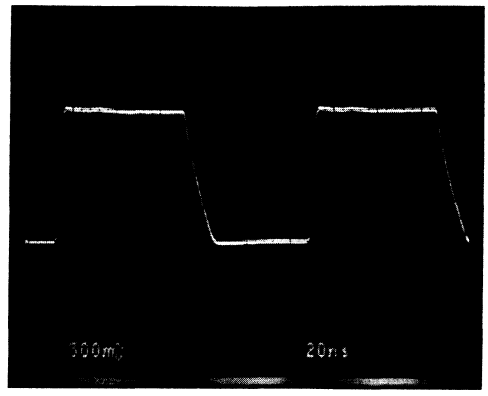
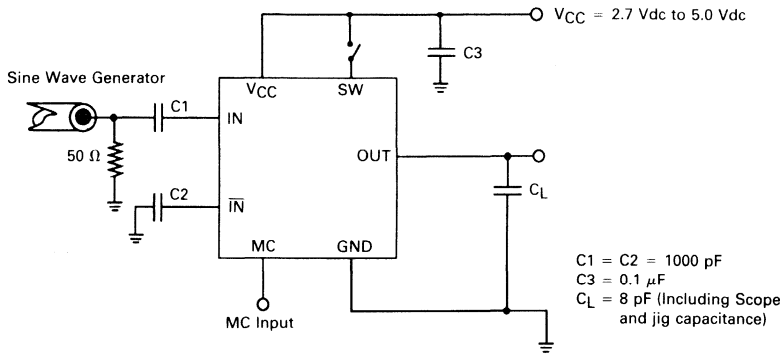


FIGURE 2B — ÷128, 1.1 GHz, 5.0 V, +25°C, OUTPUT LOADED

FIGURE 3 — AC TEST CIRCUIT



6

MOTOROLA

MC12023

MECL PLL COMPONENTS

225 MHz ÷64 PRESCALER

225 MHz PRESCALER

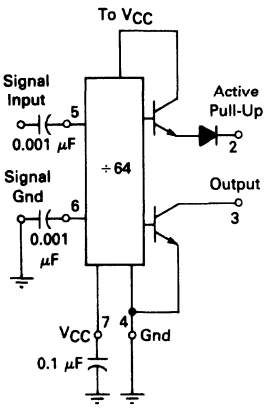
The MC12023 is a prescaler which will divide by 64. This device may be operated over supply voltage range of 3.2 to 5.5 V.

- 225 MHz Toggle Frequency
- Low Power—4.8 mA Maximum at 5.5 V
- Operating Supply Voltage — 3.2 V to 5.5 V
- Connecting Pins 2 and 3 Allows Driving One TTL Load

P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

PRESCALER BLOCK DIAGRAM



MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	0 to + 8.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.2 to 5.5 V, T_A = 0°C to +70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency	f_{max}	225	—	—	MHz
(Sine wave input)	f_{min}	—	—	35	MHz
Supply Current @ 5.5 V	I_{CC}	—	3.5**	4.8	mA
Output Voltage High* (I_{source} = 50 μA, V_{CC} = 3.2 V)	V_{OH}	1.2	1.4	—	V
Output Voltage High* (I_{source} = 50 μA, V_{CC} = 5.0 V)	V_{OH}	2.5	—	—	V
Output Voltage Low* (I_{sink} = 2.0 mA)	V_{OL}	—	—	0.5	V
Input Voltage Sensitivity	V_{in}				mVpp
35 MHz		400	—	800	
50–225 MHz		200	—	800	

*Pin 2 connected to Pin 3
**V_{CC} = 4.5 V

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MOTOROLA

MC12025

MECL PLL COMPONENTS

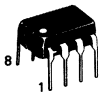
520 MHz ÷64/65 DUAL MODULUS PRESCALER

520 MHz DUAL MODULUS PRESCALER

The MC12025 is a dual modulus prescaler which divides by 64 and 65. Supply voltages of 4.75 V to 5.25 V may be connected to Pin 8.

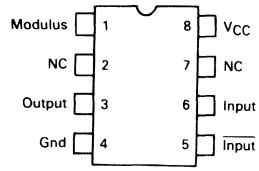
- 520 MHz Toggle Frequency
- Low-Power 9.5 mA Typical
- Control Input Is Compatible with Standard CMOS and TTL
- Supply Voltage 5.0 V, ± 0.25 V
- Propagation Delay 30 ns Typical

PIN ASSIGNMENTS



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751



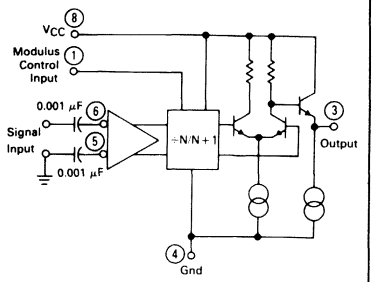
MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 8	V_{CC}	7.0	Vdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.75 to 5.25 V, T_A = −40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_{max} f_{min}	520	—	— 30	MHz
Supply Current (Pin 8)	I_{CC}	—	9.5	11.5	mA
Control Input High (÷ 64)	V_{IH}	2.0	—	—	V
Control Input Low (÷ 65)	V_{IL}	—	—	0.8	V
Output Voltage	V_{out}	0.8	1.2	—	V_{pp}
Input Voltage Sensitivity 30 MHz 100-520 MHz	V_{in}	 400 100	 — —	 800 800	mVpp
PLL Response Time (Notes 1 and 2)	t_{PLL}	—	—	t_{out}−42	ns

Note 1. t_{PLL} = The period of time the PLL has from the rising output transition to the Modulus Control input edge transition to ensure proper modulus selection.
Note 2. t_{out} = Period of output waveform.



6

MOTOROLA

MC12028A
MC12028B

MECL PLL COMPONENTS

1.1 GHz
÷32/33, ÷64/65
DUAL MODULUS
PRESCALER

1.1 GHz DUAL MODULUS PRESCALER

The MC12028A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

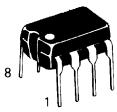
The MC12028B can be used with CMOS synthesizers requiring negative edges to trigger internal counters such as Fujitsu's MB87001.

A Divide Ratio Control (SW) permits selection of a 32/33 or 64/65 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- MC12028A for Positive Edge Triggered Synthesizers
- MC12028B for Negative Edge Triggered Synthesizers
- 6.5 mA Maximum, −40°C to +85°C, V_{CC} = 5.5 Vdc
- Modulus Control Input is Compatible with Standard CMOS and TTL
- Low-Power 4.0 mA Typical

P SUFFIX
PLASTIC PACKAGE
CASE 626

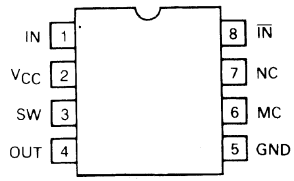


D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

Design Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

*Equivalent to a two-input NAND gate.

PRESCALER PIN ASSIGNMENT



(Top View)

Note 1:
For positive edge triggered synthesizers, order the MC12028A.
For negative edge triggered synthesizers, order the MC12028B.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	−0.5 to +7.0	Vdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Modulus Control Input, Pin 6	MC	−0.5 to +6.5	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 Vdc, T_A = −40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)	f_t	0.1	1.4	1.1	GHz
Supply Current Output Unloaded (Pin 2)	I_{CC}	—	4.0	6.5	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	—	—	V
Modulus Control Input Low (MC)	V_{IL1}	—	—	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	OPEN	OPEN	OPEN	—
Output Voltage Swing (C_L = 12 pF, R_L = 2.2 kΩ)	V_{out}	1.0	1.6	—	V_{p-p}
Modulus Setup Time MC to Out	t_{SET}	—	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	V_{in}	100 400	— —	1500 1500	mVpp
Output Current C_L = 12 pF, R_L = 2.2 kΩ	I_O	—	—	2.0	mA

FUNCTION TABLE		
SW	MC	Divide Ratio
H	H	32
H	L	33
L	H	64
L	L	65

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC}
L = Gnd to 0.8 V

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LOGIC DIAGRAM (MC12028A)

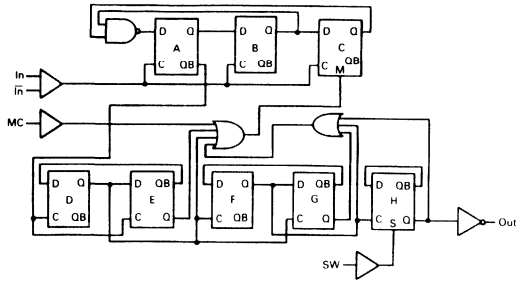
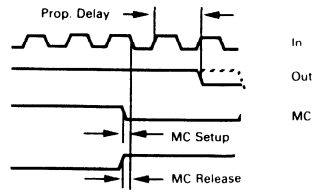


FIGURE 1 — MODULUS SETUP TIME



Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

FIGURE 2 — TYPICAL OUTPUT WAVEFORM

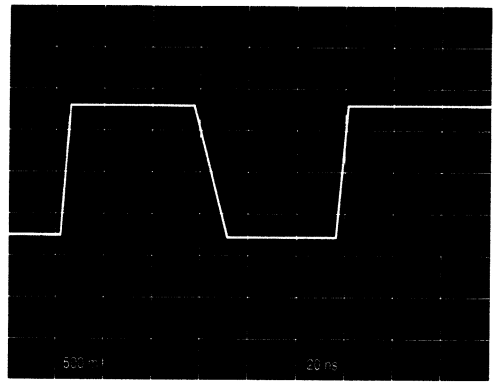


FIGURE 3 — AC TEST CIRCUIT

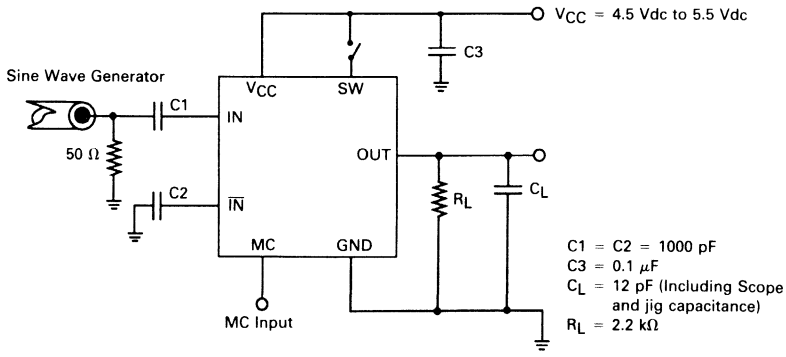


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FIGURE 4 — TYPICAL INPUT IMPEDANCE versus INPUT FREQUENCY

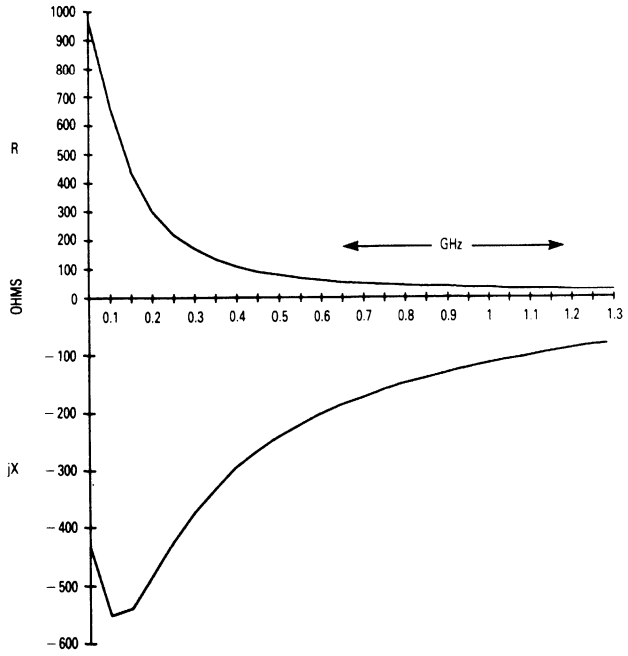
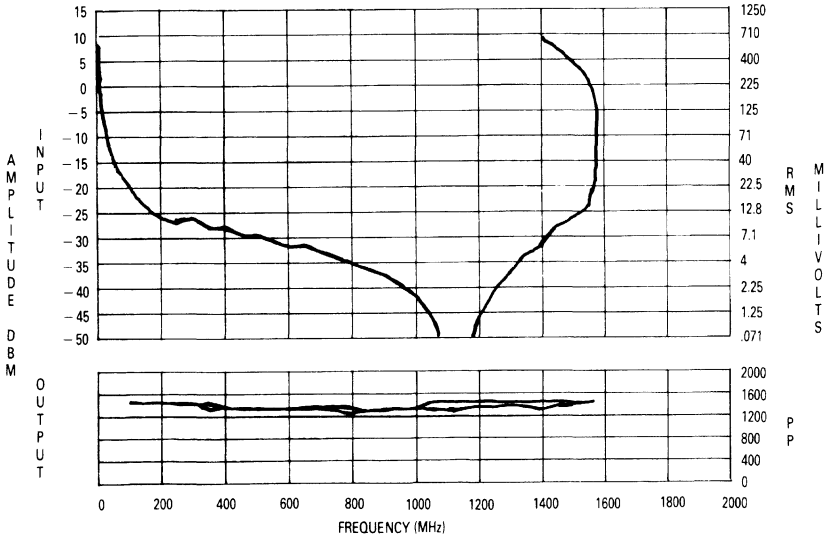


FIGURE 5 — INPUT SIGNAL AMPLITUDE versus INPUT FREQUENCY. DIVIDE RATIO = 32



MOTOROLA

MC12031A
MC12031B

Advance Information

2.0GHz Low Voltage Dual Modulus Prescaler

MECL PLL COMPONENTS

÷64/65, ÷128/129

2.0GHz Low Voltage Dual Modulus Prescaler

The MC12031 is a high frequency low voltage dual modulus prescaler used in phase-locked loop (PLL) applications. A high frequency input signal up to 2.4GHz is provided for cordless and cellular communication services such as DECT, PHP, and PCS.

The MC12031A can be used with CMOS synthesizer requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signal up to 1.1GHz in programmable frequency steps. The MC12031B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0GHz Toggle Frequency
- Supply Voltage 2.7V to 5.0Vdc
- Low Power 10.0mA Typical at V_{CC} = 2.7V
- Operating Temperature Range of –40 to +85°C
- The MC12031 is Pin and Functionally Compatible with the MC12022
- Short Setup Time (t_{set}) 8ns Typical at 2.0GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL

P SUFFIX
PLASTIC PACKAGE
CASE 626

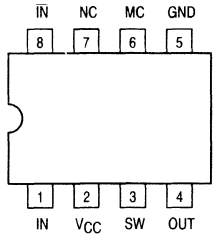
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

FUNCTION TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H = V_{CC}, L = OPEN
MC: H = 2.0V to V_{CC}; L = GND to 0.8V

Pinout: 8-Lead Plastic (Top View)



For positive edge triggered synthesizers, order the MC12031A
For negative edge triggered synthesizers, order the MC12031B

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage, Pin 2	–0.5 to +7.0	Vdc
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
MC	Modulus Control Input, Pin 6	–0.5 to +6.5	Vdc

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.0V; T_A = −40 to +85°C)

Symbol	Parameter		Min	Typ	Max	Unit
ft	Toggle Frequency (Sine Wave)		0.5	2.4	2.0	GHz
I_{CC}	Supply Current Output (Pin 2)	V_{CC} = 2.7V V_{CC} = 5.0V		10.0 13.0	TBD TBD	mA
V_{IH1}	Modulus Control Input HIGH (MC)		2.0		V_{CC}	V
V_{IL1}	Modulus Control Input LOW (MC)		GND		0.8	V
V_{IH2}	Divide Ratio Control Input HIGH (SW)		V_{CC}	V_{CC}	V_{CC}	V
V_{IL2}	Divide Ratio Control Input LOW (SW)		OPEN	OPEN	OPEN	—
V_{OUT}	Output Voltage Swing (Note 1)	C_L = 8pF; R_L = 1.2kΩ	0.8	1.2		V_{PP}
t_{set}	Modulus Setup Time MC to OUT @ 2000MHz			8	10	ns
V_{IN}	Input Voltage Sensitivity	500–2000MHz	100		1000	mV_{PP}
I_O	Output Current (Note 2)	V_{CC} = 2.7V, C_L = 8pF, R_L = 1.2kΩ V_{CC} = 5.0V, C_L = 8pF, R_L = 3.0kΩ		1.2 1.2	4.0 4.0	mA

1. Valid over voltage range 2.7 to 5.0V; R_L = 1.2kΩ @ V_{CC} = 2.7V; R_L = 3.0kΩ @ V_{CC} = 5.0V
2. Divide ratio of ÷64/65 @ 2.0GHz

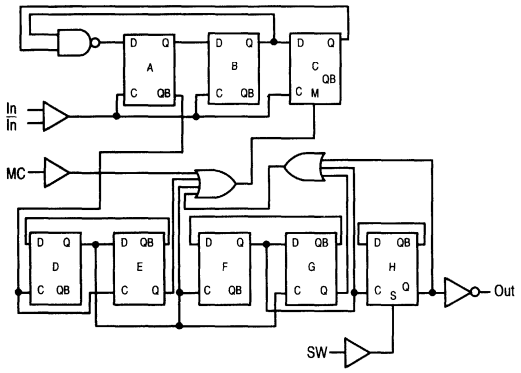
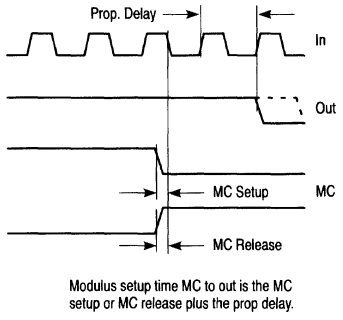


Figure 1. Logic Diagram (MC12031A)



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 2. Modulus Setup Time

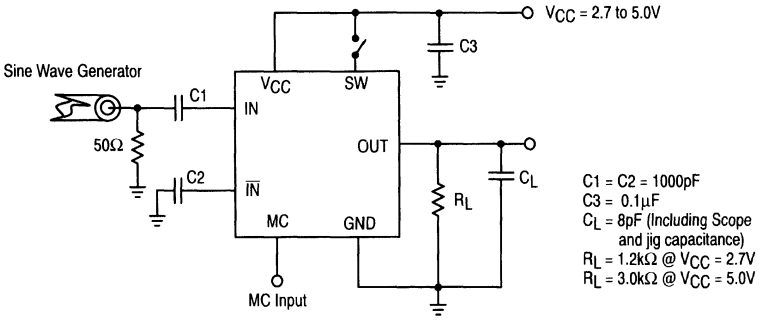


Figure 3. AC Test Circuit

MOTOROLA

MC12032A
MC12032B

2.0 GHz DUAL MODULUS PRESCALER

MECL PLL COMPONENTS

2.0 GHz
÷64/65, ÷128/129
DUAL MODULUS
PRESCALER

The MC12032A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 2.0 GHz in programmable frequency steps.

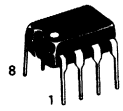
The MC12032B can be used with CMOS synthesizers requiring negative edges to trigger internal counters such as Fujitsu's MB87001.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0 GHz Toggle Frequency
- MC12032A for Positive Edge Triggered Synthesizers
- MC12032B for Negative Edge Triggered Synthesizers
- 12 mA Maximum, −40°C to +85°C, V_{CC} = 5.5 Vdc
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Low-Power 8.5 mA Typical

P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
SOIC PACKAGE
CASE 751

ORDERING INFORMATION

MC12032AP/BP	Plastic
MC12032AD/BD	SOIC

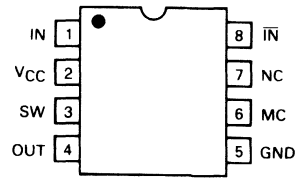
Note: For positive edge triggered synthesizers, order the MC12032A

For Negative edge triggered synthesizers, order the MC12032B

Design Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

*Equivalent to a two-input NAND gate.

PRESCALER PIN ASSIGNMENT



(Top View)

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	−0.5 to +7.0	Vdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Modulus Control Input, Pin 6	MC	−0.5 to +6.5	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = −40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.5	2.4	2.0	GHz
Supply Current Output Unloaded (Pin 2)	I_{CC}	—	8.5	12	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	—	—	V
Modulus Control Input Low (MC)	V_{IL1}	—	—	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	V
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	—
Output Voltage Swing (C_L = 12 pF, R_L = 2.2 kΩ)	V_{out}	1.0	1.6	—	V_{p-p}
Modulus Setup Time MC to Out	t_{SET}	—	8	10	ns
Input Voltage Sensitivity @ 500–2000 MHz	V_{in} Min	100	—	1500	mVpp
Output Current C_L = 12 pF, R_L = 2.2 kΩ	I_O	—	—	2.0	mA

FUNCTION TABLE		
SW	**MC**	**Divide Ratio**
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H = V_{CC}, L = Open
MC: H = 2.0 V to V_{CC}
L = Gnd to 0.8 V

6

LOGIC DIAGRAM (MC12032A)

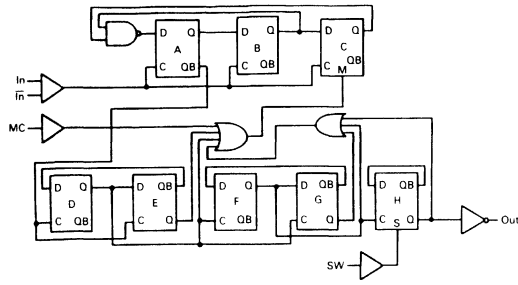
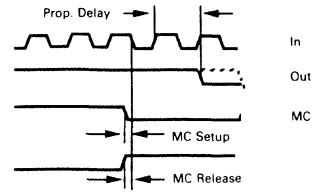


FIGURE 1 — MODULUS SETUP TIME



Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

FIGURE 2 — TYPICAL OUTPUT WAVEFORMS

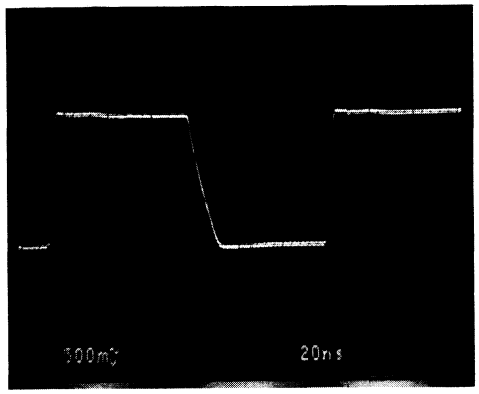


FIGURE 2A — ÷64, 500 MHz, 5.0 V, +25°C, OUTPUT LOADED

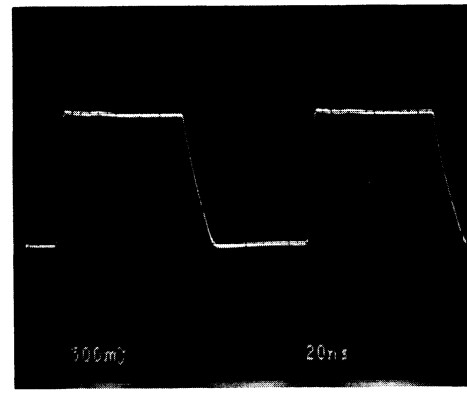


FIGURE 2B — ÷128, 1.1 GHz, 5.0 V, +25°C, OUTPUT LOADED

FIGURE 3 — AC TEST CIRCUIT

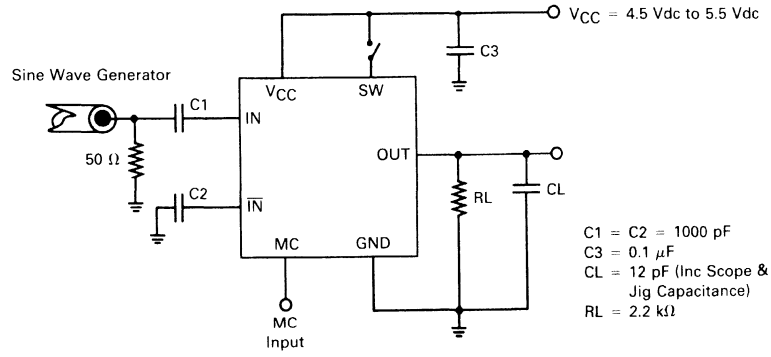


FIGURE 4A — INPUT SIGNAL AMPLITUDE versus INPUT FREQUENCY
DIVIDE RATIO = 128

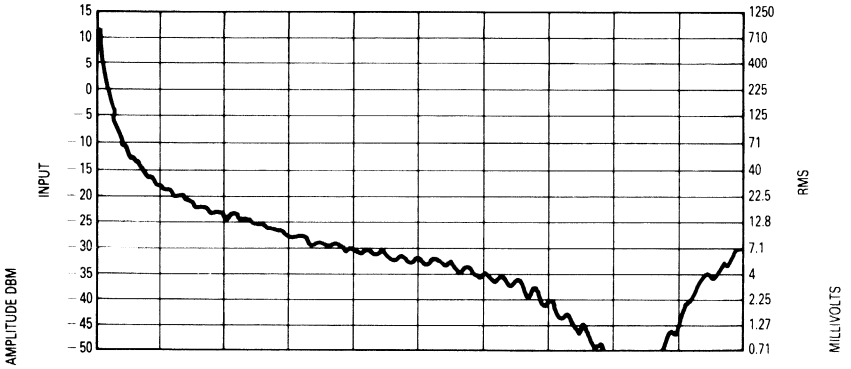


FIGURE 4B — OUTPUT AMPLITUDE versus INPUT FREQUENCY

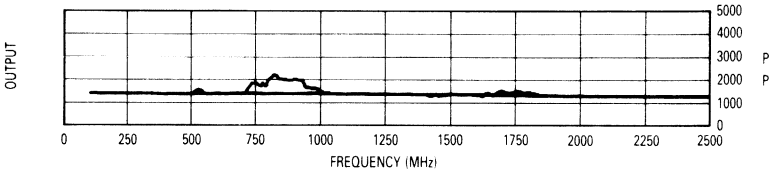
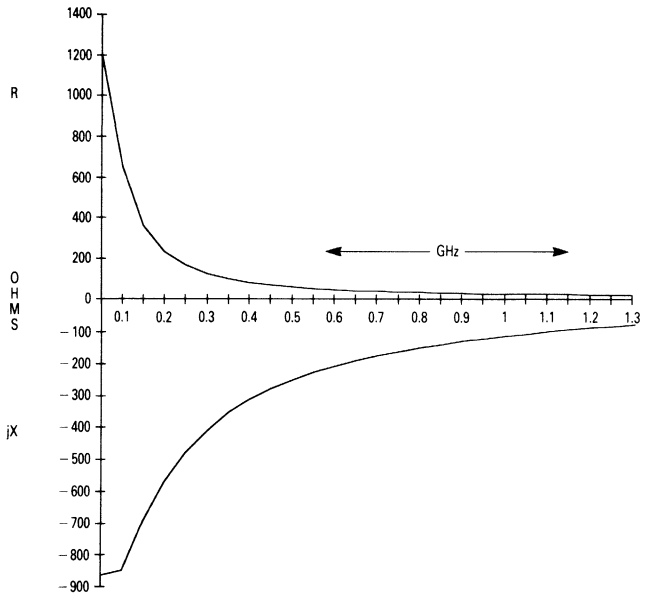


FIGURE 4C — TYPICAL INPUT IMPEDANCE versus INPUT FREQUENCY



6

MOTOROLA

MC12033A
MC12033B

Advance Information

2.0GHz Low Voltage Dual Modulus Prescaler

MECL PLL COMPONENTS

÷32/33, ÷64/65

2.0GHz Low Voltage Dual Modulus Prescaler

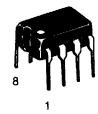
The MC12033 is a high frequency low voltage dual modulus prescaler used in phase-locked loop (PLL) applications. A high frequency input signal up to 2.4GHz is provided for cordless and cellular communication services such as DECT, PHP, and PCS.

The MC12033A can be used with CMOS synthesizer requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signal up to 1.1GHz in programmable frequency steps. The MC12033B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 32/33 or 64/65 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

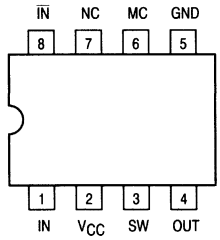
- 2.0GHz Toggle Frequency
- Supply Voltage 2.7V to 5.0Vdc
- Low Power 10.0mA Typical at V_{CC} = 2.7V
- Operating Temperature Range of –40 to +85°C
- The MC12033 is Pin and Functionally Compatible with the MC12022
- Short Setup Time (t_{set}) 8ns Typical at 2.0GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

Pinout: 8-Lead Plastic (Top View)



For positive edge triggered synthesizers, order the MC12033A
For negative edge triggered synthesizers, order the MC12033B

FUNCTION TABLE

SW	MC	Divide Ratio
H	H	32
H	L	33
L	H	64
L	L	65

Note: SW: H = V_{CC}, L = OPEN
MC: H = 2.0V to V_{CC}; L = GND to 0.8V

6

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage, Pin 2	–0.5 to +7.0	Vdc
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
MC	Modulus Control Input, Pin 6	–0.5 to +6.5	Vdc

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.0V; T_A = –40 to +85°C)

Symbol	Parameter		Min	Typ	Max	Unit
ft	Toggle Frequency (Sine Wave)		0.5	2.4	2.0	GHz
I_{CC}	Supply Current Output (Pin 2)	V_{CC} = 2.7V V_{CC} = 5.0V		10.0 13.0	TBD TBD	mA
V_{IH1}	Modulus Control Input HIGH (MC)		2.0		V_{CC}	V
V_{IL1}	Modulus Control Input LOW (MC)		GND		0.8	V
V_{IH2}	Divide Ratio Control Input HIGH (SW)		V_{CC}	V_{CC}	V_{CC}	V
V_{IL2}	Divide Ratio Control Input LOW (SW)		OPEN	OPEN	OPEN	—
V_{OUT}	Output Voltage Swing (Note 1)	C_L = 8pF; R_L = 600Ω	0.8	1.2		V_{PP}
t_{set}	Modulus Setup Time MC to OUT @ 2000MHz			8	10	ns
V_{IN}	Input Voltage Sensitivity	500–2000MHz	100		1000	mV_{PP}
I_O	Output Current (Note 2)	V_{CC} = 2.7V, C_L = 8pF, R_L = 600Ω V_{CC} = 5.0V, C_L = 8pF, R_L = 1.5kΩ		2.4 2.4	4.0 4.0	mA

1. Valid over voltage range 2.7 to 5.0V; R_L = 600Ω @ V_{CC} = 2.7V; R_L = 1.5kΩ @ V_{CC} = 5.0V
2. Divide ratio of ÷32/33 @ 2.0GHz

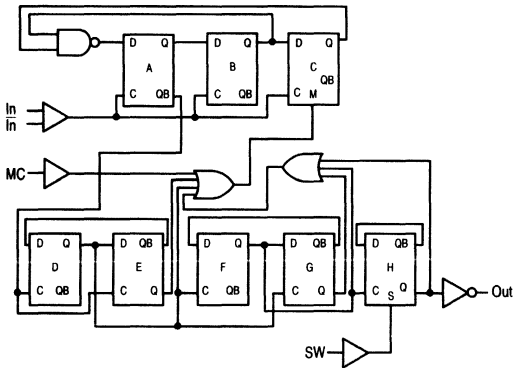


Figure 1. Logic Diagram (MC12033A)

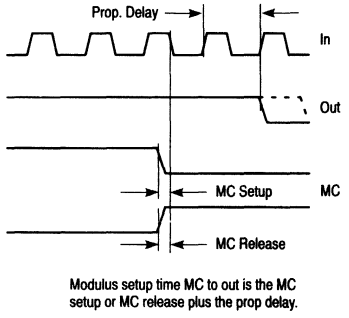


Figure 2. Modulus Setup Time

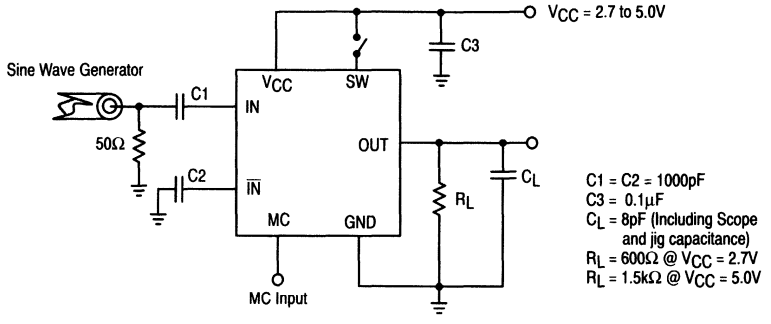


Figure 3. AC Test Circuit

6

MOTOROLA

MC12034A
MC12034B

MECL PLL COMPONENTS
2.0 GHz
÷32/33
÷64/65
DUAL MODULUS PRESCALER

2.0 GHz Dual Modulus Prescaler

The MC12034A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 2.0 GHz in programmable frequency steps.

The MC12034B can be used with CMOS synthesizers requiring negative edges to trigger internal counters such as Fujitsu's MB87001.

A Divide Ratio Control (SW) permits selection of a 32/33 or 64/65 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0 GHz Toggle Frequency
- MC12034A for Positive Edge Triggered Synthesizers
- MC12034B for Negative Edge Triggered Synthesizers
- 12 mA Maximum, –40°C to +85°C, V_{CC} = 5.5 Vdc
- Modulus Control Input is Compatible with Standard CMOS and TTL
- Low-Power 8.5 mA Typical

Design Criteria	Value	Unit
Internal Gate Count *	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

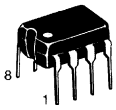
*Equivalent to a two-input NAND gate.

MAXIMUM RATINGS			
Characteristic	**Symbol**	**Range**	**Unit**
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to +7.0	Vdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Modulus Control Input, Pin 6	MC	–0.5 to +6.5	Vdc

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this hi-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

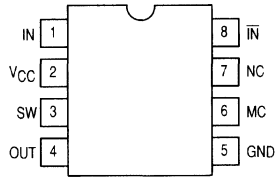
ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 Vdc, T_A = –40°C to +85°C)					
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Toggle Frequency (Sine Wave)	f_t	0.5	2.4	2.0	GHz
Supply Current Output Unloaded (Pin 2)	I_{CC}	—	8.5	12	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	—	—	V
Modulus Control Input Low (MC)	V_{IL1}	—	—	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	OPEN	OPEN	OPEN	—
Output Voltage Swing (C_L = 12 pF, R_L = 1.1 kΩ)	V_{out}	1.0	1.6	—	V_{p-p}
Modulus Setup Time MC to Out	t_{SET}	—	8.0	10	ns
Input Voltage Sensitivity 500–2000 MHz	V_{in}	100	—	1500	mVpp
Output Current (C_L = 12 pF, R_L = 1.1 kΩ)	I_O	—	—	3.5	mA

P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

PRESCALER
PIN ASSIGNMENT



(TOP VIEW)

Note 1:
For positive edge triggered synthesizers, order the MC12034A.
For negative edge triggered synthesizers, order the MC12034B.

FUNCTION TABLE		
SW	**MC**	**Divide Ratio**
H	H	32
H	L	33
L	H	64
L	L	65

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC}
L = Gnd to 0.8 V

6

LOGIC DIAGRAM (MC12034A)

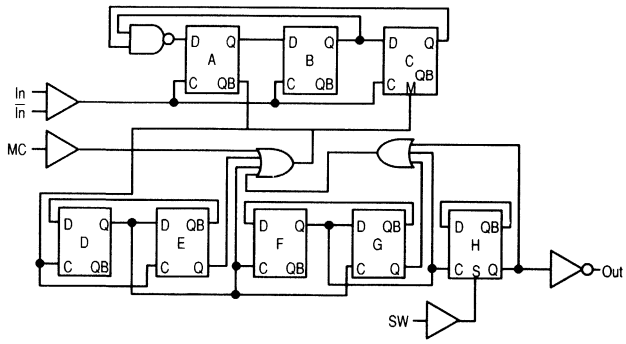
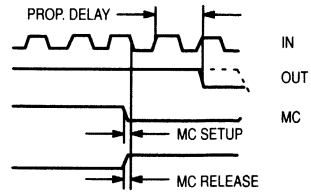


Figure 1. Modulus Setup Time



Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

Figure 2. Typical Output Waveform

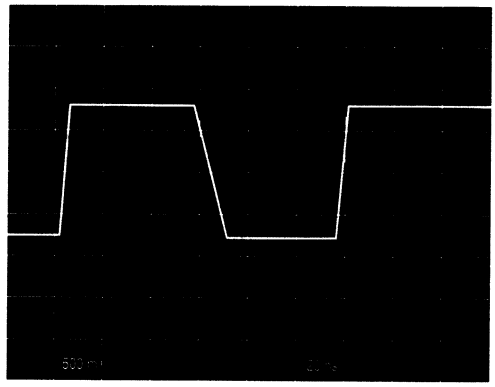
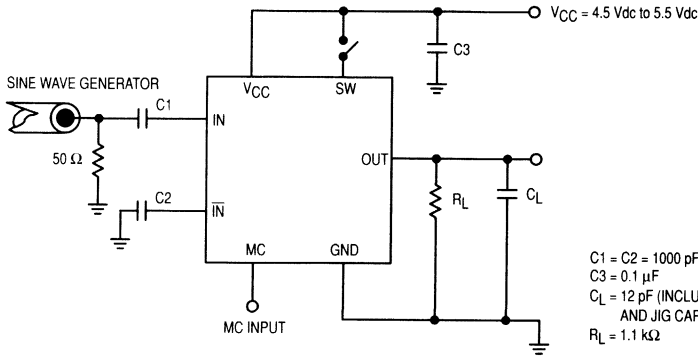


Figure 3. AC Test Circuit



C1 = C2 = 1000 pF
C3 = 0.1 μF
C_L = 12 pF (INCLUDING SCOPE AND JIG CAPACITANCE)
R_L = 1.1 kΩ

6

Figure 4A. Input Signal Amplitude versus Input Frequency
Divide Ratio = 65

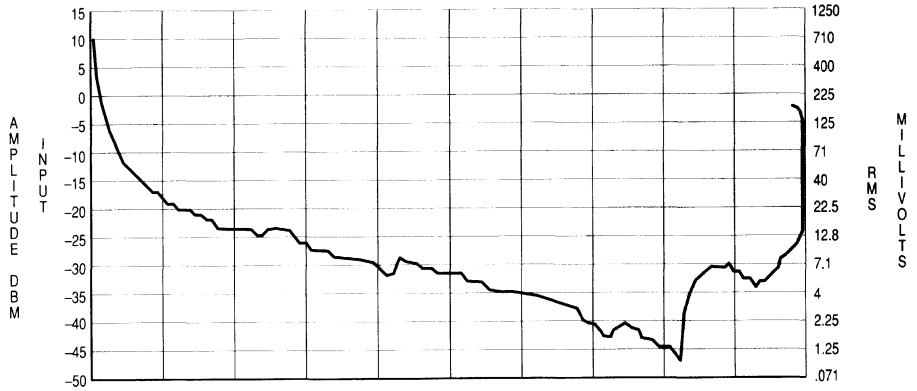
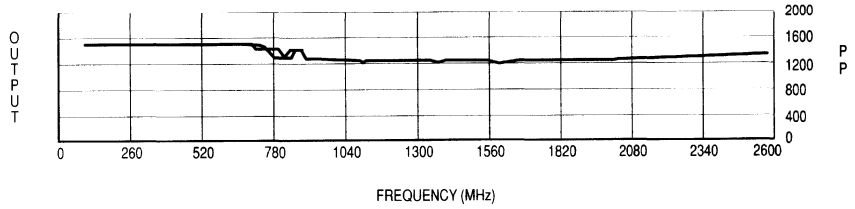


Figure 4B. Output Amplitude versus Input Frequency



6

MOTOROLA

MC12036A
MC12036B

1.1 GHz Dual Modulus Prescaler with Stand-By Mode

MECL PLL COMPONENTS

1.1 GHz
÷64/65, ÷128/129
DUAL MODULUS PRESCALER
WITH STAND-BY MODE

The MC12036A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

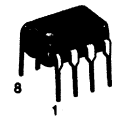
The MC12036B can be used with CMOS synthesizers requiring negative edges to trigger internal counters such as Fujitsu's MB87001.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- MC12036A for Positive Edge Triggered Synthesizers
- MC12036B for Negative Edge Triggered Synthesizers
- Modulus Control Input is Compatible with Standard CMOS and TTL
- Supply Voltage 4.5 Vdc to 5.5 Vdc
- Low-Power 4.0 mA Typical
- Low Standby Current of 0.5 mA Typical

P SUFFIX
PLASTIC PACKAGE
CASE 626

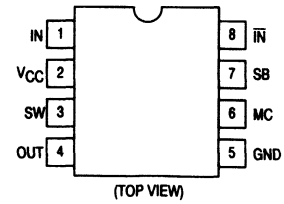


D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

Design Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

*Equivalent to a two-input NAND gate.

PRESCALER PIN ASSIGNMENT



(TOP VIEW)

Applying a Low to the Standby Pin 7 Disables the Device, Resulting in a Typical Current Draw of 0.5 mA

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 8	V_{CC}	–0.5 to +7.0	Vdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Modulus Control Input, Pin 6	MC	–0.5 to +6.5	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 Vdc, T_A = –40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current (Pin 2)	I_{CC}	—	4.0	6.5	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	—	—	V
Modulus Control Input Low (MC)	V_{IL1}	—	—	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	OPEN	OPEN	OPEN	—
Output Voltage Swing (C_L = 8 pF)	V_{out}	1.0	1.4	—	V_{p-p}
Modulus Setup Time MC to Out	t_{SET}	—	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	V_{in}	100 400	— —	1000 1000	mVpp
Standby Current	ISB	—	0.5	—	mA

FUNCTION TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H = V_{CC}, L = open
SB & MC: H = 2.0 V to V_{CC}
L = Gnd to 0.8 V

6

LOGIC DIAGRAM (MC12036A)

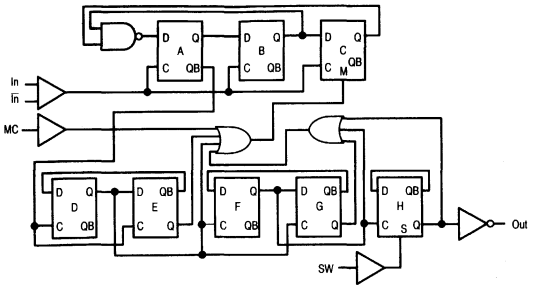
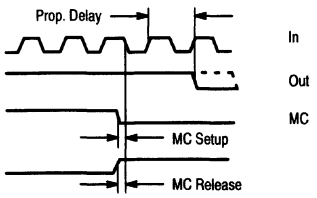


FIGURE 1 — MODULUS SETUP TIME



Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

FIGURE 2 — TYPICAL OUTPUT WAVEFORMS

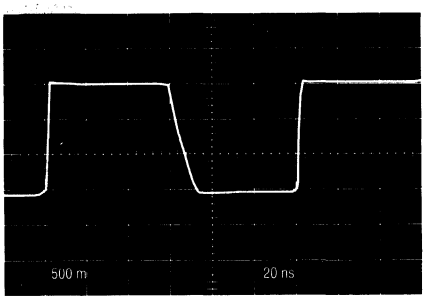


FIGURE 2A — ÷64, 500 MHz, 5.0 V, +25°C, OUTPUT LOADED

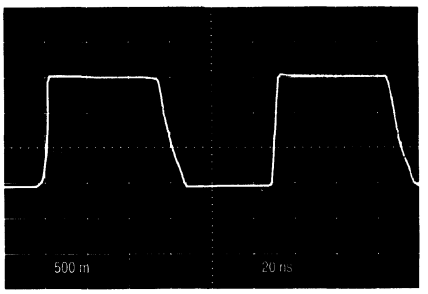
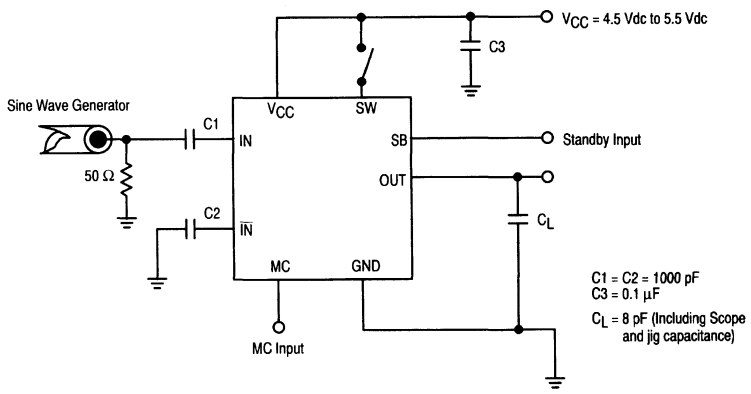


FIGURE 2B — ÷128, 1.1 GHz, 5.0 V, +25°C, OUTPUT LOADED

FIGURE 3 — AC TEST CIRCUIT



6

MOTOROLA

MC12040

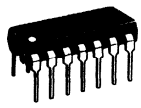
PHASE-FREQUENCY DETECTOR

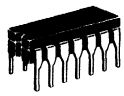
The MC12040 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is identical to that of Phase Detector #1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

Operating Frequency = 80 MHz typical

PHASE-FREQUENCY DETECTOR

P SUFFIX
PLASTIC PACKAGE
CASE 646

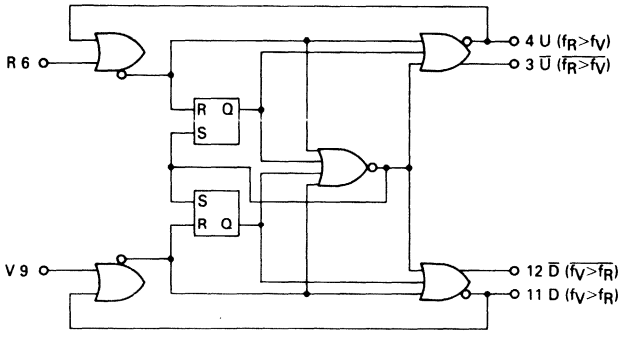




L SUFFIX
CERAMIC PACKAGE
CASE 632

FN SUFFIX
PLASTIC PACKAGE
CASE 775

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{EE} = Pin 7

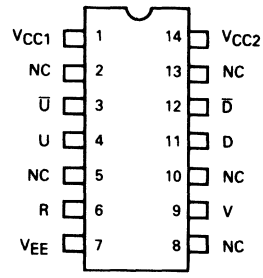
TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possible modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

INPUT		OUTPUT			
R	V	U	D	$\overline{U}$	$\overline{D}$
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	1

X = Don't Care

PIN ASSIGNMENT

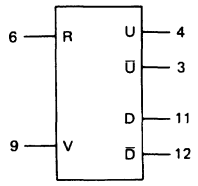


NC — No Connection

6

ELECTRICAL CHARACTERISTICS

The MC12040 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to +3.0 V for +5.0 V tests and through a 50 ohm resistor to −2.0 V for −5.2 V tests.



Supply Voltage = -5.2V

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
25°C	-0.810	-1.850	-1.105	-1.475	-5.2
75°C	-0.720	-1.830	-1.045	-1.450	-5.2

Characteristic	Symbol	Pin Under Test	MC12040 0°C Min	0°C Max	25°C Min	25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	7			-120	-60			mAdc					7	1,14
Input Current	I_{INH}	6 9				350 350			µAdc µAdc	6 9				7 7	1,14 1,14
Logic "1" Output Voltage	V_{OH} ①	3 4 11 12	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc					7	1,14
Logic "0" Output Voltage	V_{OL} ①	3 4 11 12	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc					7	1,14
Logic "1" Threshold Voltage	V_{OHA} ②	3 4 11 12	-1.020		-0.980		-0.920		Vdc			6.9		7	1,14
Logic "0" Threshold Voltage	V_{OLA} ②	3 4 11 12		-1.615		-1.600		-1.575	Vdc			9 6 9 6	6 9 6 9	7	1,14

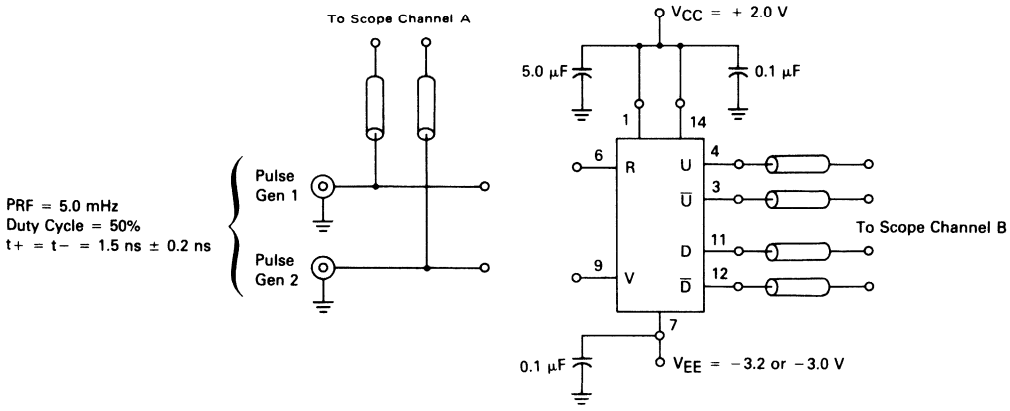
Supply Voltage = +5.0V

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{CC}
0°C	+4.160	+3.130	+3.855	+3.510	+5.0
25°C	+4.190	+3.150	+3.895	+3.525	+5.0
75°C	+4.280	+3.170	+3.955	+3.550	+5.0

Characteristic	Symbol	Pin Under Test	MC12040 0°C Min	0°C Max	25°C Min	25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{CC}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	7			-115	-60			mAdc					1,14	7
Input Current	I_{INH}	6 9				350 350			µAdc µAdc	6 9				1,14 1,14	7 7
Logic "1" Output Voltage	V_{OH} ①	3 4 11 12	4.000	4.160	4.040	4.190	4.100	4.280	Vdc					1,14	7
Logic "0" Output Voltage	V_{OL} ①	3 4 11 12	3.190	3.430	3.210	3.440	3.230	3.470	Vdc					1,14	7
Logic "1" Threshold Voltage	V_{OHA} ②	3 4 11 12	3.980		4.020		4.080		Vdc			6.9		1,14	7
Logic "0" Threshold Voltage	V_{OLA} ②	3 4 11 12		3.450		3.460		3.490	Vdc			9 6 9 6	6 9 6 9	1,14	7

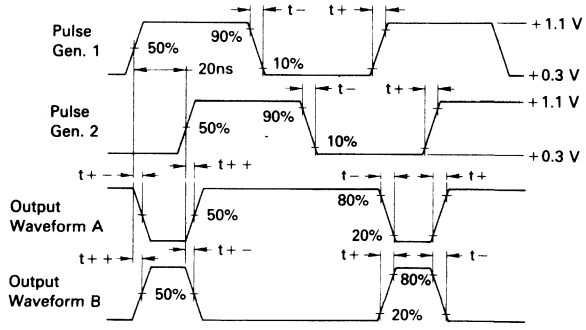
6

AC TESTS



NOTES:

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
2. Unused input and outputs are connected to a 50 Ω resistor to ground.
3. The device under test must be preconditioned before performing the ac tests. Preconditioning may be accomplished by applying pulse generator 1 for a minimum of two pulses prior to pulse generator 2. The device must be preconditioned again when inputs to pins 6 and 9 are interchanged. The same technique applies.



Characteristic	Symbol	Pin Under Test	Output Waveform	MC12040 0°C Max	MC12040 +25°C Max	MC12040 +75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	V_{EE} −3.0 or −3.2 V	V_{CC} +2.0 V
Propagation Delay	t_{6+4+}	6,4	B	4.6	4.6	5.0	ns	6	9	7	1,14
	t_{6+12+}	6,12	A	6.0	6.0	6.6		9	6		
	t_{6+3-}	6,3	A	4.5	4.5	4.9		6	9		
	t_{6+11-}	6,11	B	6.4	6.4	7.0		9	6		
	t_{9+11+}	9,11	B	4.6	4.6	5.0		9	6		
	t_{9+3+}	9,3	A	6.0	6.0	6.6		6	9		
	t_{9+12-}	9,12	A	4.5	4.5	4.9		9	6		
	t_{9+4-}	9,4	B	6.4	6.4	7.0		6	9		
Output Rise Time	t_{3+}	3	A	3.4	3.4	3.8	ns	6	9	7	1,14
	t_{4+}	4	B					6	9		
	t_{11+}	11	B					9	6		
	t_{12+}	12	A					9	6		
Output Fall Time	t_{3-}	3	A	3.4	3.4	3.8	ns	6	9	7	1,14
	t_{4-}	4	B					6	9		
	t_{11-}	11	B					9	6		
	t_{12-}	12	A					9	6		

APPLICATIONS INFORMATION

The MC12040 is a logic network designed for use as a phase comparator for MECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians.

Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 1), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (pin 11) would simply remain low.

On the other hand, it is also possible that V was leading R (Figure 1), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start-up. A stable phase-locked loop will result from either condition.

Phase error information is contained in the output duty cycle — that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage-controlled oscillator can be developed. A circuit useful for this function is shown in Figure 2.

Proper level shifting is accomplished by differentially driving the operational amplifier from the normally high outputs of the phase detector ($\overline{U}$ and $\overline{D}$). Using this technique the quiescent differential voltage to the operational amplifier is zero (assuming matched "1" levels from the phase detector). The $\overline{U}$ and $\overline{D}$ outputs are then used to pass along phase information to the operational amplifier. Phase error summing is accomplished through resistors R1 connected to the inputs of the operational amplifier. Some R-C filtering imbedded within the input network (Figure 2) may be very beneficial since the very narrow correctional pulses of the MC12040 would not normally be integrated by the amplifier. General design guides for calculating R1, R2, and C are included in the MC4044 data sheet. Phase detector gain for this configuration is approximately 0.16 volts/radian.

System phase error stems from input offset voltage in the operational amplifier, mismatching of nominally equal resistors, and mismatching of phase detector "high" states between the outputs used for threshold setting and phase measuring. All these effects are reflected in the gain constant. For example, a 16 mV offset voltage in the amplifier would cause an error of 0.016/0.16 = 0.1 radian or 5.7 degrees of error. Phase error can be trimmed to zero initially by trimming either input offset or one of the threshold resistors (R1 in Figure 2). Phase error over temperature depends on how much the offending parameters drift.

FIGURE 1 — TIMING DIAGRAM

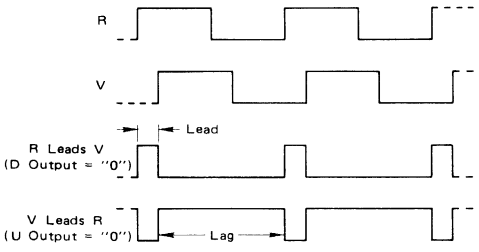
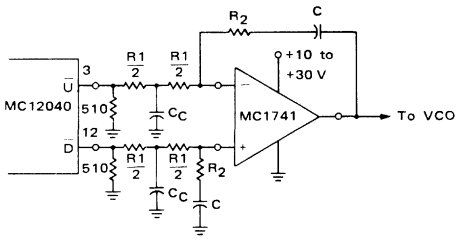


FIGURE 2 — TYPICAL FILTER AND SUMMING NETWORK



MOTOROLA

MC12052A/ MC12052B

MECL PLL COMPONENTS

1.1GHz ÷64/65, ÷128/129 Low Power Dual Modulus Prescaler

Advance Information

1.1GHz ÷64/65, ÷128/129 Low Power Dual Modulus Prescaler

The MC12052 is a low power dual modulus prescaler used in phase-locked loop applications. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 2.7mW at a minimum supply voltage of 2.7V.

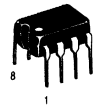
The MC12052A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1GHz in programmable frequency steps.

The MC12052B can be used with CMOS synthesizers requiring negative edges to trigger internal counters such as Fujitsu's MB87001.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1GHz Toggle Frequency
- The MC12052 is Pin and Functionally Compatible with the MC12022
- Low Power 1.0mA Typical
- 2.0mA Maximum, –40°C to +85°C, V_{CC} = 2.7–5.5 Vdc
- Short Setup Time (t_{set}) 16ns Maximum @ 1.1GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL. Maximum Input Voltage Should Be Limited to 6.5 Vdc



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to +7.0	Vdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Modulus Control Input, Pin 6	MC	–0.5 to +6.5	Vdc

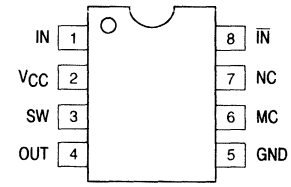
ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 VDC, T_A = –40°C to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	1.4	1.1	GHz
Supply Current (Pin 2)	I_{CC}	–	1.0	2.0	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC}	V
Modulus Control Input Low (MC)	V_{IL1}	GND	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC}	V_{CC}	V_{CC}	Vdc
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	–
Output Voltage Swing [2] (C_L = 8pF, R_L = 3.3kΩ)	V_{out}	0.8	1.1	–	V_{PP}
Modulus Setup Time MC to Out @ 1100MHz	t_{set}	–	11	16	ns
Input Voltage Sensitivity 250–1100MHz 100–250MHz	V_{in}	100 400	– –	1000 1000	mV_{PP}
Output Current [1] V_{CC} = 2.7V, C_L = 8pF, R_L = 3.3kΩ V_{CC} = 5.0V, C_L = 8pF, R_L = 7.2kΩ	I_O	 – –	 0.5 0.5	 3.0 3.0	mA

1. Divide ratio of ÷64/65 @ 1.1GHz
2. Valid over voltage range 2.7–5.5V; R_L = 3.3kΩ @ V_{CC} = 2.7V; R_L = 7.2kΩ @ V_{CC} = 5.0V

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN ASSIGNMENTS
(Top View)



Note:
For positive edge triggered synthesizers, order the MC12052A.
For negative edge triggered synthesizers, order the MC12052B.

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H = V_{CC}, L = Open
MC: H = 2.0V to V_{CC}, L = GND to 0.8V

6

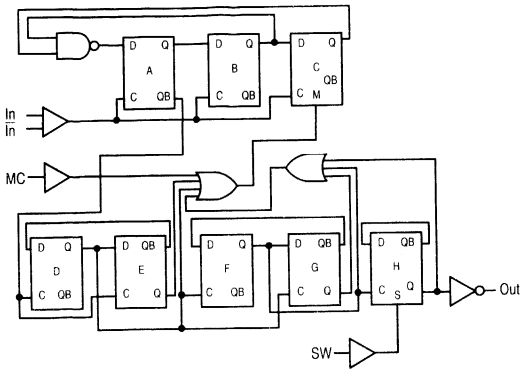
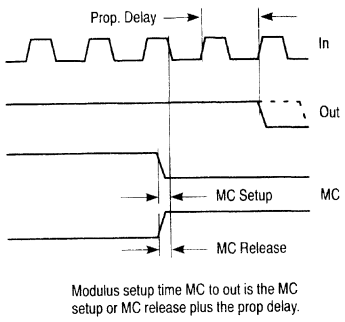


Figure 1. Logic Diagram (MC12052A)



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 2. Modulus Setup Time

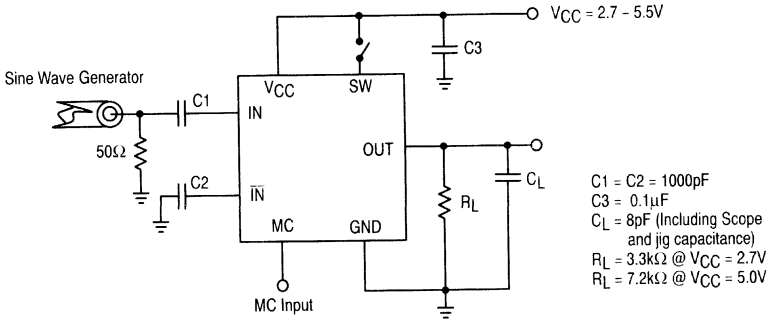


Figure 3. AC Test Circuit

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MOTOROLA

MC12061

CRYSTAL OSCILLATOR

The MC12061 is for use with an external crystal to form a crystal controlled oscillator. In addition to the fundamental series mode crystal, two bypass capacitors are required (plus usual power supply pin bypass capacitors). Translators are provided internally for MECL and TTL outputs.

- Frequency Range = 2.0 MHz to 20 MHz
- Temperature Range = 0°C to +70°C
- Single Supply Operation: +5.0 Vdc or −5.2 Vdc
- Three Outputs Available:
  1. Complementary Sine Wave (600 mVp-p typ)
  2. Complementary MECL
  3. Single Ended TTL

CRYSTAL OSCILLATOR

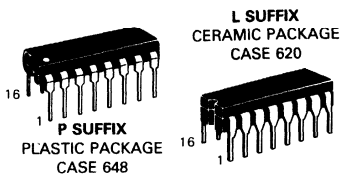
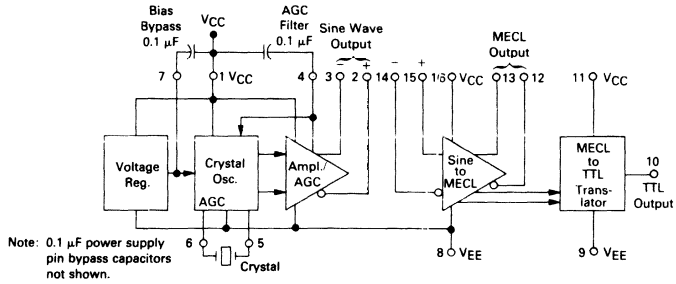


FIGURE 1—BLOCK DIAGRAM



TYPICAL CIRCUIT CONFIGURATIONS Note: 0.1 µF power supply pin bypass capacitors not shown.

FIGURE 2 — SINE WAVE OUTPUT

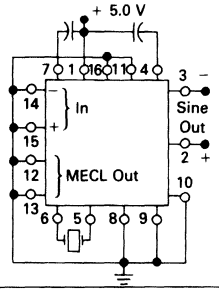


FIGURE 3 — MTTL OUTPUT

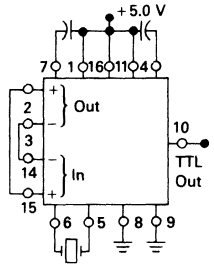


FIGURE 4 — MECL OUTPUT (+5.0 V Supply)

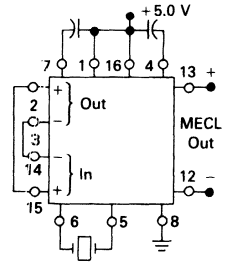
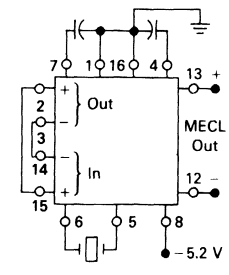


FIGURE 5 — MECL OUTPUT (−5.2 V Supply)

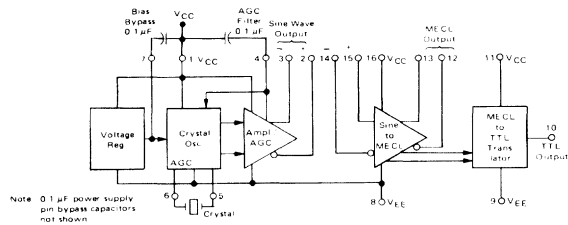


CRYSTAL REQUIREMENTS

Note: Start-up stabilization time is a function of crystal series resistance. The lower the resistance, the faster the circuit stabilizes.

Characteristic	MC12061
Mode of Operation	Fundamental Series Resonance
Frequency Range	2.0 MHz — 20 MHz
Series Resistance, R1	Minimum at Fundamental
Maximum Effective Resistance $R_{E(max)}$	155 ohms

6



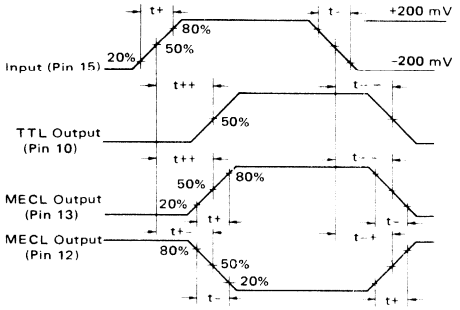
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES										
	Volts								mA		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{CCL}	V_{CC}	V_{CCH}	I_{OL}	I_{OH}	I_L
0°C	4.16	3.19	3.86	3.51	4.0	4.75	5.0	5.25	16	−0.4	−2.5
+25°C	4.19	3.21	3.9	3.52	4.0	4.75	5.0	5.25	16	−0.4	−2.5
+75°C	4.28	3.23	3.96	3.55	4.0	4.75	5.0	5.25	16	−0.4	−2.5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{CCL}	V_{CC}	V_{CCH}	I_{OL}	I_{OH}	I_L	Gnd
Power Supply Drain Current	I_{CC}	1	—	—	13	16	19	—	—	mAdc	—	—	—	—	–	—	1	—	—	—	—	8
		1	—	—	18	23	28	—	—		—	—	—	—	—	—	1	—	—	—	—	8
		11	—	—	—	3.0	4.0	—	—		14	15	—	—	—	—	11,16	—	—	—	—	8,9
		16	—	—	13	16	19	—	—		—	—	—	—	—	—	16	—	—	—	—	8
Input Current	I_{INH}	14	—	—	—	—	250	—	—	µAdc	14	15	—	—	—	—	16	—	—	—	—	8
		15	—	—	—	—	250	—	—	µAdc	15	14	—	—	—	—	16	—	—	—	—	8
	I_{INL}	14	—	—	—	—	1.0	—	—	µAdc	15	—	—	—	—	—	16	—	—	—	—	8,14
		15	—	—	—	—	1.0	—	—	µAdc	14	—	—	—	—	—	16	—	—	—	—	8,15
Differential Offset Voltage	ΔV	4 to 7	—	—	40	—	325	—	—	mVdc	—	—	—	—	5,6	—	1	—	—	—	—	8
		2 to 3	—	—	−200	0	+200	—	—		—	—	—	—	4	—		—	—	—	—	
Output Voltage Level	V_{out}	2	—	—	—	3.5	—	—	—	Vdc	—	—	—	—	4	—	1	—	—	—	—	8
		3	—	—	—	3.5	—	—	—	Vdc	—	—	—	—	4	—	1	—	—	—	—	8
Logic "1" Output Voltage	V_{OH1}*	12	4.0	4.16	4.04	—	4.19	4.1	4.28	Vdc	14	15	—	—	—	—	16	—	—	—	12	8
		13	4.0	4.16	4.04	—	4.19	4.1	4.28	Vdc	15	14	—	—	—	—	16	—	—	—	13	8
	V_{OH2}	10	2.4	—	2.4	—	—	2.4	—	Vdc	15	14	—	—	—	11,16	—	—	—	10	—	8,9
Logic "0" Output Voltage	V_{OL1}*	12	2.98	3.43	3.0	—	3.44	3.02	3.47	Vdc	15	14	—	—	—	—	16	—	—	—	12	8
		13	2.98	3.43	3.0	—	3.44	3.02	3.47	Vdc	14	15	—	—	—	—	16	—	—	—	13	8
	V_{OL2}	10	—	0.5	—	—	0.5	—	0.5	Vdc	14	15	—	—	—	11,16	—	—	10	—	—	8,9
		10	—	0.5	—	—	0.5	—	0.5	Vdc	14	15	—	—	—	—	—	11,16	10	—	—	8,9
Logic "1" Threshold Voltage	V_{OHA}	12	3.98	—	4.02	—	—	4.08	—	Vdc	—	—	14	15	—	—	16	—	—	—	12	8
		13	3.98	—	4.02	—	—	4.08	—	Vdc	—	—	15	14	—	—	16	—	—	—	13	8
Logic "0" Threshold Voltage	V_{OLA}	12	—	3.45	—	—	3.46	—	3.49	Vdc	—	—	15	14	—	—	16	—	—	—	12	8
		13	—	3.45	—	—	3.46	—	3.49	Vdc	—	—	14	15	—	—	16	—	—	—	13	8
Output Short-Circuit Current	I_{OS}	10	20	60	20	—	60	20	60	mAdc	15	14	—	—	—	11,16	—	—	—	—	—	8,9, 10

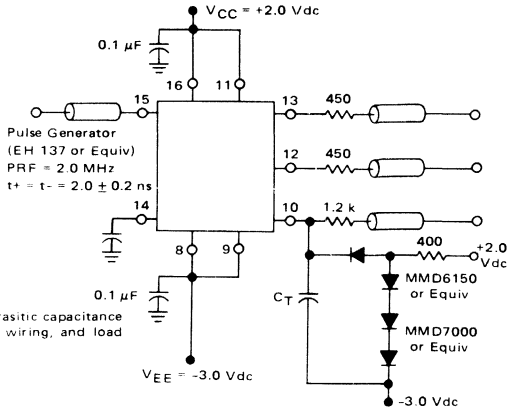
*Devices will meet standard MECL logic levels using V_{EE} = −5.2 Vdc and V_{CC} = 0.

FIGURE 6 — AC CHARACTERISTICS — MECL AND TTL OUTPUTS



All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Unused outputs are connected to a 50 Ω ±1% resistor to ground.

C_T = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.



Characteristic	Symbol	Pin Under Test	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse In	Pulse Out	+2.0 Vdc	−3.0 Vdc	Gnd
Propagation Delay	t_{15+10+}	10	—	22	—	17	25	—	27	ns	15	10	11,16	8,9	14
	t_{15-10-}	10	—	19	—	12	18	—	18			10			
	t_{15+12-}	12	—	5.2	—	4.3	5.5	—	5.8			12			
	t_{15-12+}	12	—	5.0	—	3.7	5.2	—	5.2			12			
	t_{15+13+}	13	—	4.8	—	4.0	5.0	—	5.2			13			
	t_{15-13-}	13	—	5.0	—	4.0	5.0	—	5.1			13			
Rise Time	t_{12+}	12	—	4.0	—	3.0	4.0	—	4.4	ns	15	12	11,16	8,9	14
	t_{13+}	13	—	4.0	—	3.0	4.0	—	4.4	ns	15	13	11,16	8,9	14
Fall Time	t_{12-}	12	—	4.0	—	3.0	4.0	—	4.0	ns	15	12	11,16	8,9	14
	t_{13-}	13	—	4.0	—	3.0	4.0	—	4.0	ns	15	13	11,16	8,9	14

Characteristic	Pin Under Test	+25°C Min	+25°C Typ	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW +2.0 Vdc	−3.0 Vdc
Sine Wave Amplitude	2	650	750	mVp-p	1	8, 9
	3	650	750			

FIGURE 7 — AC TEST CIRCUIT — SINE WAVE OUTPUT

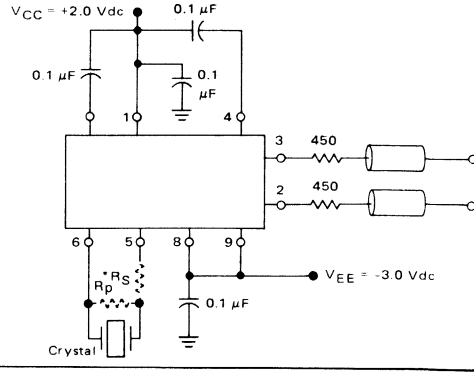
All output cables to the scope are equal lengths of 50 Ω coaxial cable. All unused cables must be terminated with a 50 Ω ± 1% resistor to ground.

450 Ω resistor and the scope termination impedance constitute a 10:1 attenuator probe.

Crystal — Reeves Hoffman Series Mode,
Series Resistance Minimum at Fundamental
f = 10 MHz
R_E = 5 Ω

*R_S = 15 kΩ is inserted only for test purposes. When used with the above specified crystal, it guarantees oscillation with any crystal which has an equivalent series resistance ≤ 155 Ω

R_p: will improve start up problems value: 200–500 Ω



6

OPERATING CHARACTERISTICS

The MC12061 consists of three basic sections: an oscillator with AGC and two translators (Figure 1). Buffered complementary sine wave outputs are available from the oscillator section. The translators convert these sine wave outputs to levels compatible with MECL and/or TTL.

Series mode crystals should be used with the oscillator. If it is necessary or desirable to adjust the crystal frequency, a reactive element can be inserted in series with the crystal — an inductor to lower the frequency or a capacitor to raise it. When such an adjustment is necessary, it is recommended that the crystal be specified slightly lower in frequency and a series trimmer capacitor be added to bring the oscillator back on frequency. As the oscillator frequency is changed from the natural resonance of the crystal, more and more dependence is placed on the external reactance, and temperature drift of the trimming components then affects overall oscillator performance.

The MC12061 is designed to operate from a single supply — either +5.0 Vdc or −5.2 Vdc. Although each translator has separate V_{CC} and V_{EE} supply pins, the circuit is NOT designed to operate from both voltage levels at the same time. The separate V_{EE} pin from the TTL translator helps minimize transient disturbance. If neither translator is being used, all unused pins (9 thru 16) should be connected to V_{EE} (pin 8). With the translators not powered, supply current drain is typically reduced from 42 mA to 23 mA for the MC12061.

Frequency Stability

Output frequency of different oscillator circuits (of a given device type number) will vary somewhat when used with a given test setup. However, the variation should be within approximately ±0.001% from unit to unit.

Frequency variations with temperature (independent of the crystal, which is held at 25°C) are small — about −0.08 ppm/°C for MC12061 operating at 8.0 MHz (see Figure 8).

Signal Characteristics

The sine wave outputs at either pin 2 or pin 3 will typically range from 800 mVp-p (no load) to 500 mVp-p (120 ohm ac load). Approximately 500 mVp-p can be provided across 50 ohms by slightly increasing the dc current in the output buffer by the addition of an external resistor (680 ohms) from pin 2 or 3 to ground, as shown in Figure 9. Frequency drift is typically less than 0.0003% when going from a high-impedance load (1 megohm, 15 pF) to the 50 ohm load of Figure 9. The dc voltage level at pin 2 or 3 is nominally 3.5 Vdc with V_{CC} = +5.0 Vdc.

Harmonic distortion content in the sine wave outputs is crystal as well as circuit dependent. The largest harmonic (third) will usually be at least 15 dB down from the fundamental. The harmonic content is approximately load independent except that the higher harmonic levels (greater than the fifth) are increased when the MECL translator is being driven.

Typically, the MECL outputs (pins 12 and 13) will drive up to five gates, as defined in Figure 10, and the TTL output (pin 10) will drive up to ten gates, as defined in Figure 11.

Noise Characteristics

Noise level evaluation of the sine wave outputs using the circuit of Figure 12, with operation at 9.0 MHz, indicates the following characteristics:

1. Noise floor (200 kHz from oscillator center frequency) is approximately −122 dB when referenced to a 1.0 Hz bandwidth. Noise floor is not sensitive to load conditions and/or translator operation.
2. Close-in noise (100 Hz from oscillator center frequency) is approximately −88 dB when referenced to a 1.0 Hz bandwidth.

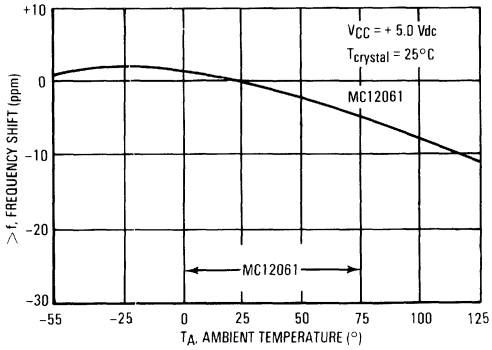


FIGURE 9 — DRIVING LOW-IMPEDANCE LOADS

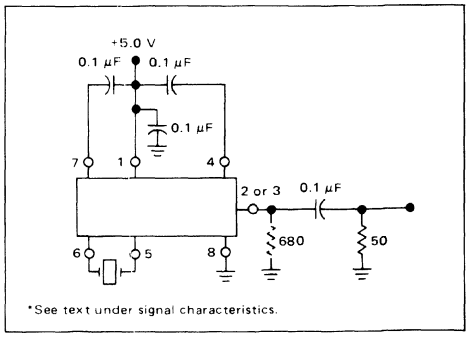


FIGURE 10 — MECL TRANSLATOR LOAD CAPABILITY

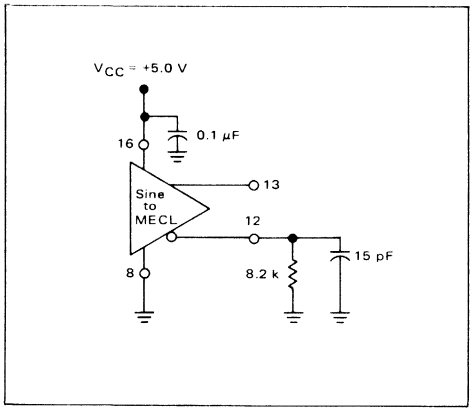


FIGURE 11 — TTL TRANSLATOR LOAD CAPABILITY

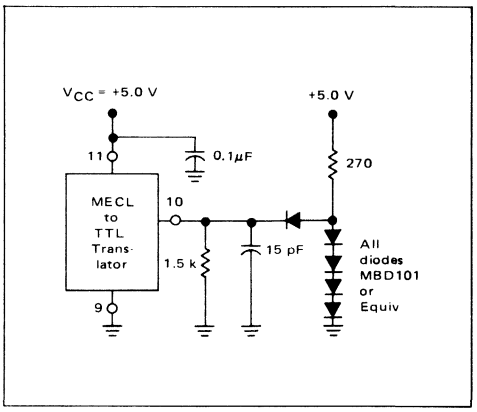
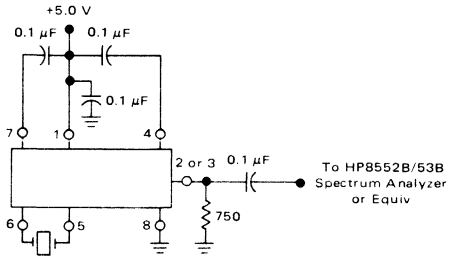


FIGURE 12 — NOISE MEASUREMENT TEST CIRCUIT

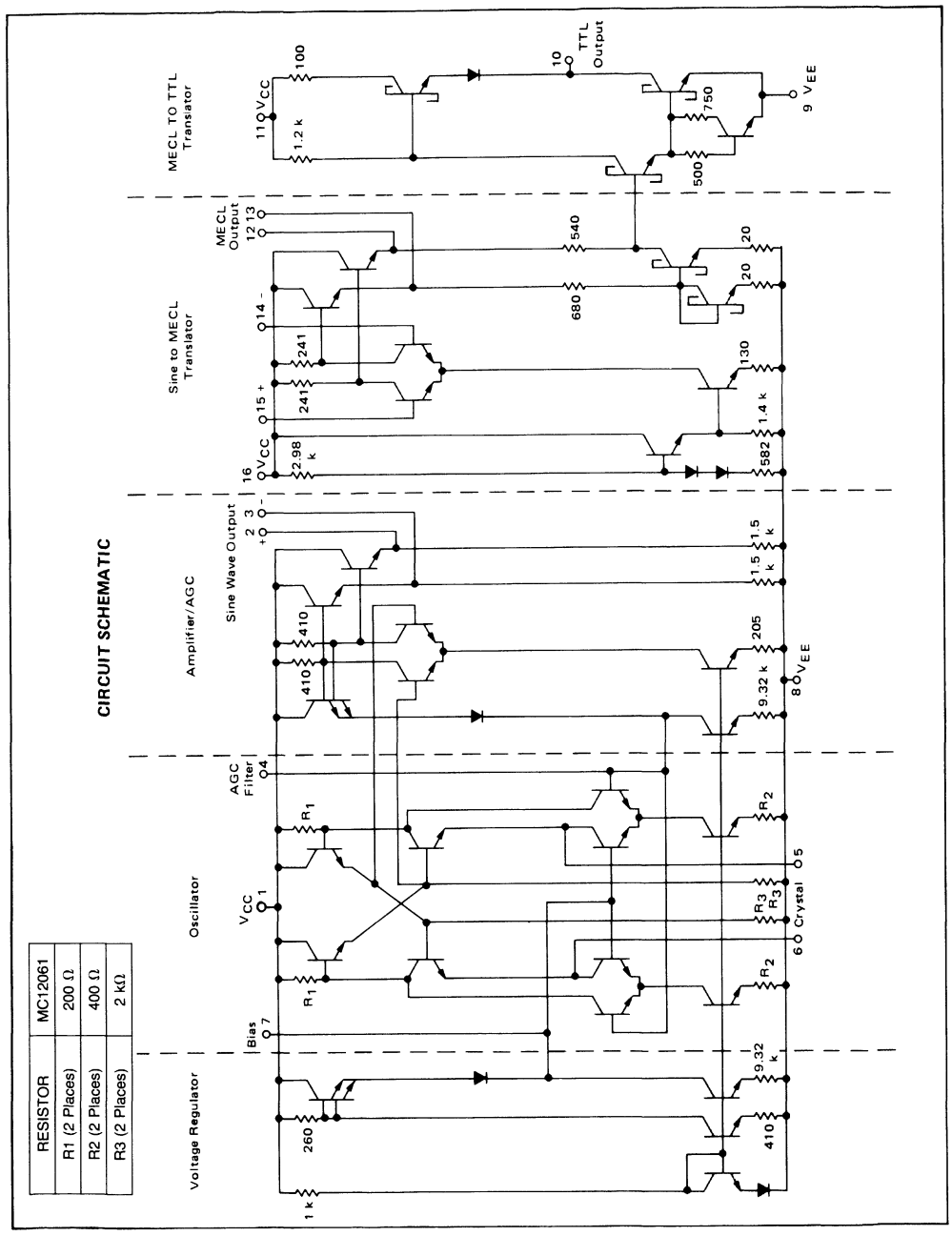


ANALYZER SETTING

Measurement	Sweep	Bandwidth	Video Filter
Noise Floor	50 kHz/div	10 kHz	10 Hz
Close-In Noise	20 kHz/div	10 Hz	10 Hz

6

CIRCUIT SCHEMATIC



RESISTOR	MC12061
R1 (2 Places)	200 Ω
R2 (2 Places)	400 Ω
R3 (2 Places)	2 kΩ

MOTOROLA

MC12073

MECL PLL COMPONENTS

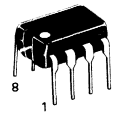
1.1 GHz
÷64
PRESCALER

1.1 GHz PRESCALER

The MC12073 is a divide by 64 prescaler. Typical frequency synthesis applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included which isolates the differential inputs and provides gain for the input signal. Differential ECL outputs are provided.

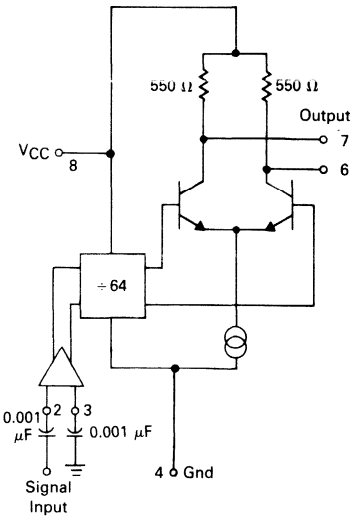
- 1.1 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5 V
- Low Power 23 mA Typical @ V_{CC} = 5.0 V
- High Input Sensitivity, 20 mVrms @ V_{CC} = 5.0 ± 10%, T_A = 0° to +70°C
- 800 mV Minimum Peak-to-Peak Output Swing
- Differential ECL Outputs



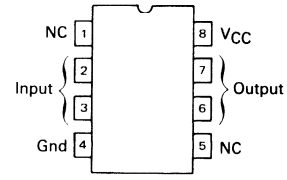
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751

PRESCALER BLOCK DIAGRAM



PRESCALER PINOUT



MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

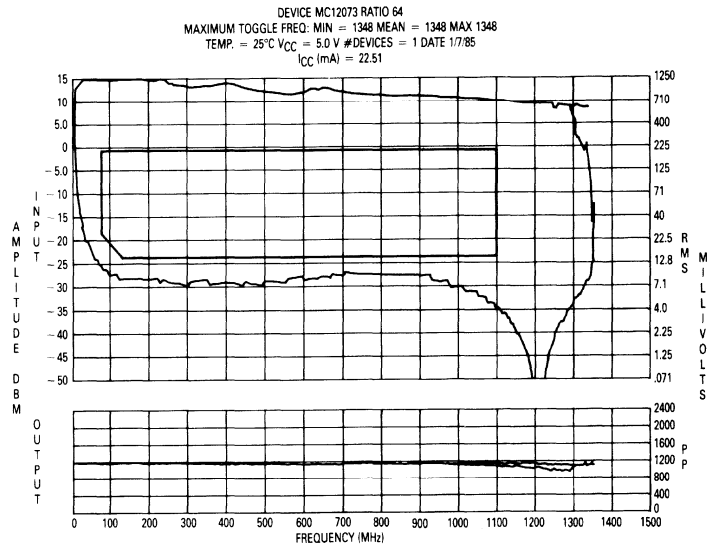
ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = 0°C to +70°C)

Characteristic	Symbol	Min	Typ*	Max	Unit
Toggle Frequency (Sine wave input)	f_{max}[1]	1.1	1.3	—	GHz
Minimum Frequency	f_{min}	—	—	90	MHz
Supply Current	I_{CC}	—	23	30	mA
Output Voltage (Load = 10 pF)	V_{out}	0.8	1.2	—	V_{pp}
Input Voltage Sensitivity @ 150–1100 MHz	V_{in} Min	—	10	20	mV_{rms}
Input Voltage Sensitivity @ 90 MHz	V_{in} Min	—	—	30	mV_{rms}
Input Overload	V_{in} Max	200	400	—	mV_{rms}

*Typical measured at +25°C, 5.0 V
[1]See Figure 1

6

FIGURE 1


DEVICE MC12073 RATIO 64
MAXIMUM TOGGLE FREQ: MIN = 1348 MEAN = 1348 MAX 1348
TEMP. = 25°C VCC = 5.0 V #DEVICES = 1 DATE 1/7/85
ICC (mA) = 22.51
AMPLITUDE DBM
INPUT
OUTPUT
RMS MILLIVOLTS
PP
FREQUENCY (MHz)

MOTOROLA

MC12074

MECL PLL COMPONENTS

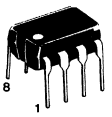
1.1 GHz
÷256
PRESCALER

1.1 GHz PRESCALER

The MC12074 is a divide by 256 prescaler. Typical frequency synthesis applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included which isolates the differential inputs and provides gain for the input signal. Differential ECL outputs are provided.

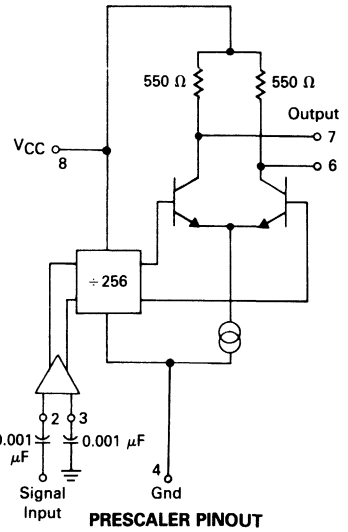
- 1.1 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5 V
- Low Power 23 mA Typical @ V_{CC} = 5.0 V
- High Input Sensitivity, 20 mVrms @ V_{CC} = 5.0 ± 10%, T_A = 0° to +70°C
- 800 mV Minimum Peak-to-Peak Output Swing
- Differential ECL Outputs



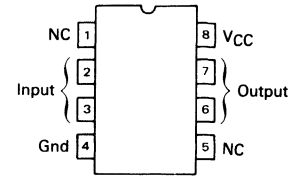
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751

PRESCALER BLOCK DIAGRAM



PRESCALER PINOUT



MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = 0°C to +70°C)

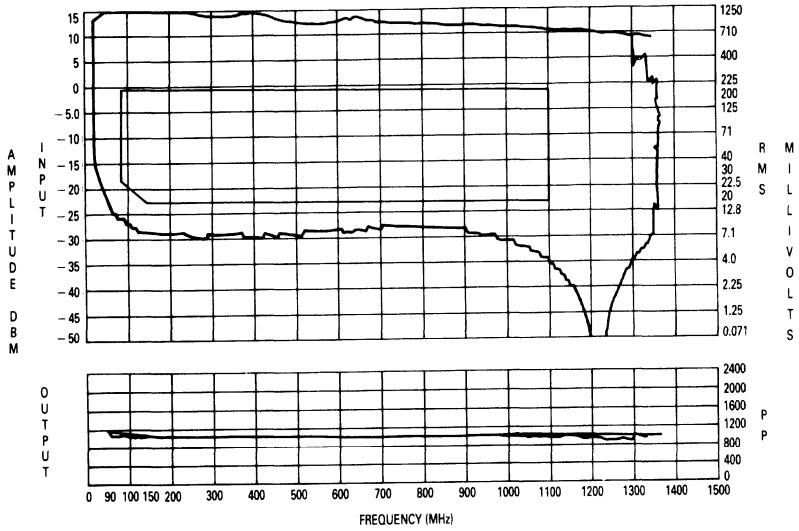
Characteristic	Symbol	Min	Typ*	Max	Unit
Toggle Frequency (Sine wave input)	f_{max}[1]	1.1	1.3	—	GHz
Minimum Frequency	f_{min}	—	—	90	MHz
Supply Current	I_{CC}	—	23	30	mA
Output Voltage (Load = 10 pF)	V_{out}	0.8	1.2	—	V_{pp}
Input Voltage Sensitivity @ 150–1100 MHz	V_{in} Min	—	10	20	mV_{rms}
Input Voltage Sensitivity @ 90 MHz	V_{in} Min	—	—	30	mV_{rms}
Input Overload	V_{in} Max	200	400	—	mV_{rms}

*Typical measured at +25°C, 5.0 V [1]See Figure 1

6

FIGURE 1

DEVICE MC12074 — RATIO 256
MAXIMUM TOGGLE FREQ: MIN = 1357 MEAN = 1357 MAX 1357
TEMP. = 25°C V_{CC} = 5.0 V + DEVICES = 1



6

MOTOROLA

MC12076

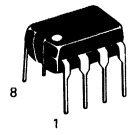
MECL PLL COMPONENTS
1.3 GHz
÷256
PRESCALER

1.3 GHz Prescaler

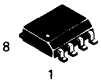
The MC12076 is a divide by 256 prescaler. Typical frequency synthesis applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included which isolates the differential inputs and provides gain for the input signal. Differential ECL outputs are provided.

- 1.3 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5 V
- Low Power 36 mA Typical @ V_{CC} = 5.0 V
- Operating Temperature Range of 0°C to +85°C
- High Input Sensitivity
- 800 mV Minimum Peak-to-Peak Output Swing
- Differential ECL Outputs

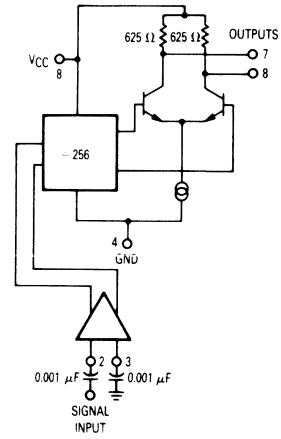


P SUFFIX
PLASTIC PACKAGE
CASE 626

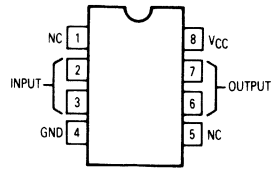


D SUFFIX
SOIC PACKAGE
CASE 751

BLOCK DIAGRAM



PIN ASSIGNMENT



Design Criteria	Value	Unit
Internal Gate Count*	62	ea
Internal Gate Propagation Delay	250	ps
Internal Gate Power Dissipation	10	mW
Speed Power Product	2.5	pJ

*Equivalent to a two-input NAND gate.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Operating Temperature Range	T_A	0 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = 0°C to +85°C)

Characteristic	Symbol	Min	Typ*	Max	Unit
Toggle Frequency (Sine Wave Input)	f_{max} (1)	1.3	1.6	—	GHz
Minimum Frequency	f_{min}	—	—	70	MHz
Supply Current	I_{CC}	—	36	50	mA
Output Voltage (Load = 10 pF)	V_{out}	0.8	1.2	—	V_{p-p}
Input Voltage Sensitivity @	V_{in} Min				mVrms
70 MHz		—	10	20	
150 to 1100 MHz		—	1.0	4.0	
1.2 GHz		—	1.5	15	
1.3 GHz		—	3.0	20	
Input Overload 70 to 1300 MHz	V_{in} Max	400	—	—	mVrms

*Typical measured @ +25°C, 5.0 V
(1) See Figure 1

6

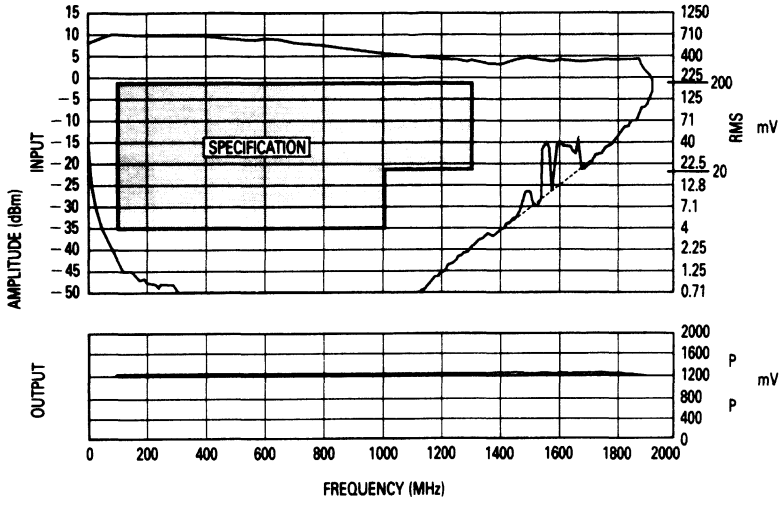


Figure 1. MC12076 Input Signal Amplitude versus Input Frequency

6

MOTOROLA

MC12078

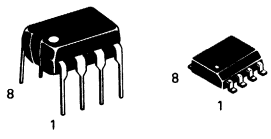
MECL PLL COMPONENTS
1.3 GHz
÷256
PRESCALER

1.3 GHz Prescaler

The MC12078 is a divide by 256 prescaler. Typical frequency synthesis applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included which isolates the differential inputs and provides gain for the input signal. Differential ECL outputs are provided.

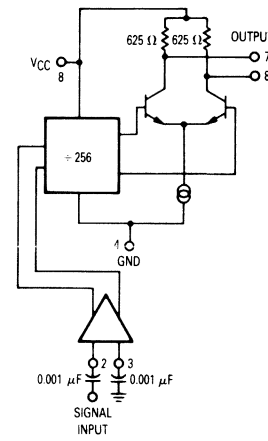
- 1.3 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5 V
- Low Power 28 mA Typical @ V_{CC} = 5.0 V
- Operating Temperature Range of 0°C to +85°C
- High Input Sensitivity
- 800 mV Minimum Peak-to-Peak Output Swing
- Differential ECL Outputs



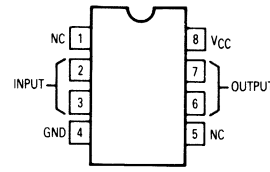
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
SOIC PACKAGE
CASE 751

BLOCK DIAGRAM



PIN ASSIGNMENT



Design Criteria	Value	Unit
Internal Gate Count*	62	ea
Internal Gate Propagation Delay	250	ps
Internal Gate Power Dissipation	10	mW
Speed Power Product	2.5	pJ

*Equivalent to a two-input NAND gate.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Operating Temperature Range	T_A	0 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = 0°C to +85°C)

Characteristic	Symbol	Min	Typ*	Max	Unit
Toggle Frequency (Sine Wave Input)	f_{max} (1)	1.3	1.6	—	GHz
Minimum Frequency	f_{min}	—	—	90	MHz
Supply Current	I_{CC}	—	28	35	mA
Output Voltage (Load = 10 pF)	V_{out}	0.8	1.2	—	V_{p-p}
Input Voltage Sensitivity @	V_{in} Min				mVrms
90 MHz		—	10	20	
150 to 1100 MHz		—	4.0	10	
1.3 GHz		—	7.0	20	
Input Overload	V_{in} Max				mVrms
90 to 500 MHz		400	—	—	
500 to 1300 MHz		400	—	—	

*Typical measured @ +25°C, 5.0 V
(1) See Figure 1

6

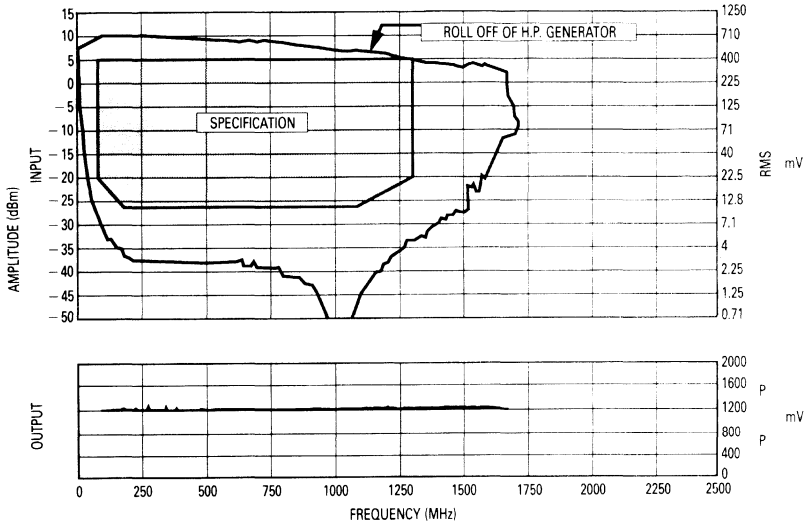


Figure 1. MC12078 Input Signal Amplitude versus Input Frequency

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MOTOROLA

MC12090

PLL COMPONENTS

750 MHz ÷2
UHF PRESCALER

750 MHz UHF PRESCALER

The MC12090 is a high-speed D master-slave flip-flop capable of toggle rates of over 700 MHz. It was designed primarily for high-speed prescaling applications in communications and instrumentation. This device employs two data inputs, two clock inputs as well as complementary Q and $\overline{Q}$ outputs. There are no SET or RESET inputs.

P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

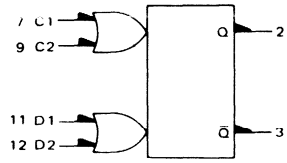
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	65	—	59	—	65	mA
Input Current High Pin 7, 9 Pin 11, 12	I_{inH}	 — —	 400 435	 — —	 260 280	 — —	 260 280	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.70	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.87	-1.495	-1.85	-1.48	-1.83	-1.45	Vdc

AC PARAMETERS

Characteristic	Symbol	−30°C		0°C		25°C		75°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Toggle Frequency	f_{tog}	500	—	700	—	750	—	700	—	500	—	MHz
		Typical (25°C)										
Propagation Delay (Clock to Output Pins 7 & 9→2)	t_{pd}	1.3										ns
Setup Time $t_{setup\ H}$ $t_{setup\ L}$	t_s	 0.3 0.3										ns
Hold Time $t_{hold\ H}$ $t_{hold\ L}$	t_h	 0.3 0.3										ns
Rise Time	t_r	0.9										ns
Fall Time	t_f	0.9										ns

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	ϕ	Q_n
↓	L	L
↓	H	H

C = C1 + C2
D = D1 + D2
ϕ = Don't Care

6

FIGURE 1 — GUARANTEED RANGE OF OPERATION
(TEMP = 75°C, # DEVICES = FIVE;
V_{CC} = 2.0 V, V_{EE} = -3.2 V, V_{BIAS} = 0.710 V)

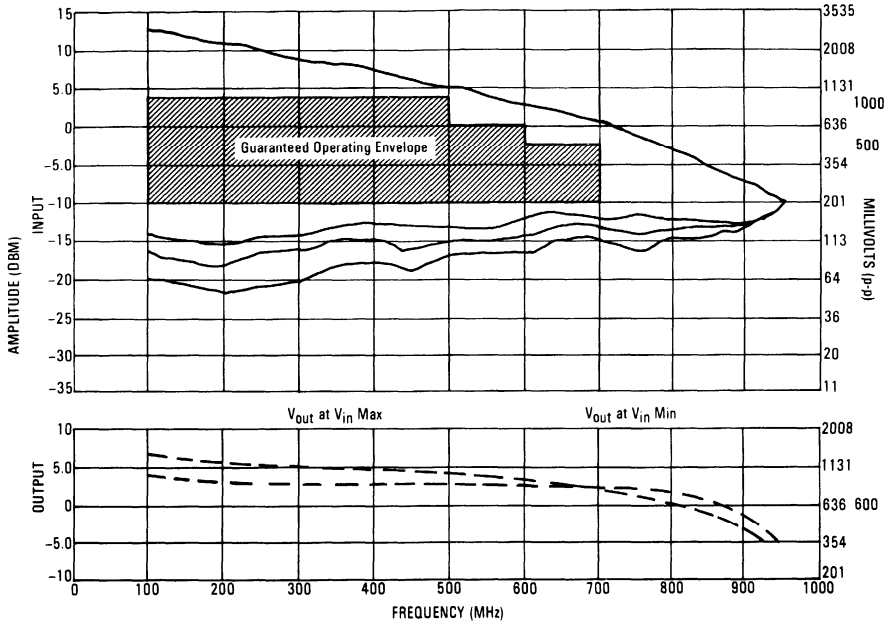
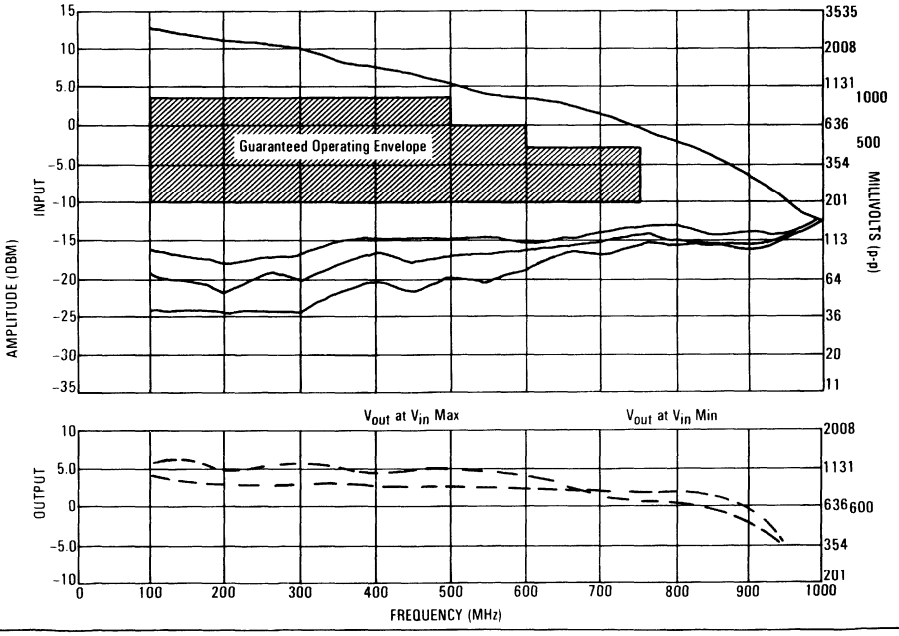


FIGURE 2 — GUARANTEED RANGE OF OPERATION
(TEMP = 25°C, # DEVICES = FIVE;
V_{CC} = 2.0 V, V_{EE} = -3.2 V, V_{BIAS} = 0.710 V)



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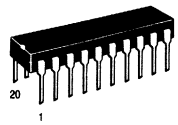
MOTOROLA

MC12100

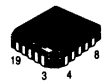
200MHz Voltage Controlled Multivibrator

200MHz VOLTAGE CONTROLLED MULTIVIBRATOR

- High Frequency VCM Ideal for PLL Applications
- Single External Resistor Determines Center Frequency; Additional Resistor Determines f/V Sensitivity
- Internal Ripple Counter (1/2, 1/4, 1/8) For Low Frequency Applications – TTL/ECL Outputs
- VCO Output Enable Pins (TTL/ECL Level)
- +5.0V Single Supply Voltage
- Packages: DIP, PLCC

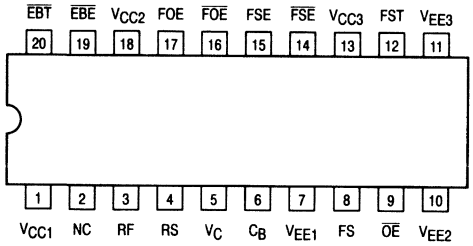


P SUFFIX
PLASTIC DIP PACKAGE
CASE 738-03

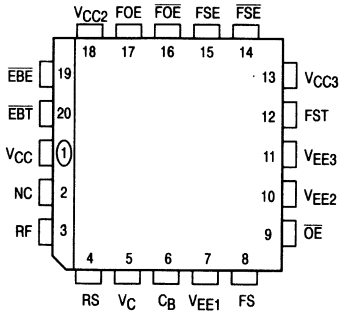


FN SUFFIX
PLCC PACKAGE
CASE 775-02

Pinout: 20-Lead Plastic Package (Top View)



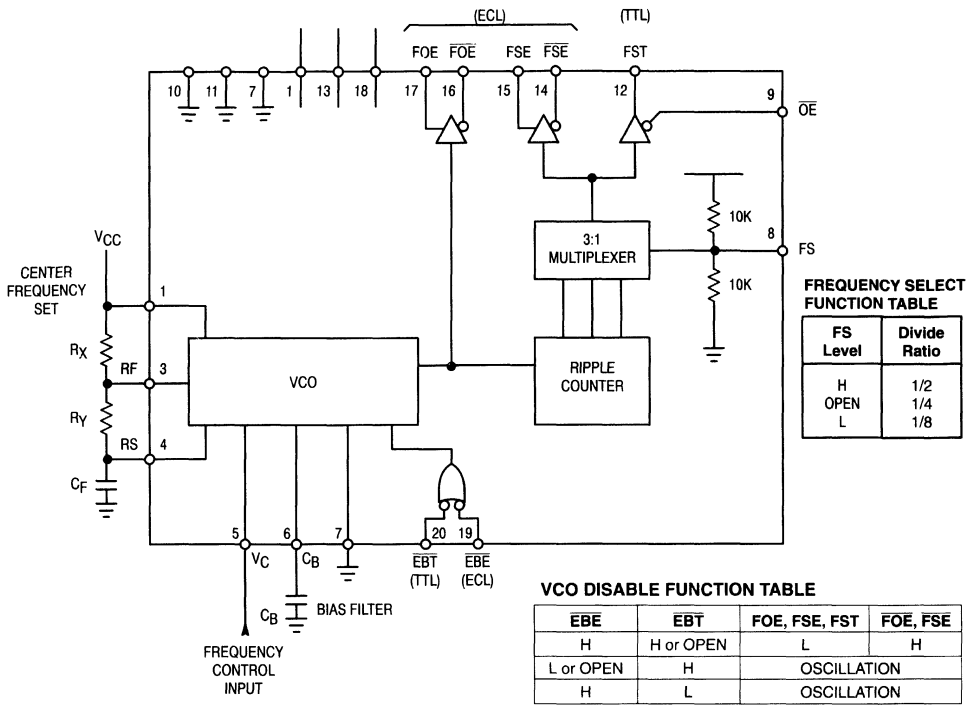
Pinout: 20-Lead PLCC Package (Top View)



PIN NAMES

Pin	Function
RF, RS	Center Frequency Inputs
V_C	Frequency Control Input
C_B	Bias Filter Input
FS	Frequency Select Input
$\overline{OE}$	TTL Output Enable
FST	TTL ÷2, ÷4, ÷8 Output
FSE, $\overline{FSE}$	Diff ECL ÷2, ÷4, ÷8 Outputs
FOE, $\overline{FOE}$	Diff ECL ÷1 Outputs
$\overline{EBE}$	VCO Disable, ECL Level Input
$\overline{EBT}$	VCO Disable, TTL Level Input

6



FREQUENCY SELECT FUNCTION TABLE

FS Level	Divide Ratio
H	1/2
OPEN	1/4
L	1/8

VCO DISABLE FUNCTION TABLE

$\overline{EBE}$	$\overline{EBT}$	FOE, FSE, FST	$\overline{FOE}$, $\overline{FSE}$
H	H or OPEN	L	H
L or OPEN	H	OSCILLATION	
H	L	OSCILLATION	

Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC1} V_{CC2} V_{CC3}	Power Supply Voltage	–0.5 to +8.0	V
V_{IN} (TTL)	Input Voltage	–0.5 to V_{CC}	V
V_{IN} (ECL)	Input Voltage	–0.5 to V_{CC}	V
I_{OUT} (ECL)	Output Source Current – Surge	100	mA
	Output Source Current – Continuous	50	mA
T_J	Junction Operating Temperature	+140	°C
T_{STG}	Storage Temperature	–55 to +150	°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
T_A	Ambient Temperature	0 to +75	°C
V_{CC}	Supply Voltage	+4.75 to +5.25	V
I_{OH} (TTL)	TTL High Output Current	–1.0	mA
I_{OL} (TTL)	TTL Low Output Current	20	mA

DC CHARACTERISTICS (V_{CC} = 5.0V ±5%; R_X = 2.4kΩ; R_Y = 1.5kΩ; C_B = 0.001μF)

		0°C		25°C			75°C			
Symbol	Characteristic	Min	Max	Min	Typ	Max	Min	Max	Unit	Condition
I_{CC}	Supply Current	75	120	65	90	110	80	135	mA	$\overline{EBT}$ = $\overline{EBE}$ = V_{CC} (ECL, TTL)
V_{OLT}	Output Low Voltage, TTL					0.5			V	F_S = GND
V_{OHT}	Output High Voltage, TTL			2.4					V	F_S = GND
V_{OLE}	Output Low Voltage, ECL			3.0		3.4			V	V_{CC} = 5.0V, R_L = 50Ω, V_T = 3.0V
V_{OHE}	Output High Voltage, ECL			3.9		4.19			V	V_{CC} = 5.0V, R_L = 50Ω, V_T = 3.0V
I_{ILT}	$\overline{EBT}$ Input Low Current					400			μA	V_{IN} = 0.4V
I_{IHT}	$\overline{EBT}$ Input High Current					20			μA	V_{IN} = 2.7V
						100			μA	V_{IN} = 7.0V
I_{INHE}	$\overline{EBE}$ Input High Current					250			μA	V_{IN} = 4.19V
I_{INLE}	$\overline{EBE}$ Input Low Current			1.0					μA	V_{IN} = 3.05V
V_{ILS}	FS Input, Max "L" Level					1.2			V	V_{CC} = 5.0V
V_{IMS}	FS Input, "Medium" Level			2.0		3.0			V	V_{CC} = 5.0V
V_{IHS}	FS Input, Min "H" Level			3.8					V	V_{CC} = 5.0V
V_{ILT}	$\overline{EBT}$ Input Low Voltage		0.8			0.8		0.8	V	
V_{IHT}	$\overline{EBT}$ Input High Voltage	2.0		2.0			2.0		V	
V_{IHE}	$\overline{EBE}$ Input High Voltage			3.87		4.19			V	V_{CC} = 5.0V
V_{ILE}	$\overline{EBE}$ Input Low Voltage			3.05		3.52			V	V_{CC} = 5.0V
V_{LM}	V_C Input Voltage, V_C = V_{CC} ÷ 2			±1.1	±1.3	±1.5			V	V_{CC} = 5.0V
V_{CB}	C_B Output Voltage			2.35	2.50	2.65			V	V_{CC} = 5.0V

AC CHARACTERISTICS (V_{CC} = 5.0V; R_X = 2.4kΩ; R_Y = 1.5kΩ; C_B = 0.001μF; V_T = 3.0V)

		0°C		25°C			75°C			
Symbol	Characteristic	Min	Max	Min	Typ	Max	Min	Max	Unit	Condition
FO	Center Frequency (V_{VC} – V_{CB} = 0V)			180	200	220			MHz	V_{CC} = +2.0V V_{EE} = –3.0V
F_{MAX} – F_{MIN}	Frequency Range (V_C = 1/2 V_{CC} ±1.5V, V_{CC} = 5.0V)			85	100	115			MHz	
t_{rE}	FOE/$\overline{FOE}$/FSE/$\overline{FSE}$ Rise Time			0.5		2.4			ns	
t_{fE}	FOE/$\overline{FOE}$/FSE/$\overline{FSE}$ Fall Time			0.5		2.4			ns	
TTT	Reset Time					35			ns	$\overline{EBT}$ ~ FST
TTO	Reset Time					25			ns	$\overline{EBT}$ ~ FOE/$\overline{FOE}$
TTS	Reset Time					30			ns	$\overline{EBT}$ ~ FSE/$\overline{FSE}$
TET	Reset Time					37			ns	$\overline{EBE}$ ~ FST
TEO	Reset Time					12			ns	$\overline{EBE}$ ~ FOE/$\overline{FOE}$
TES	Reset Time					25			ns	$\overline{EBE}$ ~ FSE/$\overline{FSE}$

Loading: ECL = 50Ω to V_T; TTL = 500Ω, 50pF

6

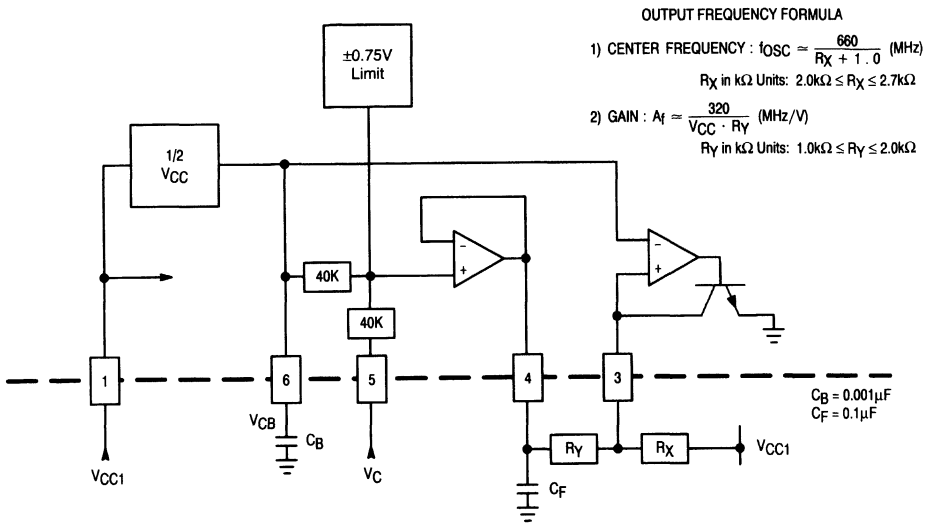


Figure 2. VCO Detail

Notes:

- For optimum VCO linearity (MHz/V), the following resistor ranges are recommended:
  2.0kΩ ≤ R_X ≤ 2.7kΩ (R_Y = 1.5kΩ)
  1.0kΩ ≤ R_Y ≤ 2.0kΩ (R_X = 2.4kΩ)
- TTL output maximum frequency = 50MHz
- Simultaneous use of both ECL and TTL outputs are not recommended due to excessive power consumption for the EIAJ Type II SO package

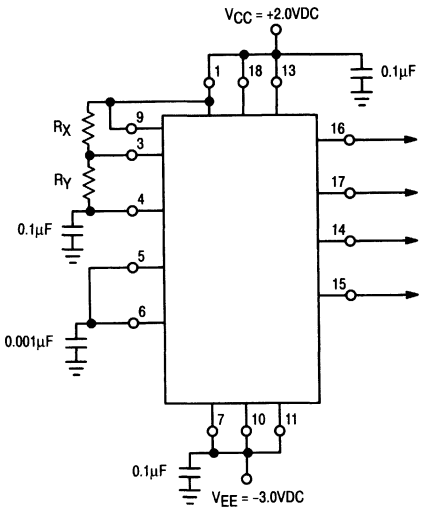


Figure 3. AC Test Circuit (FO/t_{rE}/t_{fE} Measurement)

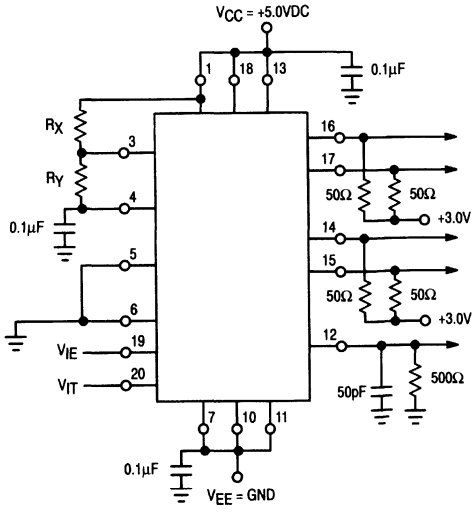


Figure 4. AC Test Circuit (Other Measurements)

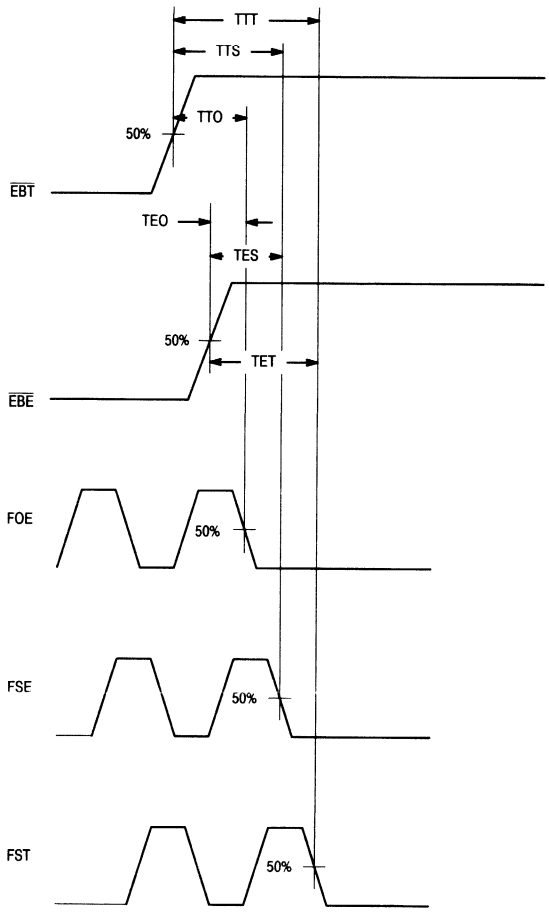


Figure 5. Switching Waveforms

VCO DISABLE FUNCTION TABLE

$\overline{EBE}$	$\overline{EBT}$	FOE, FSE, FST	$\overline{FOE}$, $\overline{FSE}$
H	H or OPEN	L	H
L or OPEN	H	OSCILLATION	
H	L	OSCILLATION	

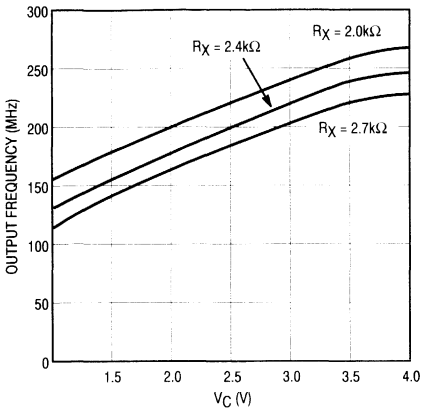


Figure 6. V_C versus Output Frequency
Varying R_X @ V_{CC} = 5.0V; T_A = 25°C; R_Y = 1.5kΩ

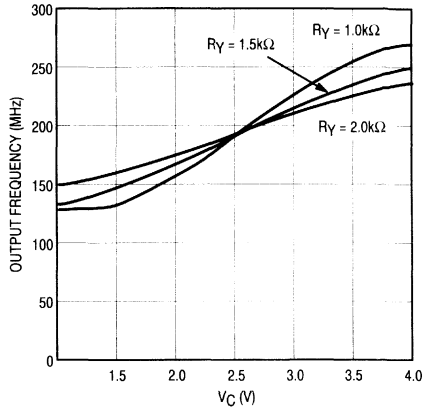


Figure 7. V_C versus Output Frequency
Varying R_Y @ V_{CC} = 5.0V; T_A = 25°C; R_X = 2.4kΩ

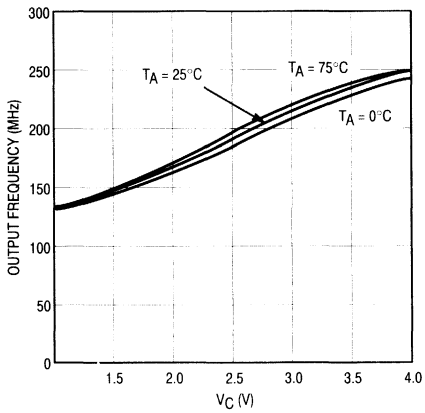


Figure 8. V_C versus Output Frequency
Varying T_A @ V_{CC} = 5.0V; R_X = 2.4kΩ; R_Y = 1.5kΩ

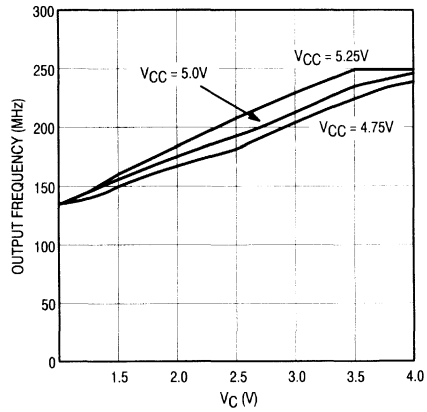


Figure 9. V_C versus Output Frequency
Varying V_{CC} @ R_X = 2.4kΩ; R_Y = 1.5kΩ; T_A = 25°C

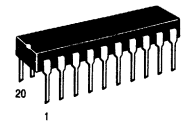
MOTOROLA

MC12101

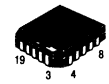
130MHz Voltage Controlled Multivibrator

130MHz VOLTAGE CONTROLLED MULTIVIBRATOR

- High Frequency VCM Ideal for PLL Applications
- Single External Resistor Determines Center Frequency; Additional Resistor Determines f/V Sensitivity
- Internal Ripple Counter (1/2, 1/4, 1/8) For Low Frequency Applications – TTL/ECL Outputs
- VCO Output Enable Pins (TTL/ECL Level)
- +5.0V Single Supply Voltage
- Packages: DIP, PLCC

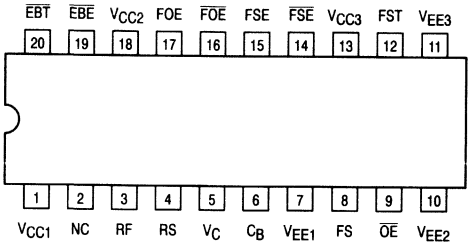


P SUFFIX
PLASTIC DIP PACKAGE
CASE 738-03

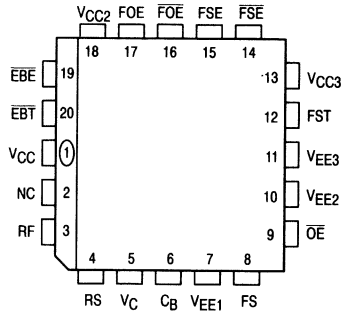


FN SUFFIX
PLCC PACKAGE
CASE 775-02

Pinout: 20-Lead Plastic Package (Top View)



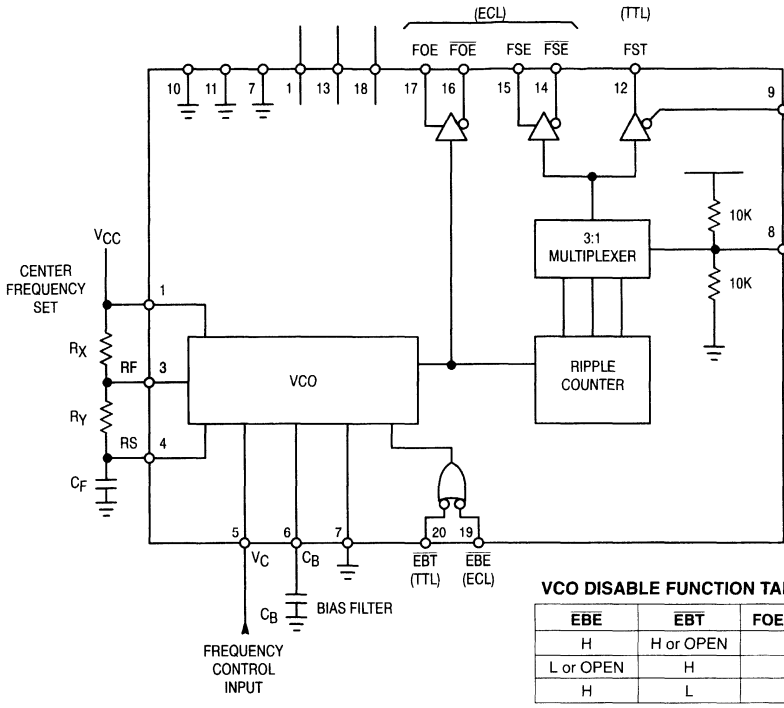
Pinout: 20-Lead PLCC Package (Top View)



PIN NAMES

Pin	Function
RF, RS	Center Frequency Inputs
V_C	Frequency Control Input
C_B	Bias Filter Input
FS	Frequency Select Input
$\overline{OE}$	TTL Output Enable
FST	TTL ÷2, ÷4, ÷8 Output
FSE, $\overline{FSE}$	Diff ECL ÷2, ÷4, ÷8 Outputs
FOE, $\overline{FOE}$	Diff ECL ÷1 Outputs
$\overline{EBE}$	VCO Disable, ECL Level Input
$\overline{EBT}$	VCO Disable, TTL Level Input

6



FREQUENCY SELECT FUNCTION TABLE

FS Level	Divide Ratio
H	1/2
OPEN	1/4
L	1/8

VCO DISABLE FUNCTION TABLE

$\overline{EBE}$	$\overline{EBT}$	FOE, FSE, FST	$\overline{FOE}$, $\overline{FSE}$
H	H or OPEN	L	H
L or OPEN	H	OSCILLATION	
H	L	OSCILLATION	

Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC1} V_{CC2} V_{CC3}	Power Supply Voltage	−0.5 to +8.0	V
V_{IN} (TTL)	Input Voltage	−0.5 to V_{CC}	V
V_{IN} (ECL)	Input Voltage	−0.5 to V_{CC}	V
I_{OUT} (ECL)	Output Source Current – Surge	100	mA
	Output Source Current – Continuous	50	mA
T_J	Junction Operating Temperature	+140	°C
T_{STG}	Storage Temperature	−55 to +150	°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
T_A	Ambient Temperature	0 to +75	°C
V_{CC}	Supply Voltage	+4.75 to +5.25	V
I_{OH} (TTL)	TTL High Output Current	−1.0	mA
I_{OL} (TTL)	TTL Low Output Current	20	mA

DC CHARACTERISTICS (V_{CC} = 5.0V ±5%; R_X = 2.4kΩ; R_Y = 1.5kΩ; C_B = 0.001μF)

Symbol	Characteristic	0°C		25°C			75°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
I_{CC}	Supply Current	80	135	70	100	120	85	150	mA	$\overline{EBT}$ = $\overline{EBE}$ = V_{CC} (ECL, TTL)
V_{OLT}	Output Low Voltage, TTL					0.5			V	F_S = GND
V_{OHT}	Output High Voltage, TTL			2.4					V	F_S = GND
V_{OLE}	Output Low Voltage, ECL			3.0		3.4			V	V_{CC} = 5.0V, R_L = 50Ω, V_T = 3.0V
V_{OHE}	Output High Voltage, ECL			3.9		4.19			V	V_{CC} = 5.0V, R_L = 50Ω, V_T = 3.0V
I_{ILT}	$\overline{EBT}$ Input Low Current					400			μA	V_{IN} = 0.4V
I_{IHT}	$\overline{EBT}$ Input High Current					20			μA	V_{IN} = 2.7V
						100			μA	V_{IN} = 7.0V
I_{INHE}	$\overline{EBE}$ Input High Current					250			μA	V_{IN} = 4.19V
I_{INLE}	$\overline{EBE}$ Input Low Current			1.0					μA	V_{IN} = 3.05V
V_{ILS}	FS Input, Max "L" Level					1.2			V	V_{CC} = 5.0V
V_{IMS}	FS Input, "Medium" Level			2.0		3.0			V	V_{CC} = 5.0V
V_{IHS}	FS Input, Min "H" Level			3.8					V	V_{CC} = 5.0V
V_{ILT}	$\overline{EBT}$ Input Low Voltage		0.8			0.8		0.8	V	
V_{IHT}	$\overline{EBT}$ Input High Voltage	2.0		2.0			2.0		V	
V_{IHE}	$\overline{EBE}$ Input High Voltage			3.87		4.19			V	V_{CC} = 5.0V
V_{ILE}	$\overline{EBE}$ Input Low Voltage			3.05		3.52			V	V_{CC} = 5.0V
V_{LM}	V_C Input Voltage, V_C = V_{CC} + 2			±1.1	±1.3	±1.5			V	V_{CC} = 5.0V
V_{CB}	C_B Output Voltage			2.35	2.50	2.65			V	V_{CC} = 5.0V

AC CHARACTERISTICS (V_{CC} = 5.0V; R_X = 2.4kΩ; R_Y = 1.5kΩ; C_B = 0.001μF; V_T = 3.0V)

Symbol	Characteristic	0°C		25°C			75°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
FO	Center Frequency (V_{VC} – V_{CB} = 0V)			117	130	143			MHz	V_{CC} = +2.0V V_{EE} = –3.0V
F_{MAX} – F_{MIN}	Frequency Range (V_C = 1/2 V_{CC} ±1.5V, V_{CC} = 5.0V)			68	80	92			MHz	
t_{rE}	FOE/$\overline{FOE}$/FSE/$\overline{FSE}$ Rise Time			0.5		2.4			ns	
t_{fE}	FOE/$\overline{FOE}$/FSE/$\overline{FSE}$ Fall Time			0.5		2.4			ns	
TTT	Reset Time					40			ns	$\overline{EBT}$ ~ FST
TTO	Reset Time					25			ns	$\overline{EBT}$ ~ FOE/$\overline{FOE}$
TTS	Reset Time					35			ns	$\overline{EBT}$ ~ FSE/$\overline{FSE}$
TET	Reset Time					32			ns	$\overline{EBE}$ ~ FST
TEO	Reset Time					12			ns	$\overline{EBE}$ ~ FOE/$\overline{FOE}$
TES	Reset Time					30			ns	$\overline{EBE}$ ~ FSE/$\overline{FSE}$

Loading: ECL = 50Ω to V_T; TTL = 500Ω, 50pF

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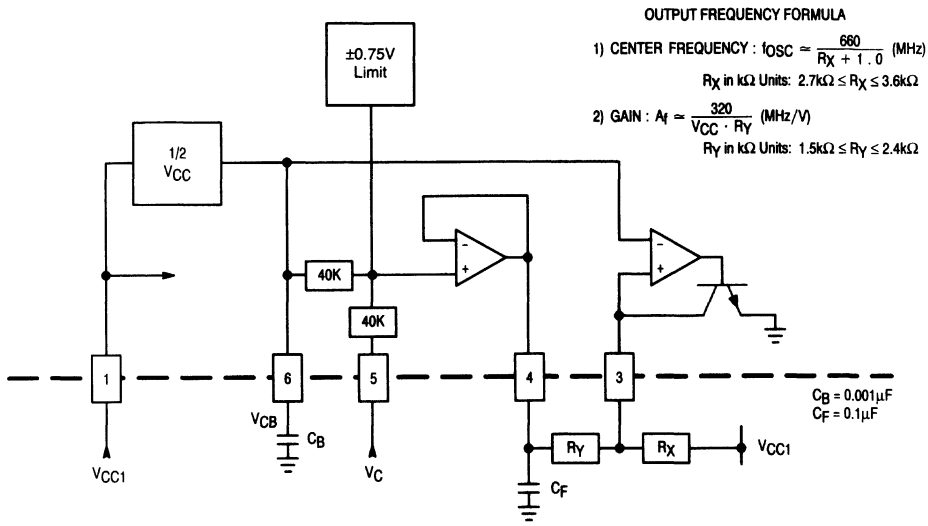


Figure 2. VCO Detail

Notes:

- For optimum VCO linearity (MHz/V), the following resistor ranges are recommended:
  2.7kΩ ≤ R_X ≤ 3.6kΩ (R_Y = 2.0kΩ)
  1.5kΩ ≤ R_Y ≤ 2.4kΩ (R_X = 3.3kΩ)
- TTL output maximum frequency = 50MHz
- Simultaneous use of both ECL and TTL outputs are not recommended due to excessive power consumption for the EIAJ Type II SO package

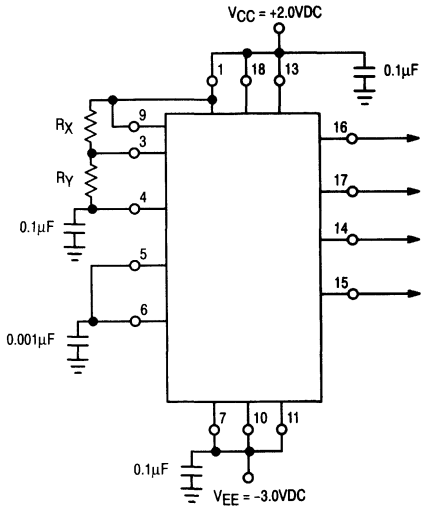


Figure 3. AC Test Circuit (FO/t_{rE}/t_{fE} Measurement)

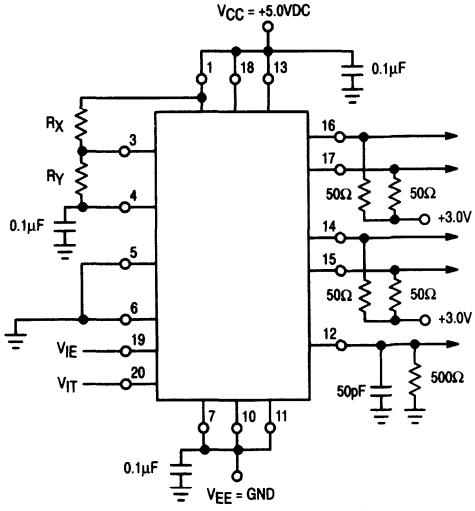


Figure 4. AC Test Circuit (Other Measurements)

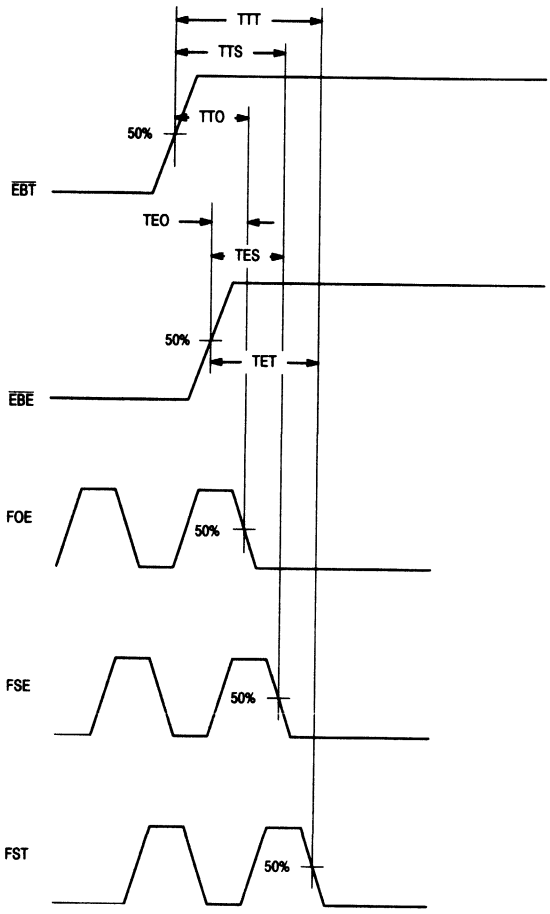


Figure 5. Switching Waveforms

VCO DISABLE FUNCTION TABLE

$\overline{EBE}$	$\overline{EBT}$	FOE, FSE, FST	$\overline{FOE}$, $\overline{FSE}$
H	H or OPEN	L	H
L or OPEN	H	OSCILLATION	
H	L	OSCILLATION	

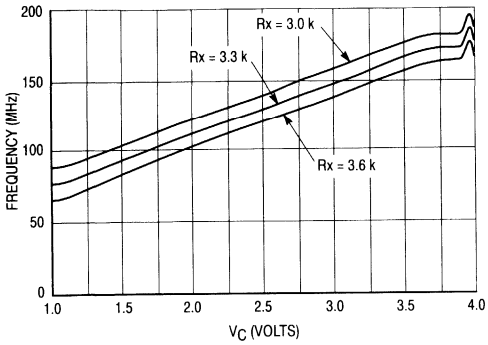


Figure 6. V_C versus Output Frequency
Varying Rx @ V_{CC} = 5.0 V; T_A = 25°C; Ry = 2.0 kΩ

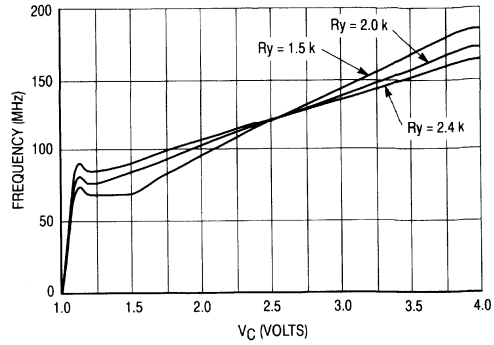


Figure 7. V_C versus Output Frequency
Varying Ry @ V_{CC} = 5.0 V; T_A = 25°C; Ry = 3.3 kΩ

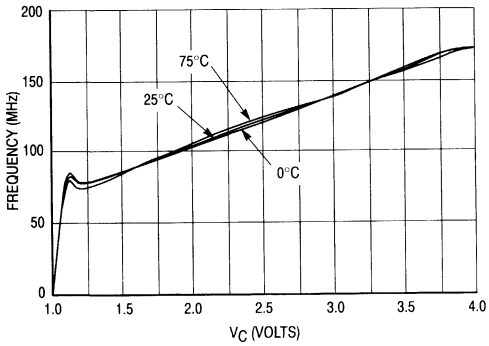


Figure 8. V_C versus Output Frequency
Varying T_A @ V_{CC} = 5.0 V; Rx = 3.3 kΩ; Ry = 2.0 kΩ

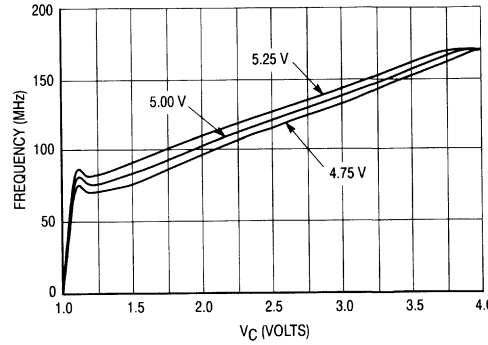


Figure 9. V_C versus Output Frequency
Varying V_{CC} @ Rx = 3.3 kΩ; Ry = 2.0 kΩ; T_A = 25°C

6

MOTOROLA

MC12148

LOW-POWER VOLTAGE CONTROLLED OSCILLATOR

Advance Information

Low-Power Voltage Controlled Oscillator

The MC12148 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C). A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). This device may also be used in many other applications requiring a fixed frequency clock.

The MC12148 is ideal in applications requiring a local oscillator. Systems include electronic test equipment and digital high-speed telecommunications.

- 700MHz Center Frequency Tunable From 200 to 1100MHz
- Low-Power 20mA at 5.0Vdc Power Supply
- 8-Pin SOIC Package
- Phase Noise –90dBc/Hz at 25KHz Typical

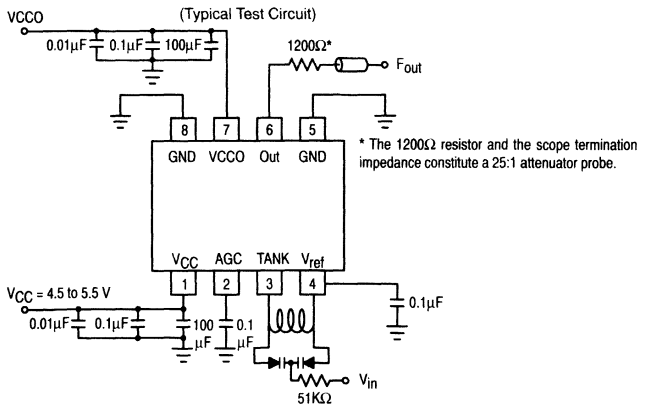
D SUFFIX
SOIC PACKAGE
CASE 751

SD SUFFIX
SSOP PACKAGE
CASE 940

MAXIMUM RATINGS

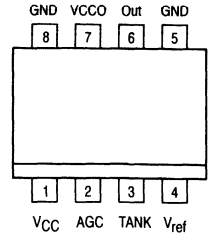
Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage, Pin 8	–0.5 to +7.0	Vdc
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C

BLOCK DIAGRAM
(Typical Test Circuit)



* The 1200Ω resistor and the scope termination impedance constitute a 25:1 attenuator probe.

Pinout: 8-Lead SOIC (Top View)



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This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V; T_A = –40°C to +85°C)

Symbol	Characteristic		Min	Typ	Max	Unit
I_{CC}	Supply Current			19	25	mA
V_{OH}	Output Level HIGH (1MΩ Impedance)			4.17		V
V_{OL}	Output Level LOW (1MΩ Impedance)			3.41		V
$\mathcal{L}(f)$	CSR @ 25KHz Offset, 1Hz BW			–90		dBc/Hz
$\mathcal{L}(f)$	CSR @ 1MHz Offset, 1Hz BW			–120		dBc/Hz
SNR	SNR (Signal to Noise Ratio from Carrier)			40		dB
Fsts	Frequency Stability	Supply Drift		3.6		KHz/mV
Fstt		Thermal Drift		0.1		KHz/°C
H2	Second Harmonic (from Carrier)			–25		dBc

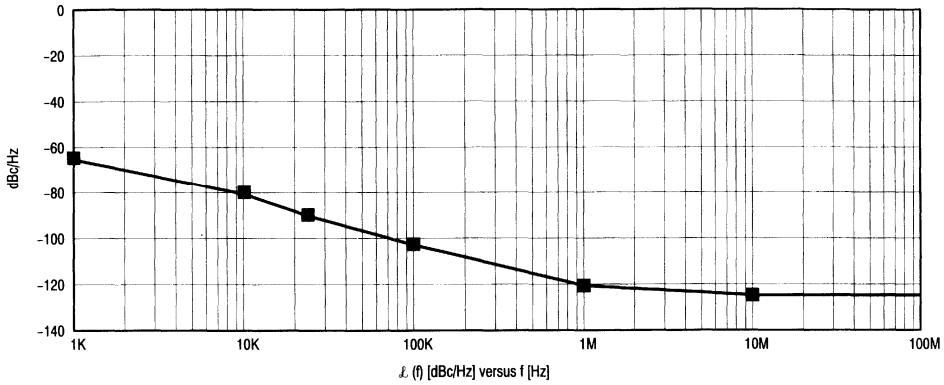


Figure 1. Typical Evaluation Results
(CSR MC12148 5.0Vdc; V_{CC} @ 25°C; 930MHz CW)

Tank Component Suppliers

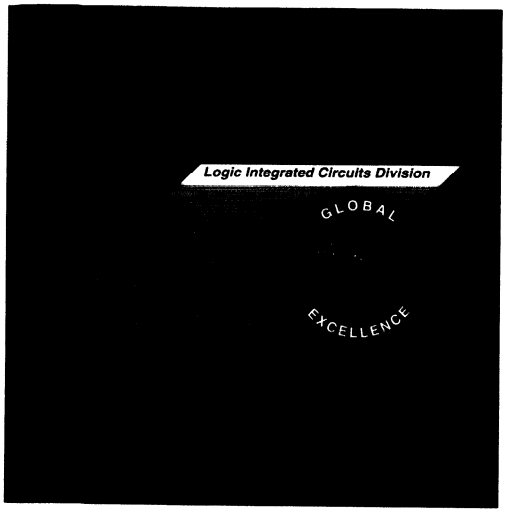
Below are suppliers who manufacture tuning varactors and inductors which can be used to build an external tank circuit. Motorola has used these varactors and inductors for evaluation purposes, however, there are other vendors who manufacture similar products.

Coilcraft Inductors A01T thru A05T
Coilcraft-Coilcraft, Inc.
1102 Silver Lake Rd.
Gary, Illinois 60013
708-639-6400

Loral Tuning Varactors GC1500 Series
Loral
16 Maple Road
Chelmsford, Massachusetts 01824
508-256-8101 or 508-256-4113

Motorola Varactor MMBV809L
Contact your local Motorola Semiconductor Sales Office.

Alpha Tuning Diodes DVH6730 Series
Alpha
Semiconductor Devices Division
20 Sylvan Road
Woburn, MA 01801
617-935-5150



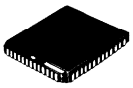
Carrier Band Modem

Data Sheet 7

MOTOROLA

MC68194

Carrier Band Modem (CBM)

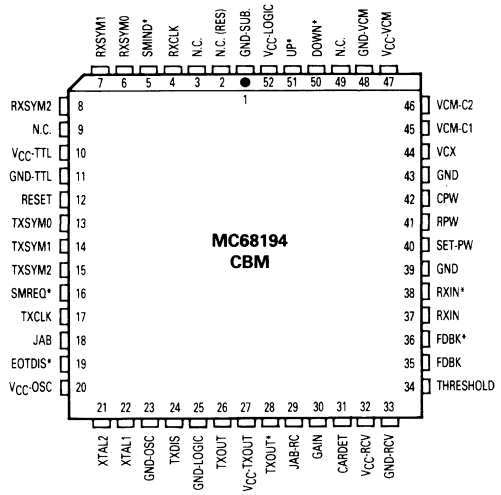


FJ SUFFIX
J-LEAD CERQUAD
CASE 778B-01

The bipolar LSI MC68194 Carrier Band Modem (CBM) when combined with the MC68824 Token Bus Controller provides an IEEE 802.4 single channel, phase-coherent carrier band Local Area Network (LAN) connection. The CBM performs the Physical Layer function including symbol encoding/decoding, signal transmission and reception, and physical management. Features include:

- Implements IEEE 802.4 single channel, phase-coherent Frequency Shift Keying (FSK) physical layer including receiver blanking.
- Provides physical layer management including local loopback mode, transmitter enable, and reset.
- Supports data rates from 1 to 10 Mbps. IEEE 802.4 standard uses 5 or 10 Mbps.
- Interfaces via standard serial interface to MC68824 Token Bus Controller.
- Crystal controlled transmit clock.
- Recovery of clocked data through phase-locked loop.
- RC controlled Jabber Inhibit Timer.
- Single +5.0 volt power supply.
- Available in 52-lead Cerquad package.

PIN ASSIGNMENTS



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SECTION 1
GENERAL DESCRIPTION

1.1 TOKEN BUS LAN CARRIER BAND NODE OVERVIEW

The MC68194 Carrier Band Modem (CBM) is part of Motorola's solution for an IEEE 802.4 token bus carrier band Local Area Network (LAN) node. The CBM integrates the function of the single-channel, phase-coherent Frequency Shift Keying (FSK) physical layer. Figure 1-1 illustrates the architecture of a token bus LAN node as commonly used in Manufacturing Automation Protocol (MAP) industrial communications. Based on the ISO-OSI model, the LLC Sublayer and additional upper layers are typically supported by a local MPU subsystem, while the IEEE 802.4 token bus MAC Sublayer and Physical Layer are implemented by the MC68824 Token Bus Controller (TBC) and MC68194 CBM respectively.

The MC68194 provides the three basic functions of the physical layer including data transmission to the coax cable, data reception from the cable, and management of the physical layer. For standard data mode (also called MAC mode), the carrier band modem receives a serial transmit data stream from the MC68824 TBC (called symbols or atomic symbols), encodes, modulates the carrier, and transmits the signal to the coaxial cable. Also in the data mode, the CBM receives a signal from the cable, demodulates the signal, recovers the data, and sends the received data symbols to the TBC. Communication between the TBC and CBM is through a standardized serial interface consistent with the IEEE 802.4 DTE-DCE serial interface.

The physical layer management provides the ability to reset the CBM, control the transmitter, and do loopback testing. Also, an onboard RC timer provides a "jabber" inhibit function to turn off the transmitter and report an error condition if the transmitter has been continuously on for too long. Similar to the data mode, the CBM management mode makes use of the TBC serial interface.

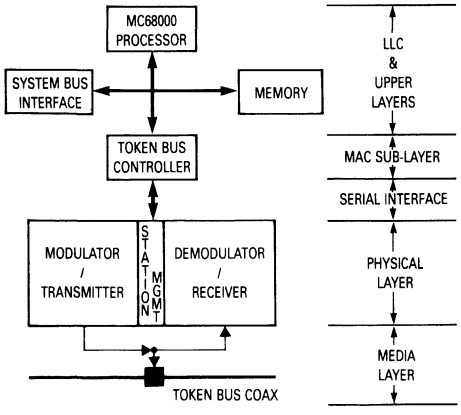

Figure 1-1. IEEE 802.4 Token Bus Carrier Band Node

1.2 CARRIER BAND MODULATION TECHNIQUE

The CBM uses phase-coherent frequency shift keying (FSK) modulation on a single channel system. In this modulation technique, the two signaling frequencies are integrally related to the data rate, and transitions between the two signaling frequencies are made at zero crossings of the carrier waveform. Figure 1-2 shows the data rate and signaling frequencies. An {L} is represented as one half cycle of a signal, starting and ending with a nominal zero amplitude, whose period is equal to the period of the data rate, with the phase of one half cycle changing at each successive {L}. An {H} is represented as one full cycle of a signal, starting and ending with a nominal zero amplitude whose period is equal to half the period of the data rate. In a 5 Mbps implementation, the frequency of {L} is 5.0 MHz and for {H} is 10 MHz. For a 10 Mbps implementation, the frequency of {L} is 10 MHz and for {H} is 20 MHz. The other possible physical symbol is when no signal occurs for a period equal to one half of the period of the data rate. This condition is represented by {off}.

Data Rate MBPS	Frequency of Lower Tone MHz {L}	Frequency of Higher Tone MHz {H}
5	5.0	10
10	10	20

Figure 1-2. Data Rate versus Signaling Frequencies

The specified physical symbols ({L}, {H} and {off}) are combined into pairs which are called MAC-symbols. The MAC-symbols are transferred across the serial link. The encodings for the five MAC-symbols are shown in Figure 1-3. Figure 1-4 shows the phase coherent FSK modulation scheme for ONE, ZERO, and NON-DATA. The IEEE 802.4 document does not specify the polarity used to transmit data on the physical cable. The receiver must operate without respect to polarity.

Mac-Symbol	Encoding
Silence	{off off}
Pad-Idle Pairs	{L L} {H H}
Zero	{H H}
One	{L L}
Non-Data	
ND1	{H L}
ND2	{L H}

Figure 1-3. MAC Symbol Encodings

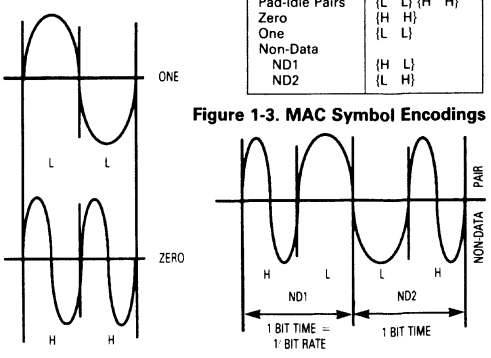

Figure 1-4. Phase-Coherent Modulation Scheme

1.3 MESSAGE (FRAME) FORMAT

Although the CBM only uses MAC symbols one-at-a-time, the MAC or TBC is responsible for combining the above defined MAC symbols into messages (more correctly called frames). For the purposes of the CBM, a simplified frame format can be used consisting of:

SILENCE || PAD-IDLE | START DELIMITER | DATA | END DELIMITER || SILENCE

where:

PAD-IDLE = alternating {LL} {HH} pairs which must occur in octets or groups of eight symbols. Pad-idle provides a training signal for the receiver and occurs at the beginning of every transmission (and between frames in a multiple frame transmission).

START DELIMITER = a unique pattern of eight symbols (one octet) that marks the beginning of a frame. The pattern is:

ND1 ND2 0 ND1 ND2 0 0 0

where ND1 is the first symbol transmitted.

DATA = octets of ZERO/ONE patterns that are the actual data or "information" contained within the frame.

END DELIMITER = a unique pattern of symbols that marks the end of a frame. The pattern is:

ND1 ND2 1 ND1 ND2 1 {I=0/1} {0/1}

where ND1 is the first symbol transmitted. Note that unlike the Start Delimiter, the last two bits of the End Delimiter octet are not always the same. The seventh bit of the octet is called the I Bit or Intermediate bit which = 1 when there is more to transmit and = 0 at the end of a transmission.

A single transmission can consist of one or more frames. In a multi-frame transmission, Pad-Idle is sent between consecutive frames to separate them. If an End Delimiter occurs **within** a multi-frame transmission its I Bit will = 1, and the **last** end delimiter will have its I Bit = 0.

The CBM accepts a stream of MAC symbols from the TBC and modulates the phase-coherent transmit signal accordingly. Conversely, the CBM receives a phase-coherent signal stream from the cable, decodes the MAC symbols, and reports them. On transmission there is a direct one-to-one correlation between MAC symbols requested and the modulated signal; however, during reception exceptions can occur. The CBM is allowed to report Silence or the actual Zero/One pattern during preamble which is done to allow the receiver to "train" to the incoming signal. Also, if noise in the system has corrupted the data, it may show up as an incorrect MAC symbol or the CBM can report a BAD SIGNAL symbol if an incorrect combination of ND symbols is detected (ND2 without an ND1, ND2 followed by ND2, etc.)

1.4 SYSTEM CONFIGURATION

Figure 1-5 illustrates the CBM and peripheral circuitry required for an IEEE 802.4 carrierband 5 Mbps or 10 Mbps data rate phase-coherent FSK physical layer. The CBM communicates with the MAC or TBC through a TTL compatible serial interface that is consistent with the IEEE 802.4 exposed DTE-DCE interface. Management and transmission symbol requests are accepted via the CBM physical data request channel (TXSYM0-TXSYM2, SMREQ*, and TXCLK). The physical data indication channel (RXSYM0-RXSYM2, SMIND*, and RXCLK) is used to send received symbols and management responses to the MAC.

The periphery circuitry is primarily associated with interface to the LAN coaxial cable and data recovery. An external crystal or clock source is required (20 MHz for 5 Mbps data rate or 40 MHz for 10 Mbps data rate) for onboard timing and transmit clock. Also, an RC timing network sets the jabber timeout period.

The coaxial cable interface combines the transmit and receive signal functions. For transmission, the CBM provides differential drive signals (TXOUT and TXOUT*) whose signaling is ECL levels referenced to V_{CC} (logic high $\approx +4.1$ V, logic low $\approx +3.3$ V) and a gate signal called TXDIS. The IEEE 802.4 standard puts specific requirements on the signal transmitted to the cable:

Between +63 dB and +66 dB (1.0 mV, 75 Ω) [dBmV] output voltage level.

Transmitter-off leakage not to exceed −20 dB (1.0 mV, 75 Ω) [dBmV].

Signal transition time window (eye pattern) dependent on data rate.

Because of this, an external amplifier with waveshaping is required. The CBM TXOUT/TXOUT* outputs provide complementary signals with virtually no slew, and the TXDIS is an enable signal helpful for turning the external amp off "hard" to meet the low level leakage.

On the reception side, the CBM requires a pre-amplifier to receive the low level signal from the cable. The signal available at the "F"-connector can range from +10 dB to +66 dB (1.0 mV, 75 Ω) [dBmV]. The signal required at the CBM is about 12 dB above this (net gain through the transformer, pre-amp, and any filtering). The receiver can be used in full differential or single-ended mode.

A second part of the receiver function is the signal detect or carrier detect function. The IEEE 802.4 requires that the receiver detect a signal of +10 dBmV or above (i.e., be turned "on") and report Silence for a signal of +4.0 dBmV or below (i.e., be turned "off"). Therefore, a 6.0 dB (2:1 voltage ratio) range or window is defined in which the signal detect must switch. The CBM is optimized for this range (including the pre-amp gain), although it is trimmed via an external THRESHOLD.

The remaining external components are associated with clock recovery. A capacitor and resistor (internal R also provided) set one-shot timing, and an active filter for a PLL used in clock and data recovery is required. The active filter can be implemented via an op amp, or if 5.0 volt operation is required, an alternate charge pump design can be used. The clock recovery and data decoder

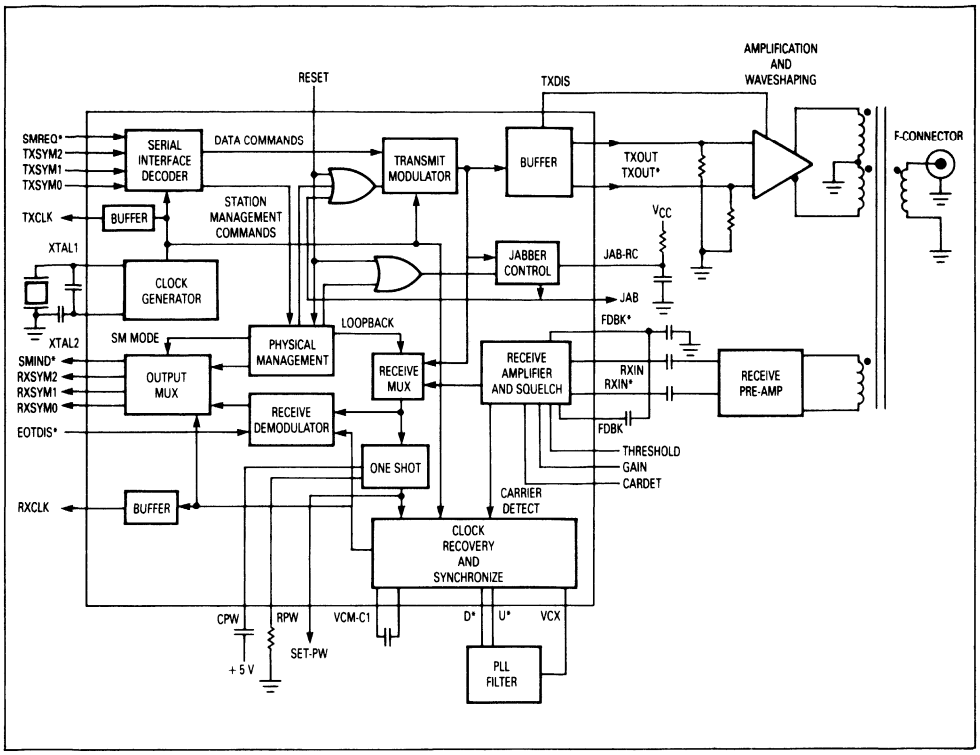

Figure 1-5. Functional Block Diagram

is a synchronous design which provides superior performance minimizing clock jitter.

Although primarily intended for the IEEE 802.4 carrier band, the CBM is also an excellent device for point-to-point data links, fiberoptic modems, and proprietary LANs. The MC68194 can be used over a wide range of frequencies and interfaces easily into different kinds of media.

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SECTION 2
SIGNAL DESCRIPTION

Symbol	Type	Name/Description
TXSYM0-TXSYM2	TTL/I*	**TRANSMIT SYMBOLS** — These TTL inputs are request channel signals used to send either serial transmission symbols in the MAC mode or commands in station management mode. They are synchronized to TXCLK and are normally connected to the TXSYMX outputs of the MC68824. SMREQ* selects the meaning of these signals as either MAC mode or management mode.
SMREQ*	TTL/I*	**STATION MANAGEMENT REQUEST** — A TTL input that selects the mode of the request channel signals TXSYMX. Synchronized to TXCLK, SMREQ* is equal to one for MAC mode and equal to zero for management mode. It is normally driven by the SMREQ* output of the MC68824.
TXCLK	TTL/O	**TRANSMIT CLOCK** — A TTL clock output generated from the crystal oscillator (it is 1/4 of the oscillator frequency) used to receive request channel symbols from the MC68824. TXCLK is equal to the data rate of the application (5.0 MHz or 10 MHz for IEEE 802.4). TXSYMX and SMREQ* are synchronized to the **positive** edge of TXCLK which is supplied to the MC68824.
RXSYM0-RXSYM2	TTL/O	**RECEIVE SYMBOLS** — These TTL outputs are indication channel signals used to provide either serial receive symbols in MAC mode or command confirmation/indication in station management mode. They are synchronized to RXCLK and are normally connected to the RXSYMX inputs of the MC68824. SMIND* selects the meaning of these signals as either MAC mode or management mode.
SMIND*	TTL/O	**STATION MANAGEMENT INDICATION** — A TTL output that indicates the mode of the CBM and RXSYMX lines. Synchronized to RXCLK, SMIND* is equal to one for MAC mode and equal to zero for management mode. It is normally connected to the SMIND* input of the MC68824.
RXCLK	TTL/O	**RECEIVE CLOCK** — A TTL clock output used to send indication channel symbols to the MC68824. Its frequency is nominally equal to the data rate (5.0 MHz or 10 MHz for IEEE 802.4). RXCLK is generated from a PLL that is locked to the local oscillator during loopback, station management, or the absence of received data. During frame reception the PLL is locked to the incoming received data. RXSYMX and SMIND* are synchronized to **negative** edge of RXCLK.
EOTDIS*	TTL/I*	**END-OF-TRANSMISSION DISABLE** — When low, this TTL input disables the end-of-transmission receiver blanking required by the IEEE 802.4 Spec, Section 12.7.6.3. When high the blanking works in accordance with the spec requirements.
TXOUT,TXOUT*	ECL/O	**TRANSMIT OUTPUTS** — A differential output signal pair (MECL level referenced to V_{CC}) used to drive the transmitter circuitry. The silence or "off" state is both outputs one (high). The output data stream is phase-coherent FSK encoded.
TXDIS	OC	**TRANSMIT DISABLE** — An open collector output used to disable transmitter circuitry. This output is high when the transmitter is off (TXOUT and TXOUT* both high).
JAB	TTL/O	**JABBER** — A TTL output signal generated from the jabber-inhibit timer. When equal to one, JAB indicates the timer has timed-out and an error has occurred.
RESET	TTL/I*	**RESET** — A TTL input signal that when high asynchronously resets the CBM.
RXIN, RXIN*	I	**RECEIVER INPUTS** — A differential input signal pair for the receiver amplifier/limiter. These inputs may be used differentially or single ended.
FDBK, FDBK*		**DC FEEDBACK BYPASS** — These two points are provided to bypass dc feedback around the receiver amplifier.

*All TTL inputs include a 15 kΩ pullup resistor to V_{CC}.

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Signal Description (Cont.)

Symbol	Type	Name/Description
THRESHOLD	I	**THRESHOLD ADJUST** — The receiver threshold detect is trimmed with this pin.
GAIN	O	**GAIN** — This output can be used to monitor the receiver amplifier output signal. Used only for test purposes.
CARDET	O	**CARRIER DETECT** — This output can be used to filter the internal signal that is sampled to sense carrier detect.
RPW, CPW	I	**PULSE-WIDTH RESISTOR/CAPACITOR** — A resistor and capacitor set a one-shot pulse width used in the clock recovery circuitry.
SET-PW	O	**PULSE WIDTH TEST POINT** — Output test point used for adjusting clock recovery one-shot pulse width.
UP*, DOWN*	ECL/O	**PLL PHASE DETECTOR OUTPUTS** — UP* and DOWN* are the pump-up and pump-down outputs, respectively, of the PLL digital phase detector. They are MECL levels referenced to +5.0 volts and are used to drive inputs to an active filter or charge pump for the PLL.
VCX	I	**VCM CONTROL** — The control voltage applied to the PLL voltage controlled multivibrator.
VCM-C1,VCM-C2	I	**VCM CAPACITOR** — VCM capacitor inputs. VCM frequency is 4X RXCLK.
JAB-RC	I	**JABBER-INHIBIT RC** — A resistor-capacitor network connected to this pin sets the jabber-inhibit time constant.
XTAL,1 XTAL2	I	**CLOCK CRYSTAL** — Oscillator circuit inputs may be used with a crystal or an external clock source. Oscillator frequency is 4X data rate.
V_{CC}-VCM		**VCM POWER** — 5.0 ± 5% volts for VCM.
V_{CC}-TXOUT		**TXOUT POWER** — 5.0 ± 5% volts for TXOUT/TXOUT*.
V_{CC}-OSC		**OSCILLATOR POWER** — 5.0 ± 5% volts for oscillator.
V_{CC}-RCV		**RECEIVER POWER** — 5.0 ± 5% volts for receiver amplifier/limiter.
V_{CC}		**LOGIC POWER** — 5.0 ± 5% volts for remaining logic.
V_{CC}-TTL		**TTL POWER** — 5.0 ± 5% volts for TTL output buffers.
GND-TTL, GND-VCM, GND-LOGIC, GND-OSC, GND-RCV, GND-SUBS, GND		**GROUND** — Reference voltage for TTL buffers, VCM, internal logic, oscillator, receiver/limiter, substrate respectively. Two additional grounds are used to isolate signals.

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SECTION 3
TRANSMITTER

3.1 OVERVIEW

The transmitter function includes the serial interface decoder, transmit modulator, transmit buffer, jabber inhibit, and clock generator. (Although the clock generator is not used exclusively by the transmit function, the generator will be discussed here.) The MC68194 receives request channel symbols on the TXSYMX pins which are synchronized to TXCLK. As is described in the Serial Interface discussion, MAC transmit symbols are input serially (CBM in MAC mode), decoded, and used to modulate an output signal. The Serial Interface Decoder is used both for MAC mode to decode data transmit commands (symbols) and management mode to decode management commands. The decoded transmit commands or symbols are used by the Transmit Modulator to generate phase-coherent signaling as discussed in the CBM General Description. The transmit buffer receives the modulated signal and drives differential output signals.

The clock generator provides TXCLK and internal clocks of 2 times (2X) and 4 times (4X) TXCLK. The 4X clock is actually the oscillator frequency. These clocks are used to receive the TX symbols and generate the modulated signal.

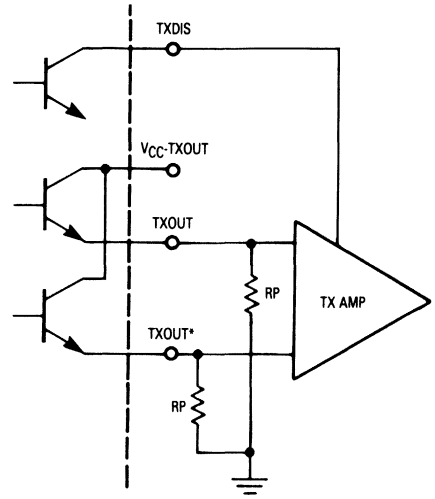


Figure 3-1. Transmitter Outputs

3.2 TRANSMIT BUFFER

The modulated transmit data stream drives the TXOUT and TXOUT* pins of the MC68194. These pins are complementary outputs with closely matched edge transitions. This is useful in helping meet the IEEE 802.4 carrierband requirement for a transmit jitter of less than ±1% of the data rate. TXOUT and TXOUT* are generally used to drive a differential amplifier which is used to achieve the necessary output level at the cable and meet the rise/fall time window (or "eye" pattern) of the IEEE 802.4. A third output called TXDIS is available to gate the amplifier circuitry on or off.

The TXOUT and TXOUT* have ECL levels referenced to V_{CC} (Figure 3-1). Levels are typically 4.11 V for a high and 3.25 for a low. Pulldown resistors are required with the outputs specified to drive a maximum load of 220 Ω to ground reference.

Operation of the transmit outputs is controlled in the following manner:

1. Management mode — The TX outputs are always disabled while the CBM is in management mode. When leaving management mode the TX outputs remain disabled if a RESET command has been issued and an ENABLE TRANSMITTER and DISABLE LOOPBACK commands have **not** been issued. Resetting the CBM enables internal loopback and disables the transmitter.
2. MAC (data) mode — After leaving management mode, the CBM can function in internal loopback (for test) with the transmitter disabled, out of loopback with transmitter disabled (receive only), or in standard data mode with the TX outputs controlled by the modulator.
3. Jabber inhibit activated — If the jabber inhibit fires, it forces the CBM into management mode and disables the TX outputs. This condition can only be cleared by a reset condition.

The TXDIS output is an open collector switched current source. TXDIS sinks a nominal 0.5 mA when the TXOUT/TXOUT* outputs are enabled. TXDIS is off or high impedance when the transmitter is disabled.

The signaling on the TX outputs and TXDIS is shown in Figure 3-2. The "off" or silence condition is both TXOUT outputs high and TXDIS also high. The figure shows an example of the signal pattern for both leaving and entering a silence condition.

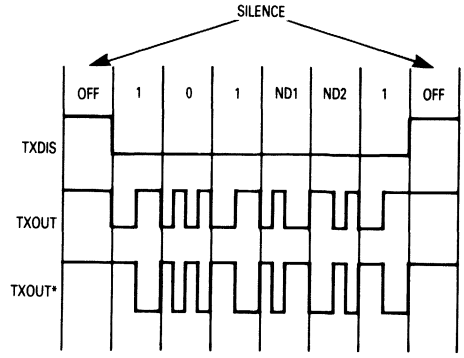


Figure 3-2. Transmit Output Signaling

3.3 JABBER INHIBIT

The jabber inhibit function prevents the transmitter from transmitting indefinitely. An external resistor and capacitor pair tied to the CBM JAB-RC pin set the maximum time that the transmitter is allowed to transmit. When transmission is attempted for a period longer than the specified time, the jabber inhibit function forces the transmitter to shut down and alerts the system that this has been done by generating a PHYSICAL ERROR indication on the serial interface indication channel. The error indication is removed only after a reset has occurred on the RESET pin or after a RESET command has been received on the station management interface. The ENABLE TRANSMITTER and DISABLE LOOPBACK commands can then be used to re-enable the transmitter outputs. While the PHYSICAL ERROR indication is present, the normally-low JAB pin of the MC68194 will be high. This TTL output may be used to turn off external transmitter circuitry or an isolation relay.

A block diagram of the jabber inhibit function is shown in Figure 3-3. When edges are present on the TXDATA line, the jabber capacitor is allowed to charge. When the transmitter stops transmitting, the capacitor is discharged. The circuit looks for any edges in the previous 16 TXCLKs before deciding whether to charge or discharge the capacitor. When the capacitor voltage reaches the reference threshold, the comparator switches and the jabber output is latched. The jabber output is fed back internally and disables the transmitter. This signal is also brought out to the JAB pin for use in disabling external transmitter circuitry.

For the IEEE 802.4 spec, the jabber timeout must be 0.5 sec ± 25%. An RC time constant of 265 millisec. will give about a 0.5 sec timeout. The maximum resistor size is 125 kΩ. Components should be 10% tolerance or better. Common values are R = 120 kΩ and C = 2.2 μF.

3.4 CLOCK GENERATOR

The clock generator is used to generate all of the transmit timing, TXCLK, and internal CBM timing for station management and loopback. The generator consists of a crystal oscillator/buffer that drives ÷2 and ÷4 stages. The oscillator frequency must be four times (4X) the serial data rate. As an example, the IEEE 802.4 5 Mbps carrier band (TXCLK = 5.0 MHz) requires an oscillator frequency of 20 MHz. The basic circuit is a single transistor Colpitts oscillator as shown in Figure 3-4.

The oscillator is used in one of three modes depending on the data rate and the application:

1. With a parallel-resonant, fundamental mode crystal.
2. With a parallel-resonant, overtone mode crystal.
3. With an external clock source.

The fundamental mode can typically be used up to frequencies of about 20 MHz; this is crystal dependent and some crystal types can be used as high as 40 MHz. Beyond the fundamental mode upper limit, an overtone mode crystal is used. An alternative to a crystal is an external clock source such as an integrated crystal clock to drive the CBM.

3.4.1 Parallel-Resonant, Fundamental Mode Crystal

Figure 3-4 shows the external crystal and capacitors C1 and C2 used for fundamental mode operation. The crystal must be parallel resonant with a maximum series resistance of 30 Ω.

This configuration is normally used for the IEEE 802.4 5 Mbps carrierband standard. The required transmit frequency stability is ± 100 ppm (0.01%). It is suggested that a crystal with a total frequency tolerance (calibration tolerance, temperature variation, plus aging) of ± 50 ppm to ± 60 ppm be used. The remaining frequency budget is reserved for the CBM and other components over temperature and power supply variation.

The series combination of C1 and C2 should be equal to the specified crystal load (typically 20 pF or 32 pF). Additionally, C1 and C2 should be large enough to swamp out the CBM device capacitance. The XTAL1 input capacitance is typically 1.5 pF to 2.0 pF, and C1 should be at least an order of magnitude greater (C1 > 20 pF). Also, C1 must be greater than the crystal load capacitance because of the series combination of C1 and C2. Generally the ratio C1:C2 is from 1:1 to 3:1.

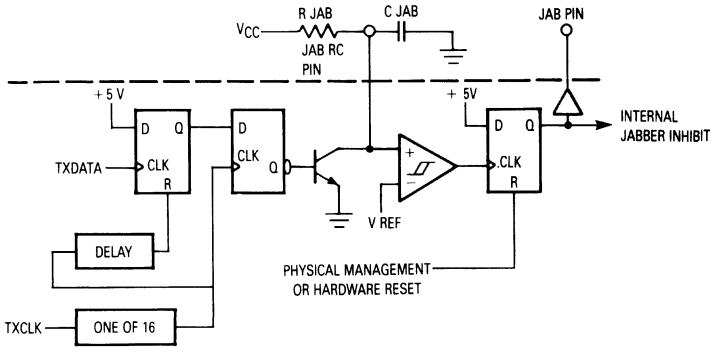


Figure 3-3. Jabber Inhibit Block Diagram

For a 20 pF crystal load:

$$20\ pF = C1C2/(C1 + C2)$$

and

$$C2 = 20\ pF\ [C1/(C1 - 20\ pF)]$$

Typical values are C1 = 60 pF and C2 = 30 pF.

It is suggested that best results will be had with close tolerance (5%) NPO ceramic capacitors — trimming should not be required. If trimming is necessary, a third trimming capacitor C3 can be placed in series with the crystal. Capacitors C1 and C2 will have to be increased in value because the crystal load now becomes C1 and C2 and C3 in series. For help in designing the capacitor network the user is directed to *Design of Crystal and Other Harmonic Oscillators,* B. Parzen, Wiley, 1983.

3.4.2 Parallel-Resonant, Overtone Mode Crystal

Figure 3-4 also shows the network used for overtone mode operation. The crystal is still parallel resonant, but must be specified for overtone (harmonic) operation at the desired frequency. A low series resistance of less than 30 Ω is recommended.

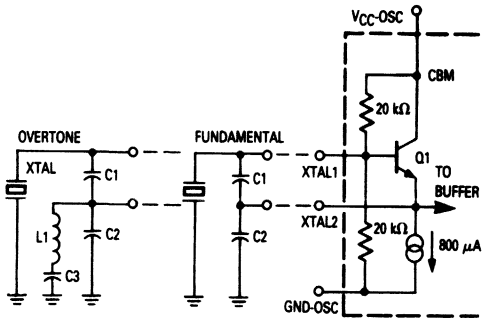


Figure 3-4. Crystal Oscillator Schematic Shows Configurations For Both Overtone and Fundamental Modes

Inductor L1 and capacitor C2 form a tank circuit that is parallel resonant at a frequency **lower** than the desired crystal harmonic but above the next lower odd harmonic. C3 = 0.01 μF is a dc blocking capacitor to ground. At the operating frequency the tank circuit impedance will appear capacitive; therefore, the load to the crystal is C1 in series with the capacitive reactance of the tank circuit.

This series combination should be equal to the desired crystal load. Typically, C2 will increase in value as compared to the fundamental mode situation because of the cancelling effects of L1. Again the user is directed to the above reference for optimum selection of components.

3.4.3 External Clock Source

Figure 3-5 shows the connection used for a TTL compatible external clock source. XTAL1 and XTAL2 are tied together defeating transistor Q1. External resistor R1 = 2.0 kΩ assures a high level greater than 3.0 V at an input current of 800 μA. The TTL driver must be capable of sinking 2.5 mA.

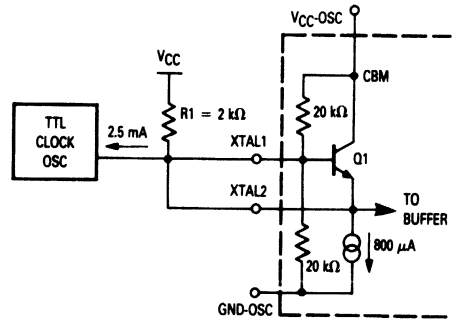


Figure 3-5. TTL Compatible Clock Source Driving CBM

The IEEE 802.4 for 5 Mbps or 10 Mbps data rate carrier band requires a transmit frequency stability of ± 100 ppm (0.01%). The external clock source must be specified for this stability over temperature.

SECTION 4
RECEIVER AMPLIFIER/LIMITER WITH CARRIER DETECT

4.1 OVERVIEW

The IEEE 802.4 spec provides that the incoming signal range for good signal is +10 dB (1.0 mV, 75 Ω) [dBmV] to +66 dB (1.0 mV, 75 Ω) [dBmV] available at the modem connector. The IEEE 802.4 further specifies that the modem will report silence for any signal below +4.0 dB (1.0 mV, 75 Ω) [dBmV]. Therefore, the receiver function must amplify any signal of +10 dBmV and above to limiting for good data recovery, and the signal detect must switch within the +4.0 dBmV to +10 dBmV window, that is, it must be "off" for +4.0 dBmV and below, and be "on" for +10 dBmV and above. The MC68194 requires a pre-amplifier of about 12 dB in front of the onboard amplifier and carrier detect function. Clock and data recovery are extracted from the amplified/limited incoming signal, and the carrier detect is used to control the clock and data recovery function based on presence of good signal.

4.2 AMPLIFIER

Figure 4-1 shows a simple block diagram of the receiver amplifier. Internally, dc feedback is used to bias the amplifier, and connection points FDBK and FDBK* are provided to ac bypass the feedback. With both receiver inputs RXIN and RXIN* available, the device can be wired either for differential or single-ended operation. Differential is preferred for low noise.

An external preamplifier with gain of about 12 dB is used with the onboard amplifier. The pre-amp can drive the CBM either single-ended or differentially. The onboard amplifier output signal is used in two ways. One path adds an additional limiter stage and is used to drive the clock and data recovery stages. The second path is used to develop carrier detect.

In the signal window where carrier detect must be active, the internal amplifier remains in the linear (nonlimiting) range. Its output is fullwave rectified, and the rectified signal is compared to an onboard threshold that is temperature and voltage compensated. The rectified signal is also brought out to an external lead called CARDET. A capacitor can be added at this pin which combines with the series 125 Ω resistor to form a low pass filter. This filtering is used to knock any high frequency noise off of the signal. The output of the comparator is a series of pulses (when the signal amplitude is sufficiently large) which are digitally integrated in the internal squelch signal.

4.3 CARRIER DETECTION THRESHOLD

The carrier detect threshold is internally generated and compensated for power supply and temperature variation. The THRESHOLD pin is provided to adjust the threshold via an external resistor tied to V_{CC}.

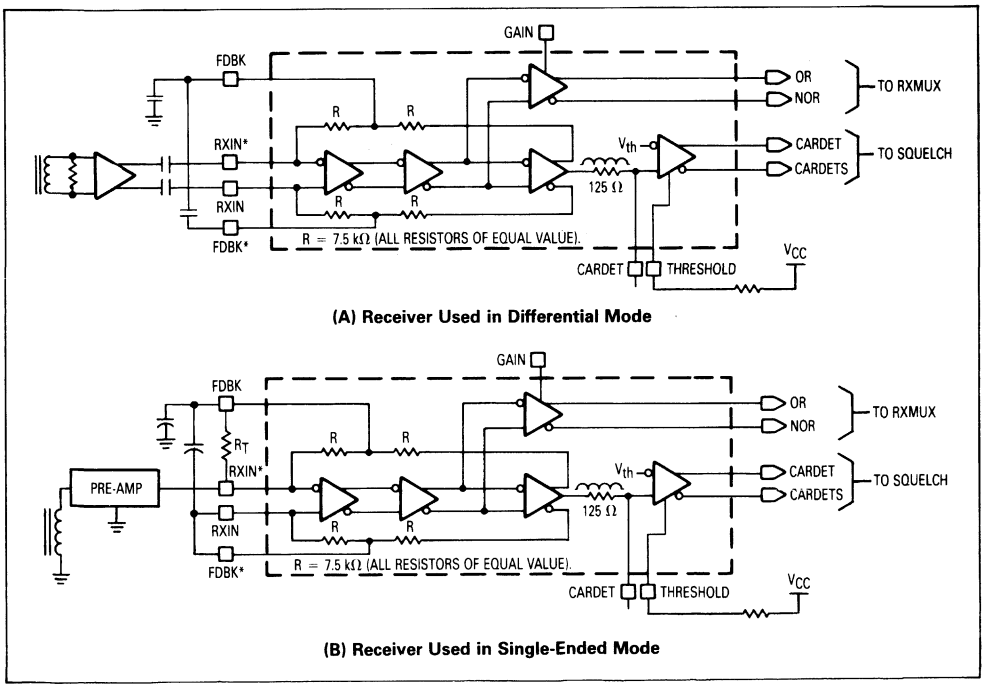


Figure 4-1. Receiver Amplifier With Carrier Detect

SECTION 5
CLOCK RECOVERY

5.1 OVERVIEW

The clock recovery circuitry is a key part of the receive function providing RX clock, a 2 times (2X) RX clock, and a 4 times (4X) RX clock for data recovery and to send receive symbols to the MAC. Figure 5-1 is a simplified functional schematic of the clock recovery logic. The clock recovery is fed by the output stage of the receive amplifier. The phase-coherent signal contains frequency components equal to 1X and 2X the serial data rate. Figure 5-2 shows an example of timing for a 5 Mb/s serial data rate. The RXOUT signal drives a one-shot with a time period of 75% of 1/2 bit time; this locks out edges caused by the higher frequency component. The one-shot is non-retriggerable and is triggered on both positive and negative going edges. This produces a pulse for every edge of the lower frequency.

The output of the one-shot is divided by 2 to produce a 50% duty cycle signal equal in frequency to the lower frequency of the phase-coherent signal. In turn, the ÷2 flip-flop output runs through a multiplexer to a phase-locked loop (PLL) system. The multiplexer selects the RXOUT signal when carrier detect is present; otherwise the local oscillator divided by 4 is selected.

The PLL system consists of a digital phase detector, an active loop filter, a voltage-controlled multivibrator (VCM), and a divide-by-4 feedback counter. When in phase lock, the output of the divide-by-4 feedback counter is locked to the reference clock. In turn, the VCM 4 times clock is also aligned with the reference clock as shown in Figure 5-2.

The 4 times clock from the VCM, the 2 times clock, and the 1 times clock are all in phase (when the PLL is phase-locked) with the reference clock, and are used to do data recovery. Note that the reference clock can be 180° out of phase with the bit time boundaries (Figure 5-2). This does not affect the 2X and 4X clocks which are used to sample the data. However, RXCLK can be out of sync with the bit time boundaries and special circuitry in the data recovery logic detects and corrects this condition.

When no valid input signal is available from the receive amplifier (carrier detect is not asserted), the multiplexer selects the local clock as a reference. This has the advantages of:

1. Supply a RXCLK when no data is present.
2. Holding the PLL in frequency lock so that only phase-lock must be achieved when switching to the RX signal.
3. Providing a smooth transition for RXCLK when moving from the local oscillator (at the beginning of a frame) and vice versa (at the end of a frame). The PLL acts as an integrator.

The IEEE 802.4 provides a PAD-IDLE or training signal at the beginning of any transmission. The PAD-IDLE for phase-coherent FSK is an alternating one and zero pattern, and the PLL is capable of being locked-in well within the 24 bit times (3 octets). The design goal is to be locked-in within 12–16 bit times. Data recovered during this lockup time at the beginning of a transmission can be invalid because the PLL clocks are not sync'ed. As a result the data recovery logic forces silence for 17–18 bit times after the carrier detect switches the reference clock (via the multiplexer) at the beginning of a received transmission.

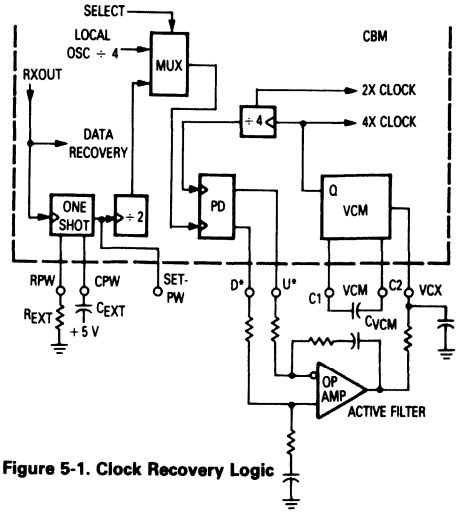
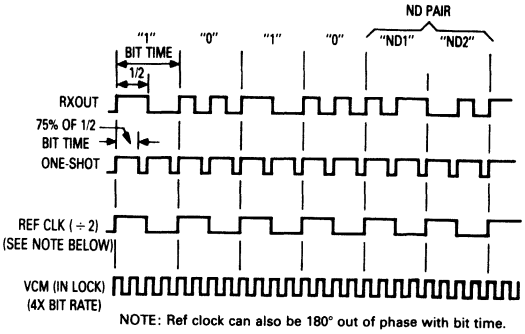


Figure 5-1. Clock Recovery Logic

5.2 ONE-SHOT

As previously stated, the one-shot is used to lock out the transitions due to the higher frequency component of the phase-coherent signal. The one-shot is non-retriggerable and fires off both edges of the incoming RXOUT signal. The time period should be set to 75% of half the bit time. As an example, the 5 Mb/s data rate has a 200 nsec bit time and the one-shot period then has a period of 75 nsec.



NOTE: Ref clock can also be 180° out of phase with bit time.

Figure 5-2. Clock Recovery Timing Signals

Figure 5-3 shows the arrangement of the external timing capacitor and resistor. The internal resistor R_{INT} may be used with or without an external resistor. A test pin is also provided (SET-PW) to monitor the pulse width.

For 5 Mbps operation, typically R_{PW} = 1.5 kΩ and C_{PW} = 33 pF.

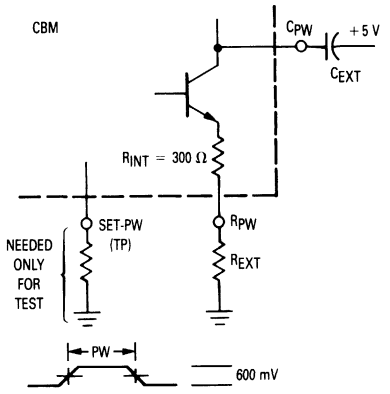
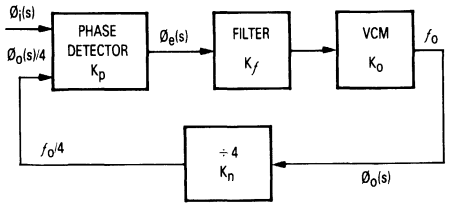


Figure 5-3. One-Shot Timing Components

5.3 PHASE-LOCKED LOOP (PLL) COMPONENTS

The PLL consists of a digital phase detector (PD), an active loop filter, a VCM, and a divide-by-4 feedback path. Figure 5-4 shows the fundamental elements of the PLL with their gain constants. The basic PLL allows the output frequency f_o to be "locked-on" to the input frequency f_i with a fixed phase relationship and to track it in frequency. When "in lock" the inputs to the phase detector have zero phase error. The input frequency is referenced to $f_o/4$.

A PLL follows classic servo theory and equations. In the following discussion a working knowledge of a PLL is assumed. For more background and applications information on PLL, the user is directed to Motorola Application Note AN535.



$\emptyset_e(s) = (1 / [1 + G(s) H(s)]) \emptyset_i(s)$

$\emptyset_o(s) = (G(s) / [G(s) H(s)]) \emptyset_i(s)$

where:

$G(s) = K_p K_f K_o \quad H(s) = K_n \quad K_n = 1 / N = 1/4$

Reference: Motorola App Note AN535

Figure 5-4. PLL Elements and Loop Equations

5.3.1 Phase Detector (PD)

The phase detector produces a voltage proportional to the phase difference between $\emptyset_i(s)$ and $\emptyset_o(s)/4$. This voltage after filtering is used as the control signal for the VCM. The PD has pump-up UP* and pump-down DOWN* outputs with a typical 800 mV logic swing. UP* produces a low level pulse equal in width to the amount of time the positive edge of $\emptyset_i$ (REF CLOCK) leads the positive edge of $\emptyset_o/4$ (VCM/4). DOWN* produces a low level pulse equal in width to the amount of time the positive edge of $\emptyset_i$ lags $\emptyset_o/4$. Both pulses will not occur on the same clock cycle as $\emptyset_o/4$ must either lead or lag $\emptyset_i$ when the PLL is out of lock. When in-lock, both outputs produce a very narrow pulse or negative spike.

The gain of the phase detector is equal to (reference Motorola app note AN532A):

K_p = (Logic swing)/2π = 800 mV/2π = 0.127 V/radian

5.3.2 Voltage Controlled Multivibrator (VCM)

The operating frequency range of the VCM is determined by the capacitor tied to pins VCM-C1 and VCM-C2. The capacitor should be selected to put the desired operating frequency in the center of the VCM tuning range.

The transfer function of the VCM is given by:

$$K_o = K_v/s$$

where K_v is the sensitivity in radians per second per volt. K_v is found by:

$$K_v = \frac{[(\text{Upper frequency limit}) - (\text{Lower frequency limit})]2\pi}{(\text{Control voltage tuning range})}$$

$$= 2\pi\,(\Delta f)/\Delta V_{CX} \text{ rad/s/V}$$

then

$$K_o = 2\pi\,(\Delta f)/(\Delta V_{CX})s \text{ rad/s/V}$$

5.3.3 Loop Filter

Since a Type 2 system is required (phase coherent output, see reference AN535), the loop transfer function of Figure 5-4 takes the form:

$$G(s)\,H(s) = [K\,(s+a)] / s^2$$

Writing the loop transfer function (from Figure 5-4) and relating it to the above form:

$$G(s)\,H(s) = [K_p K_v K_n K_f] / s = [K\,(s+a)] / s^2$$

Having determined K_p, K_o, and that K_n = 1/4 then K_f (filter transfer function) must take the form:

$$K_f = (s+a) / s$$

An active filter of the form shown in Figure 5-5A gives the desired results, where:

K_f = (R2 C s+1) / R1 C s (for large A)

The active filter can also be implemented as shown in Figure 5-5B using an alternate approach of a charge pump. The advantage of the charge pump design is that it can be implemented using only a single 5.0 volt supply. Its transfer function is:

K_f = (RC s +1) / C s

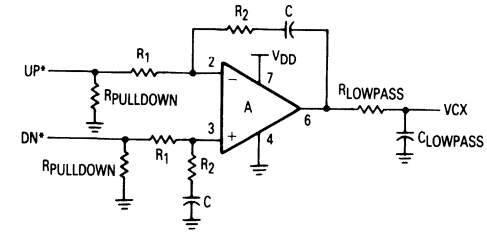


Figure 5-5A. Active Filter Using Op Amp

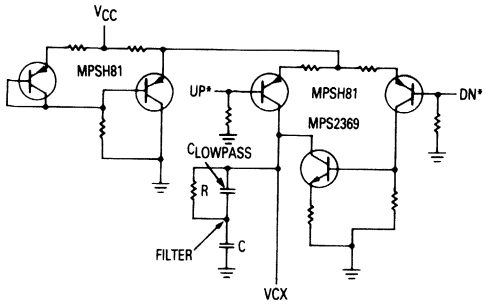


Figure 5-5B. Charge Pump/Filter

5.3.4 Loop Characteristics

If an active filter as shown with an op amp is used, the general PLL loop transfer function now becomes:

$$G(s)\,H(s) = K_p\,K_f\,K_o\,K_n$$
$$= K_p\,[(R2\,C\,s+1)\,/\,R1\,C\,s]\,(K_v/s)\,(1\,/\,N)$$

Its characteristic equation is set to the form:

$$C.E. = 1 + G(s)\,H(s) = 0$$
$$= s^2 + (K_p\,K_v\,R2)\,s\,/\,(R1\,N) + (K_p\,K_v)\,/\,(R1\,C\,N)$$

Relating to the standard form $(s^2 + 2\zeta\omega_n s + \omega_n 2)$ and solving:

$$\omega_n^2 = (K_p\,K_v)\,/\,R1\,C\,N \quad 2\zeta\omega_n = (K_p\,K_v R2)\,/\,R1\,N$$

where

ω_n = Natural frequency
ζ = damping factor.

If a charge pump loop filter is used, the general PLL loop transfer function alternately becomes:

$$G(s)\,H(s) = K_p\,K_f\,K_o\,K_n$$
$$= K_p[(R\,C\,s + 1)\,/\,C\,s]\,(K_v\,/\,s)\,(1\,/\,N)$$

Its characteristic equation is set to the form:

$$C.E. = 1 + (Gs)\,H(s) = 0$$
$$= s^2 + (K_p\,K_v\,R)\,s\,/\,(N) + (K_p\,K_v)\,/\,(C\,N)$$

Relating to the standard form $(s2 + 2\zeta\omega_n s + \omega_n 2)$ and solving:

$$\omega_n^2 = (K_p\,K_v)\,/\,C\,N \quad 2\zeta\omega_n = (K_p\,K_v\,R)\,/\,N$$

SECTION 6
DATA RECOVERY

6.1 OVERVIEW

The RXOUT signal from the receive amplifier and clocks generated by the clock recovery logic are used by the data recovery logic. The MC68194 recovers the data from the encoded receive signal by opening sampling windows around the 1/4 and 3/4 bit time positions and looking for edges in the received signal (refer to Figure 6-1 for the encoded data representations). A data ONE has transitions only at the 0 and 1/2 bit time positions. A data ZERO has transitions at the 0, 1/4, 1/2, and 3/4 bit

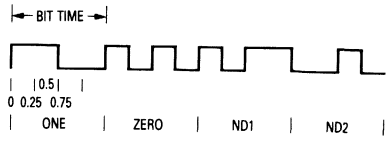


Figure 6-1. Encoded Data Representation

7

time positions. A NON-DATA symbol has transitions at the 0, 1/4, and 1/2 bit time positions (ND1) or at the 0, 1/2, and 3/4 bit time positions (ND2). NON-DATA symbols should always occur in pairs; each pair is made up of one of each type of NON-DATA encoded symbols as shown in Figure 6-2 (ND1 followed by ND2).

ONEs, ZEROs, and NON-DATA pairs can be easily decoded by keeping track of the 1/4 and 3/4 bit time position transitions. The ONEs, ZEROs, and NON-DATA pairs are then reported on the RXSYMX pins as described in the serial interface discussion. Two other conditions can also be reported while receiving in MAC mode — BAD SIGNAL and SILENCE. BAD SIGNAL is reported when a ND1 symbol is not followed immediately by a ND2 symbol or when a ND2 symbol is received and not immediately preceded by a ND1 symbol.

SILENCE is reported when one of four conditions occurs:

1. When the amplitude of the received signal is not large enough to trigger the on-chip carrier detect circuit. Reporting SILENCE when the carrier detect signal is not asserted prevents the chip from responding to low level noise.
2. When in internal loopback mode and SILENCE is being requested on the TXSYMX pins, SILENCE will be reported on the RXSYMX pins. An internal digital carrier detect is used during loopback and this signal is negated when SILENCE is requested on the request channel.
3. During the PLL training period at the beginning of a transmission. When an incoming signal first triggers the carrier detect in the amplifier, the PLL must lock to the new reference clock (generated from the data stream). During the lockup time, recovered data may not be valid. The data recovery logic forces SILENCE for a fixed period of time (17–18 bit times).
4. During end-of-transmission blanking. See Section 6.2.

The PAD-IDLE at the beginning of a transmission is used as a training signal as described in the clock recovery section. After the PLL has achieved lock, the recovered clock at this point may be in phase or 180° out of phase with the bit time clock at the sending end. This creates a problem for RXCLK and the data recovery logic because symbols would be decoded as the wrong combination of 1/2 bit time transitions.

Logic in the data recovery circuitry corrects for this situation. If the clock is 180° out of phase, the PAD-IDLE sequence (ONE, ZERO, ONE, ZERO, ONE, . . .) will be decoded as a sequence of NON-DATA symbols. Refer to Figure 6-2. In normal data reception, NON-DATA symbols occur only in pairs; there are never three or more in a row. Therefore, three or more NON-DATA symbols occurring in a row indicate that the bit time clock is 180° out

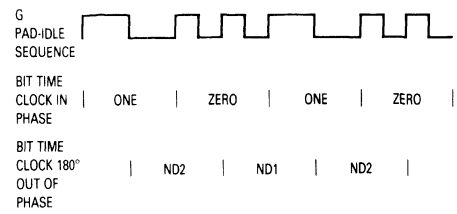


Figure 6.2 Training Sequence Decoded With In-Phase and Out-Of Phase Clocks

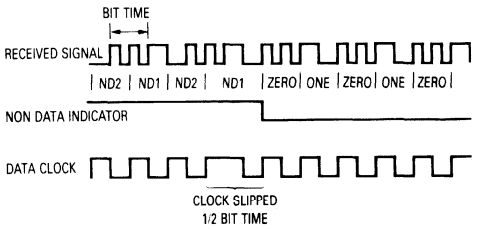


Figure 6-3. Clock Slip To Bring In Phase With Data Stream

of phase and the bit time clock (RXCLK) must be slipped as shown in Figure 6-3. The clock frequency and phase have now been recovered and symbol decode proceeds as described above.

6.2 RECEIVER END-OF-TRANSMISSION BLANKING

The IEEE 802.4 requires that the physical layer recognize the end of a transmission and report silence to the MAC for a period thereafter. This period of silence is referred to as blanking and must meet the following conditions:

1. Blanking must begin no later than 4 MAC-symbol times after the last MAC-symbol of the End Delimiter (i.e., the last End Delimiter of the transmission).
2. Blanking must continue to a point at least 24 MAC-symbol times but not more than 32 MAC-symbol times from the last MAC-symbol of the End Delimiter.

The MC68194 provides this function by recognizing the last End Delimiter of a transmission (I Bit = 0, see Section 1.3). The CBM reports silence for 32 symbols after the last symbol of the End Delimiter.

The blanking function can be disabled for test purposes or non-IEEE 802.4 applications via the EOTDIS* input.

7

SECTION 7
SERIAL INTERFACE

7.1 OVERVIEW

The serial interface is composed of the Physical Data Request Channel and the Physical Data Indication Channel. The serial interface is used to pass commands and data frames to and from the CBM.

7.2 PHYSICAL DATA REQUEST CHANNEL

Five signals comprise the physical data request channel. Three of these signals (TXSYM2, TXSYM1 and TXSYM0) are multiplexed and have different meanings depending on the mode of SMREQ*. When SMREQ* is equal to one, the MAC mode is selected. When SMREQ* is equal to zero, the physical layer management mode is selected.

7.2.1 TXCLK — Transmit Clock

The transmit clock can be from 1.0 to 10 MHz. TXSYM2, TXSYM1, TXSYM0 and SMREQ* are synchronized to TXCLK. The IEEE 802.4 standard for carrier band allows for 5.0 or 10 MHz clocks.

7.2.2 SMREQ* — Station Management Request

SMREQ* directs the physical layer to be in MAC or physical layer management mode. In MAC mode SMREQ* = 1 and in management mode SMREQ* = 0.

7.2.3 TXSYM0, TXSYM1, and TXSYM2 — Transmit Symbols

In physical layer management mode TXSYM2, TXSYM1 and TXSYM0 have the meanings shown in Figure 7-1.

State	TXSYM2	TXSYM1	TXSYM0
RESET	1	1	1
DISABLE LOOPBACK	1	0	1
ENABLE TRANSMITTER	0	1	1
SERIAL SM DATA/IDLE	0	0	0/1

Figure 7-1. Request Channel Encoding for Physical Management Mode (SMREQ* = 0)

The CBM supports only four station management commands (RESET, LOOPBACK DISABLE, ENABLE TRANSMITTER and IDLE) encoded on lines TXSYM2, TXSYM1 and TXSYM0. The CBM does not support the SMDATA commands, but responds with a **"NACK"**. In MAC mode, the encoding for TXSYM2, TXSYM1, and TXSYM0 are shown in Figure 7-2.

Symbol	TXSYM2	TXSYM1	TXSYM0
ZERO	0	0	0
ONE	0	0	1
NON-DATA	1	0	X
PAD-IDLE	0	1	X
SILENCE	1	1	X

Where:

ZERO is binary zero.
ONE is binary one.
NON-DATA is a delimiter flag and is always present in pairs.
PAD-IDLE is one symbol of preamble/interframe idle.
SILENCE is silence or no signal.

Figure 7-2. Request Channel Encoding For MAC Mode (SMREQ* = 1)

7.3 PHYSICAL DATA INDICATION CHANNEL

Five signals comprise the physical data indication channel. Three of these signals (RXSYM2, RXSYM1 and RXSYM0) are multiplexed and have different meanings depending on the state of SMIND*. When SMIND* is equal to one, the physical layer is in MAC mode and when SMIND* is equal to zero, the physical layer is in management mode or an error has occurred.

7.3.1 RCXLK — Receive Clock

The receive clock can be from 1.0 to 10 MHz. RXSYM2, RXSYM1, RXSYM0, and SMIND* are synchronized to RXCLK. The IEEE 802.4 standard for carrier band networks allows 5.0 or 10 MHz clocks.

7.3.2 SMIND* — Station Management Indication

SMIND* indicates whether the physical layer is in MAC mode (SMIND* = 1) or management mode (SMIND* = 0) of operation. When in MAC mode of operation, the physical layer has RXSYM2, RXSYM1, and RXSYM0 encoded indicating data reception. When in management mode of operation, the physical layer RXSYM2, RXSYM1 and RXSYM0 are encoded to confirm response to received commands or to indicate a physical error (jabber inhibit).

7.3.3 RXSYM0, RXSYM1 and RXSYM2 — Receive Symbols

The encoding for RXSYM2, RXSYM1, and RXSYM0 in physical management mode is shown in Figure 7-3:

State	RXSYM2	RXSYM1	RXSYM0
NACK (non-acknowledgement)	1	0	*
ACK (acknowledgement)	0	1	*
IDLE	0	0	1
Physical Layer Error	1	1	1

*Indicates RXSYM0 contains the SM RX data when responding to a serial data command.

Figure 7-3. Indication Channel Encoding For Physical Management Mode (SMIND* = 0)

The encoding of RXSYM2, RXSYM1, and RXSYM0 in MAC mode is shown in Figure 7-4.

Symbol	RXSYM2	RXSYM1	RXSYM0
ZERO	0	0	0
ONE	0	0	1
NON-DATA	1	0	X
SILENCE	1	1	X
BAD SIGNAL	0	1	X

Where:

ZERO is the received data zero.
ONE is the received data one.
NON-DATA is a delimiter flag and is always present in pairs.
SILENCE is silence or no signal.
BAD SIGNAL is received bad signal.
X = Don't care.

Figure 7-4. Indication Channel Encoding For MAC Mode (SMIND* = 1)

SECTION 8
PHYSICAL MANAGEMENT

8.1 OVERVIEW

The MC68194 supports four physical management commands on the request channel: RESET, DISABLE LOOPBACK, ENABLE TRANSMITTER, and IDLE. The serial data station management commands are not implemented in the MC68194. These unimplemented commands are typically used to set up and read registers or control bits within a more complex modem. The CBM does not have registers and does not require the SMDATA commands. Upon reception of a SMDATA command, the CBM will respond with a NONACKNOWLEDGEMENT (NACK) and a response byte in accordance with the IEEE DTE-DCE Interface Standard. The data in the response byte is all ZEROs. Receipt of a RESET, DISABLE LOOPBACK, or ENABLE TRANSMITTER command will abort the SMDATA response.

8.2 RESET

The RESET command performs the same function as the RESET pin; the internal loopback mode is enabled, the transmitter outputs are disabled and TXDIS is enabled, and the jabber inhibit timeout is cleared. In addition the RESET command will generate an ACKNOWLEDGEMENT response (ACK) on the RXSYMx pins.

The RESET pin is an asynchronous function. When taken high it resets the CBM as described above leaving the CBM ready to respond to the physical data request channel.

NOTE: For the MC68194 to respond properly to commands after a hardware reset, the request channel must either be in MAC mode upon exiting the hardware reset or the request channel must go to MAC mode briefly before going to management mode. If the MC68194 is in management mode upon exiting the hardware reset, it remains reset and does not recognize the command because it is waiting for a MAC mode to management mode transition. This situation can be corrected by either exiting hardware reset with the request channel in MAC mode or putting the request channel in MAC mode briefly before issuing any management commands. See Section 8.6 for command response timing.

8.3 INTERNAL LOOPBACK

The internal loopback mode is provided for testing the CBM. In this mode a multiplexer selects the internal transmitter signal to drive the clock recovery and data recovery portions of the receive circuitry. This transmit signal is taken just prior to the output buffer stages of the transmitter circuit.

The loopback mode can only be selected via RESET (management command or external pin). Loopback mode is exited upon receipt of the management command DISABLE LOOPBACK. The CBM will respond with ACK to this command.

A normal sequence of events to test the CBM then would be:

1. Initialize the CBM via a RESET command or hardware reset.
2. Return to MAC mode and send test data. The CBM is full duplex.
3. In management mode, send DISABLE LOOPBACK command to exit loopback.

Following the test the modem can be setup for standard operation.

8.4 STANDARD OPERATION

Standard operation requires that the transmitter be enabled as well as disabling loopback. The transmitter is automatically disabled on RESET. Three things must happen after a RESET before transmissions can begin:

1. Loopback mode must be exited with the DISABLE LOOPBACK command. The MC68194 responds to this command with the ACK management response.
2. The transmitter must be activated with the ENABLE TRANSMITTER command. The MC68194 responds to this command with the ACK management response.
3. The MC68194 must exit the management mode and enter the MAC data mode.

The CBM is now ready to send and receive data, i.e., the CBM is in MAC or data mode, loopback is disabled, and the transmitter is enabled.

8.5 IDLE

The CBM provides the IDLE response when an IDLE management command is received. In addition, the IDLE response is returned for all invalid, as opposed to unimplemented (SMDATA) commands.

8.6 COMMAND RESPONSE TIMING

The MC68194's management command/response operation is:

1. ACK response to RESET, DISABLE LOOPBACK, and ENABLE TRANSMITTER within 2 clock periods. As shown in Figure 8-1, the precise response time depends on the relative phase of the TXCLK and the RXCLK signals. If they are in phase, the response will be available at the RXSYMx pins 1.5 clocks after the command is latched. If the clocks are 180° out of phase, the delay will be 2 clocks. The command should be held on the TXSYMX pins until the response is received on the RXSYMX pins.
2. The IDLE command and all invalid commands will produce the IDLE response with the same delay as described above.
3. The SMDATA command response timing is shown in Figure 8-2. The NAK response to the SMDATA command is available on the RXSYMX pins in 2.5 or 3 clock periods depending on the relative phases of the TXCLK and RXCLK signals. When NAK becomes valid, RXSYM0 is low creating a start bit

for the response byte. NAK is held for 9 clock periods with RXSYM0 low (start bit plus 8 ZERO data bits). NAK is held for one additional clock with RXSYM0 high. This is the stop bit and mark the end of the SMDATA response byte. 12.5 or 13 clock periods after receiving the SMDATA command the NAK response is removed.

In management mode, RXCLK is always locked to TXCLK. These clocks may be in phase or 180° out of phase as discussed above. This uncertainty exists because the clock recovery PLL can lock to either phase of the local clock. The response delays relative to TXCLK may therefore differ by 1/2 clock period. The MC68194 must leave management mode, enter MAC mode, and return to management mode for a phase change to occur. The relative phase of the two clocks will not change while in management mode.

Because the clock recovery PLL requires a training period when first entering management mode, the PLL must have sufficient time to lock to the new clock source (TXCLK) before being required to provide a response. To provide enough time for the PLL to lock up, the MC68194 delays 16.5 to 17 clock periods before entering station management mode (SMIND* = 0) after the station management mode is selected (SMREQ* = 0). Refer to Figure 8-3 for the timing diagram. During this delay, the MAC mode SILENCE response will be present on the RXSYMX pins.

Users must be aware that when first requesting management mode there will be this added delay before the mode is entered and a response is available. If a management command is sent along with the station management mode request (SMREQ* = 0) and held on the TXSYMX pins until the CBM enters station management mode, the proper response will be available on the RXSYMX pins immediately except in the case of SMDATA commands. SMDATA commands must not be requested on the TXSYMX pins until after SMIND* indicates that station management mode has been entered.

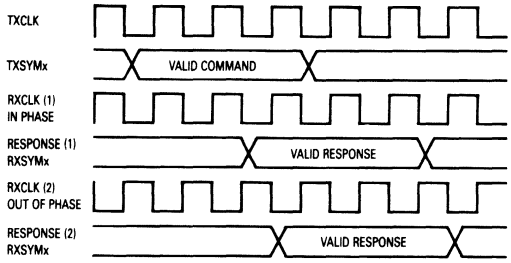


Figure 8-1. Parallel Command Response Time

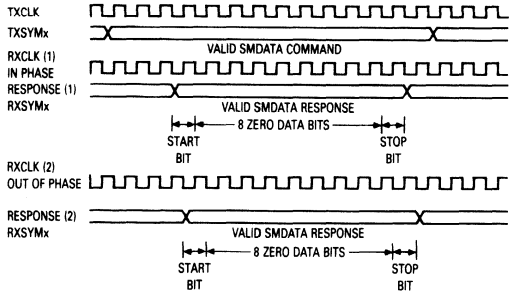


Figure 8-2. SMDATA Command Response Time

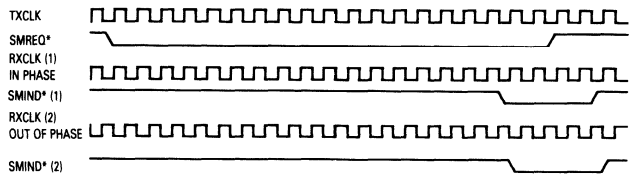


Figure 8-3. Station Management Request Response Time

SECTION 9
MC68194 CARRIER BAND MODEM
ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS (Limits Beyond Which Device Life May Be Impaired)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	0 to +7.0	Vdc
TTL Input Voltage	V_{IN}	0 to +5.5	Vdc
TTL Output Voltage (Applied to output HIGH)	V_{OUT}	0 to +5.5	Vdc
ECL Output Source Current	I_{out}	50	mAdc
Storage Temperature Cerquad	T_{stg}	−55 to +165	°C
Junction Temperature Cerquad	T_J	165	°C

GUARANTEED OPERATING RANGES

Characteristic	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Operating Temperature (Cerquad in still air)	T_A	0	25	70	°C

DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
TTL INPUTS (TXSYM0-TXSYM2, SMREQ*, RESET, EOTDIS)† (T_A = 0–70°C, V_{CC} = 5.0 Vdc ± 5%)						
Input HIGH Voltage	V_{IH}	2.0			Vdc	
Input LOW Voltage	V_{IL}			0.8	Vdc	
Input HIGH Current	I_{IH}			20	μA	V_{CC} = MAX, V_{IN} = 2.7 Vdc
Input LOW Current	I_{IL}			−0.7	mA	V_{CC} = MAX, V_{IN} = 0.4 Vdc
† All TTL inputs include a 15 k-ohm pullup resistor to V_{CC}.						
TTL OUTPUTS (TXCLK, RXSYM0-RXSYM2, SMIND*, RXCLK, JAB) (T_A = 0–70°C, V_{CC} = 5.0 Vdc ± 5%)						
Output HIGH Voltage	V_{OH}	2.7			Vdc	V_{CC} = MIN, I_{OH} = MAX
Output LOW Voltage	V_{OL}			0.5	Vdc	V_{CC} = MIN, I_{OL} = MAX
Output HIGH Current	I_{OH}			−0.4	mA	
Output LOW Current	I_{OL}			8.0	mA	
ECL OUTPUTS (TXOUT, TXOUT*) (T_A = 25°C, V_{CC} = 5.0 Vdc)						
Output HIGH Voltage	V_{OH}		4.10		Vdc	$R_{pulldown}$ = 220 Ω
Output LOW Voltage	V_{OL}		3.28		Vdc	$R_{pulldown}$ = 220 Ω
OPEN COLLECTOR OUTPUT (TXDIS) (T_A = 25°C, V_{CC} = 5.0 Vdc)						
Output LOW Current	I_{OL}	450		550	μA	V_{OL} = 3.0 Vdc
Output HIGH Leakage Current	I_{OH}			50	μA	V_{OH} = 5.0 Vdc

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DC ELECTRICAL CHARACTERISTICS — continued

OTHER PARAMETERS
(T_A = 25°C, V_{CC} = 5.0 Vdc)

POWER SUPPLY DRAIN CURRENT

Characteristic	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Power Supply Drain Current	I_{CC}		220	270	mA	No outputs loaded, TTL inputs open.
RECEIVER (SINGLE-ENDED OPERATION)						
GAIN Output Voltage HIGH	G_{VOH}		4.2		Vdc	I_{OH} = 5.0 mA
GAIN Output Voltage LOW	G_{VOL}		3.6		Vdc	I_{OL} = 5.0 mA
Input Signal (for limiting)	RV_{IN}		+17		dBmV	GAIN output = 600 mV
Detected Threshold	V_{thres}		+18		dBmV	R_{THRES} = 120 kΩ to V_{CC}
PHASE DETECTOR OUTPUTS (UP*, DOWN*)						
Phase Detector Output Voltage HIGH	PD_{VOH}		4.0		Vdc	I_{OH} = 10 mA
Phase Detector Output Voltage LOW	PD_{VOL}		3.3		Vdc	I_{OL} = 10 mA
VCM						
VCM Oscillator Frequency	F_{osc1}		40		MHz	C_{vcm} = 24 pF, RXCLK = 5.0 MHz, VCX = 3.6 Vdc
	F_{osc2}		20		MHz	C_{vcm} = 68 pF, RXCLK = 10 MHz, VCX = 3.6 Vdc
VCM Tuning Ratio	TR		4.0			
VCX Tuning Range	V_{CX} V_{CX}	2.6		4.6	Vdc	
ONE-SHOT						
SET-PW Output Voltage HIGH	PW_{VOH}		4.2		Vdc	I_{OH} = 5.0 mA
SET-PW Output Voltage LOW	PW_{VOL}		3.6		Vdc	I_{OL} = 5.0 mA
Timing Current	IT		0.8	4.0	mA	
Internal Resistor	R_{int}		300		Ohms	
Timing Reference Voltage (measured at RPW pin)	V_{ref}	1.2	1.3	1.4	Vdc	IT = 0.8 mA
External Timing Resistor	R_{EXT}		1.5		kΩ	For 5.0 Mb/s data rate.
External Timing Capacitor	C_{EXT}		33		pF	For 5.0 Mb s data rate.
JABBER TIMER						
RC Threshold High	JAB_{VIH}		4.25		Vdc	I_{IN} = 5.0 μA Max
RC Output V_{OL}	JAB_{VOL}		0.4		Vdc	I_{OL} = 10 mA
Jabber Resistor	R_{JAB}		120	125	kΩ	For 0.5 sec timing
Jabber Capacitor	C_{JAB}		2.2		μF	For 0.5 sec timing
CRYSTAL OSCILLATOR						
Input HIGH Voltage	V_{IH}	3.0			Vdc	XTAL1 & XTAL2 tied together
Input LOW Voltage	V_{IL}			2.0	Vdc	XTAL1 & XTAL2 tied together

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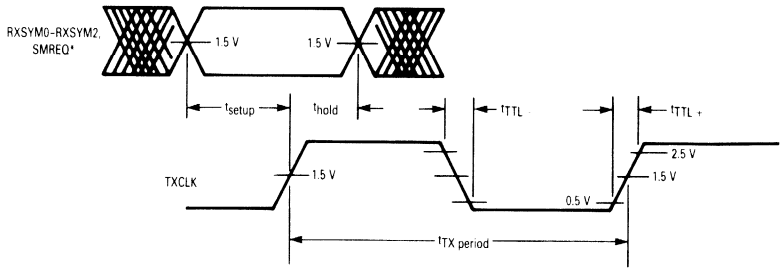
AC ELECTRICAL CHARACTERISTICS††
(T_A = 0–70°C, V_{CC} = 5.0 Vdc ± 5%)

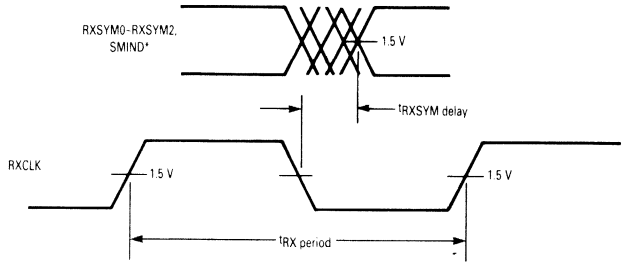
Characteristic	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
TXCLK Period	$t_{TXperiod}$	180	200	220		@ 5.0 MHz, Figure 9-1A.
RXCLK Period	$t_{RXperiod}$	180	200	220		@ 5.0 MHz, PLL locked to TXCLK, Figure 9-1B.
TTL Rise/Fall Time	$t_{TTL\pm}$		4.0		ns	Figure 9-1A.
TXSYMX, SMREQ* Setup Time (to TXCLK)	t_{setup}		15	25	ns	Figure 9-1A.
TXSYMX, SMREQ* Hold Time (to TXCLK)	t_{hold}		−9.0	0	ns	Figure 9-1A.
RXSYMX, SMIND* Delay Time (to RXCLK)	$t_{RXSYM\ delay}$	0	2.5	5.0	ns	Figure 9-1B.
XTAL1,2 to TXCLK Delay	$t_{TXCLK\ delay}$		18		ns	Figure 9-1C. XTAL1 and XTAL2 tied together and driven with external source.
TXOUT, TXOUT* Rise/Fall Time	$t_{TXOUT\pm}$		1.5		ns	$R_{pulldown}$ = 500 Ω
UP*, DOWN* Rise/Fall Time	$t_{PD\pm}$		1.5		ns	$R_{pulldown}$ = 500 Ω
TXDIS Rise/Fall Time	$t_{TXDIS\pm}$		35		ns	2.0 kΩ pullup to V_{CC}. **Do not use Figure 9-2 test load.**

†† See Figure 9-2 for AC test load.

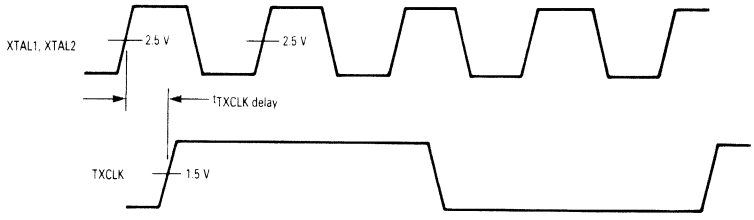
7



(A) TXSYMX, SMREQ* Setup and Hold Timing to TXCLK



(B) RXSYMX, SMIND* Delay Timing to RXCLK



(C) TXCLK Delay Timing to XTAL1, XTAL2

Figure 9-1. AC Test Waveforms

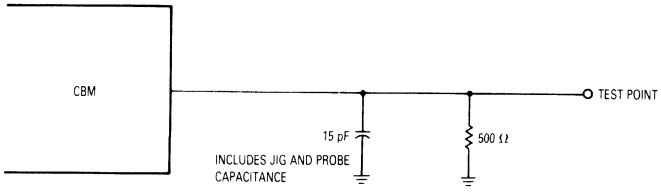


Figure 9-2. TTL, TXOUT, TXOUT*, Up* & Down* AC Test Load

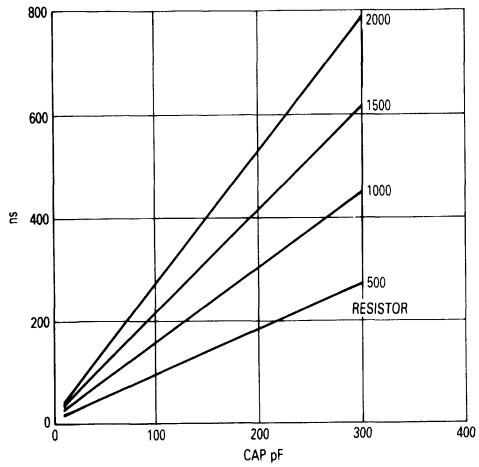


Figure 9-3. One Shot Pulse Width versus Rext/Cext

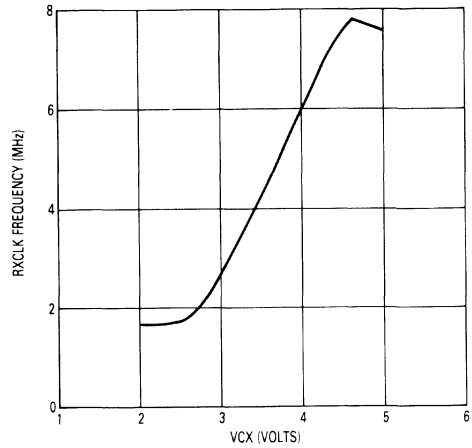


Figure 9-4. VCM Frequency versus Control Voltage (V_{CC} = 5.0 Vdc & C = 68 pF)

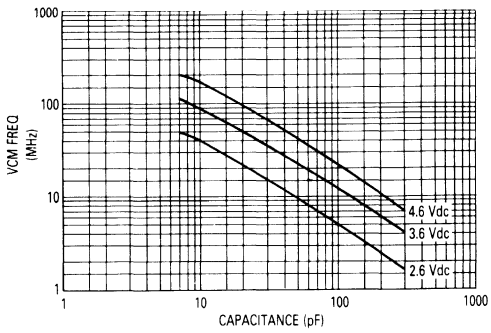


Figure 9-5. VCM Frequency versus Capacitance

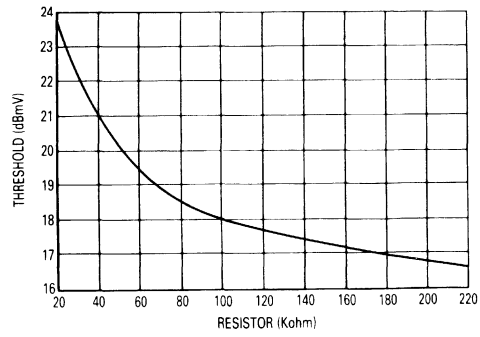


Figure 9-6. Detected Threshold versus Threshold Resistor

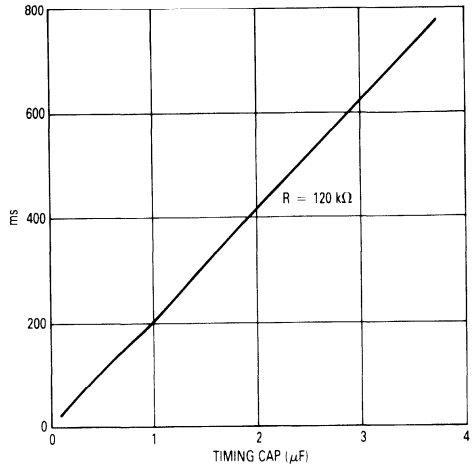
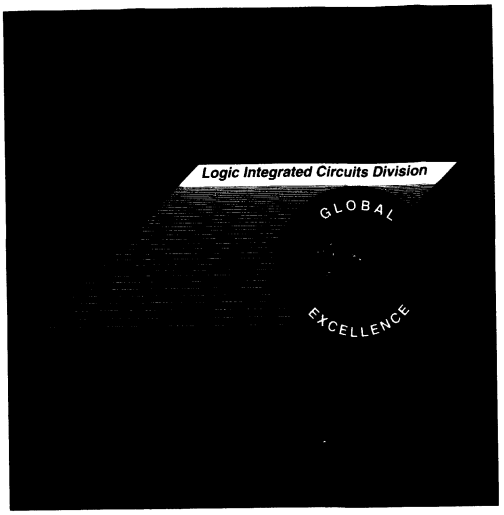


Figure 9-7. Jabber Time Constant versus Capacitance

7



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